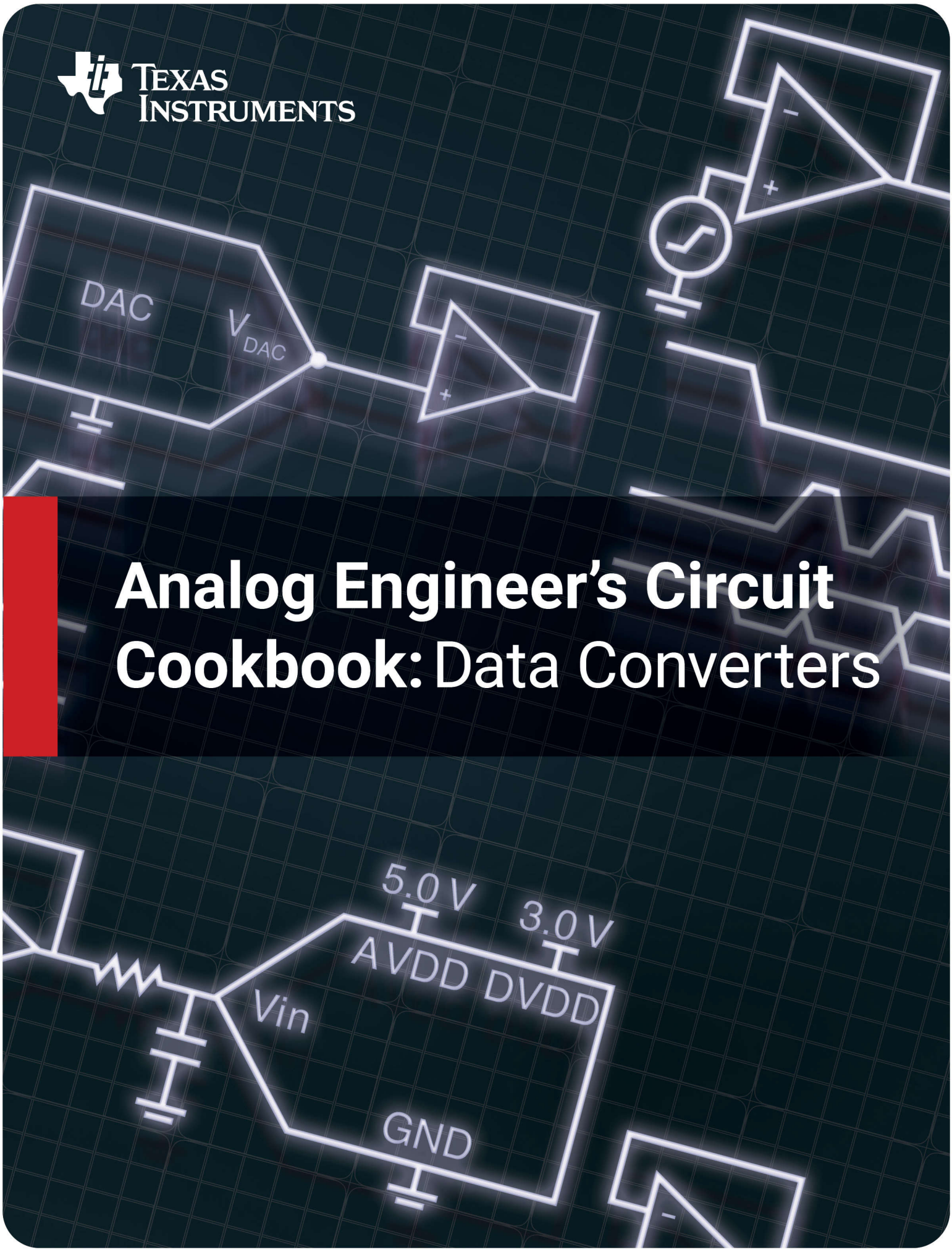
Texas Instruments



Analog Engineer's Circuit Cookbook: Data Converters

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Third Edition
SLYY138 - 12/2024

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Message from the editors

The *Analog Engineer's Circuit Cookbook: Data Converters* provides analog-to-digital converter (ADC) and digital-to-analog converter (DAC) sub-circuit ideas that can be quickly adapted to meet your specific system needs. Each circuit is presented as a "definition by example." They include step-by-step instructions, like a recipe, with formulas enabling you to adapt the circuit to meet your design

goals. Additionally, all circuits are verified with SPICE simulations and include links to the corresponding TINA-TI™ SPICE circuits.

We've provided at least one recommended data converter for each circuit, but you can swap it with another device if you've found one that's a better fit for your design. You can search our large portfolio of **data converters**.

Our circuits require a basic understanding of amplifier and data converter concepts. If you're new to data converter design, we highly recommend completing our TI Precision Labs (TIPL) training series. TIPL includes courses on introductory topics, such as device architecture, as well as advanced, application-specific problem-solving, using both theory and practical knowledge. Check out our curriculum for amplifiers, data converters and more at: **TI Precision Labs**.

We plan to update this e-book with new ADC and DAC circuit building blocks and encourage you to see if your version is the latest at **TI Analog Circuits**.

We hope you find our collection of data converter circuits helpful in developing your designs!

Additional Resources to Explore

TI Precision Labs

ti.com/precisionlabs

- On-demand courses and tutorials ranging from introductory to advanced concepts that focus on application-specific problem solving
- Hands-on labs and evaluation modules (EVM) available
  - TIPL Op Amps experimentation platform, **ti.com/TIPL-amp-evm**
  - TIPL SAR ADC experimentation platform, **ti.com/TIPL-adc-evm**

Analog Engineer's Pocket Reference

ti.com/analogrefguide

- PCB, analog and mixed-signal design formulae; includes conversions, tables and equations
- e-book, iTunes and Android apps and hardcopy available

***The Signal* e-book**

ti.com/signalbook

- Short, bite-sized lessons on on op-amp design topics, such as offset voltage, input bias current, stability, noise and more

Reference Designs

ti.com/referencedesigns

- Ready-to-use reference designs with theory, calculations, simulations schematics, PCB files and bench test results

Data Converter Parametric Quick Search

- Find your next precision or high-speed ADC, **ti.com/ADC-search**
- Find your next precision or high-speed DAC, **ti.com/DAC-search**
  - TINA-TI simulation software: **ti.com/tool/TINA-TI**
- Complete SPICE simulator for DC, AC, transient and noise analysis
- Includes schematic entry and post-processor for waveform math

Analog Engineer's Calculator

ti.com/analogcalc

- ADC and amplifier design tools, noise and stability analysis, PCB and sensor tools

PCB and sensor tools

- For online technical support, see the **TI E2E™ design support forums**

Table of Contents

Analog Engineer's Circuit

Driving a SAR ADC Directly Without a Front-End Buffer Circuit (Low-Power, Low-Sampling-Speed DAQ)

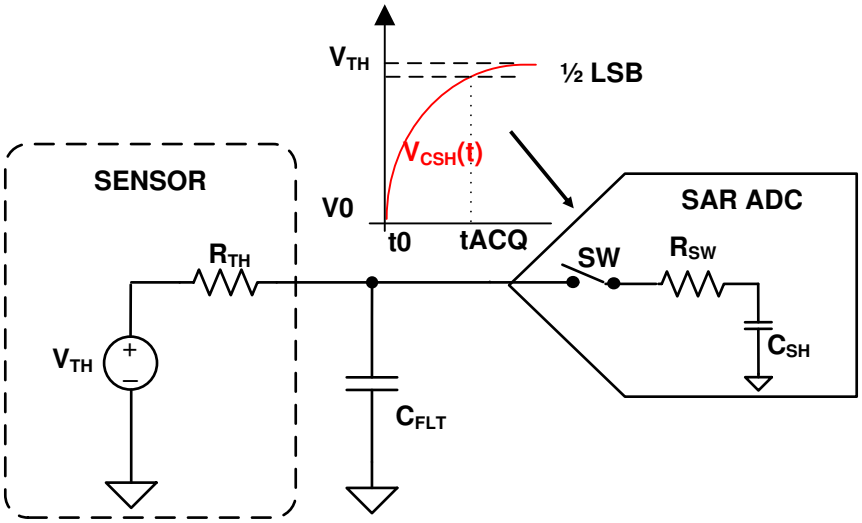
Abhijeet Godbole

Design Description

This design explains how sensor outputs can be directly interfaced with a SAR ADC input. In applications such as wireless environmental sensors, gas detectors, and smoke and heat detectors, the input is very slow-moving and the sensor output voltage is sampled at fairly slower speeds (10ksps or so). In such or similar systems, the sensor output can be directly interfaced with the SAR ADC input without the need for a driver amplifier to achieve a small form-factor, low-cost design.

Interfacing Sensor Output Directly to a SAR ADC

The following figure shows a typical application diagram for interfacing a sensor directly to a SAR ADC input without the use of a driver amplifier. The sensor block highlights the Thevenin equivalent of a sensor output. Voltage source, V_{TH}, is the Thevenin-equivalent voltage and source resistance R_{TH} is the Thevenin-equivalent impedance. Most sensor data sheets provide the Thevenin model of the sensor from which the value of the series impedance can be easily calculated.



Specifications

Parameter	Calculated	Simulated	Measured
Transient ADC Input Settling Error	< 0.5LSB < 100.5µV	36.24µV	N/A
Step Input Full Scale Range	3.15V	3.15V	3.14978
Input Source Impedance (R_{TH})	10kΩ	10kΩ	10.01kΩ
Filter Capacitor Value (C_{FLT})	680pF	680pF	N/A
ADC Sampling Speed	10ksps	10ksps	10ksps

Design Note

1. Determine source impedance of input signal. Calculate the RC time constant of the input source impedance and filter capacitor (known value).
2. Determine the minimum acquisition time required for the input signal to settle for a given source impedance and the filter capacitor combination.
3. Select COG capacitors to minimize distortion.
4. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.

Component Selection for ADC Input Settling

SAR ADCs can be directly interfaced with sensors when the analog input source is capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal to within ½ of an LSB within the acquisition time of the SAR ADC. To achieve this, the external RC filter (R_{TH} and C_{FLT}) must settle within the acquisition time (t_{ACQ}) of the ADC. The relationship between the ADC acquisition time and RC time constant of the external filter is:

$$t_{ACQ} \geq k \times \tau_{FLT}$$

where

- $\tau_{FLT} = R_{TH} \times C_{FLT}$
- k is the single pole time constant for N bit ADC

The following design example values are given in the table on page 1:

$$R_{TH} = 10k\Omega$$

$$C_{FLT} = 680pF$$

K = 11 (Single pole time constant multiplier for 14-bit ADC) – More information is found on pages 96 and 97 of the *Analog Engineer's Pocket Reference Guide* e-Book.

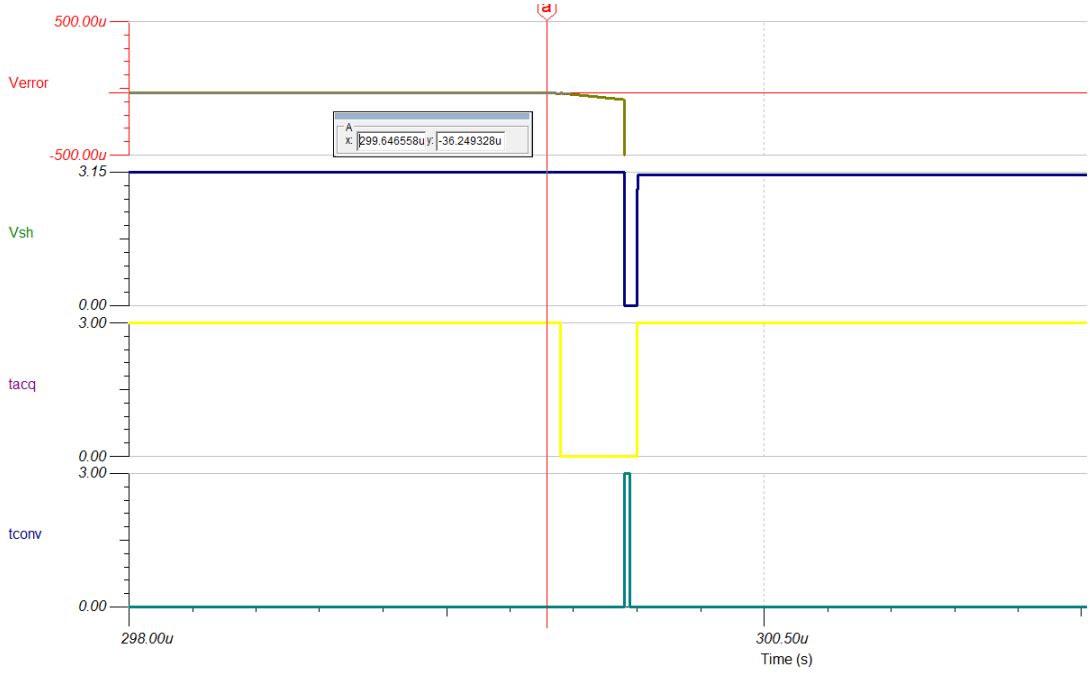
Minimum acquisition time required for proper settling is calculated using this equation:

$$t_{ACQ} \geq 11 \times 10k\Omega \times 680pF = 74.80\mu s$$

For more information on SAR ADCs and front end design for SAR ADCs, refer to the*Introduction to SAR ADC Front-End Component Selection* video.

Transient Input Settling Simulation using TI-TINA

The following figure shows the settling of an *ADS7056* ADC given a 3.15-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* in the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Increasing Acquisition Time of SAR ADC for Input Signal Settling

The acquisition time of a SAR ADC can be increased by reducing the throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput.
2. Keeping the SCLK fixed at the highest permissible value and increasing the CS high time.

The following table lists the acquisition time for the previous two cases for the *ADS7056* SAR ADC operating at 10ksps throughput (tcycle = 100µs). Case 2 provides a longer acquisition time for the input signal to settle because of the increased frequency of the SCLK given a fixed conversion and cycle time.

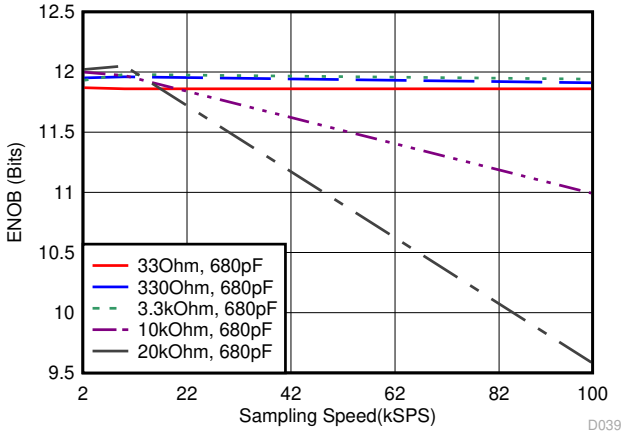
Case	SCLK	t_{cycle}	Conversion Time (18 × t_{SCLK})	Acquisition Time (t_{cycle} – t_{conv})
1	0.24MHz	100µs	74.988µs	25.01µs
2	60MHz	100µs	0.3µs	99.70µs

The following table shows a performance comparison between an 8-, 10-, 12-, and 14-bit ADC with respect to sampling speed and effective number of bits (ENOB) when a sensor output with an output impedance of 10kΩ is directly interfaced with the ADC input. As expected, the ENOB degrades with higher sampling rates because the acquisition time decreases.

Sampling Speed (ksps)	ADS7040 (8-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7041 (10-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7042 (12-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7056 (14-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 680pF)
10	7.93	9.87	10	12.05
100	7.92	9.85	9.97	10.99
500	7.88	9.68	9.95	8.00

Performance Achieved at Different Throughput Rates with Different Source Impedance

The following figure provides the ENOB achieved from the ADS7056 at different throughout with different input impedances. Note that all the results for the following graph were taken with a 100-Hz analog input signal and without an ADC driver amplifier.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7040	8-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	Ultra-low-power, ultra-small-size SAR ADC, 8-bit, 1MSPS, single ended	Analog-to-digital converters (ADCs)
ADS7041	10-bit resolution, SPI, 1Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	Ultra-low power and ultra-small size SAR ADC, 10-bit, 1 MSPS, single ended	
ADS7042	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	12-Bit, 1MSPS, Ultra-Low-Power, Ultra-Small-Size SAR ADC With SPI	
ADS7056	14-bit resolution, SPI, 2.5-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	14-bit 2.5-MSPS ultra-low-power ultra-small-size SAR ADC with SPI	

Note

The ADS7042 and ADS7056 use the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

Link to Key file

Texas Instruments, source files for SBAA256, SBAC178 support files

Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (January 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to Data Converters and added link to circuit cookbook landing page.	1

Analog Engineer's Circuit

Low-Power Sensor Measurements: 3.3V, 1Ksps, 12-Bit, Single-Ended, Dual-Supply Circuit

Reed Kaczmarek

Design Goals

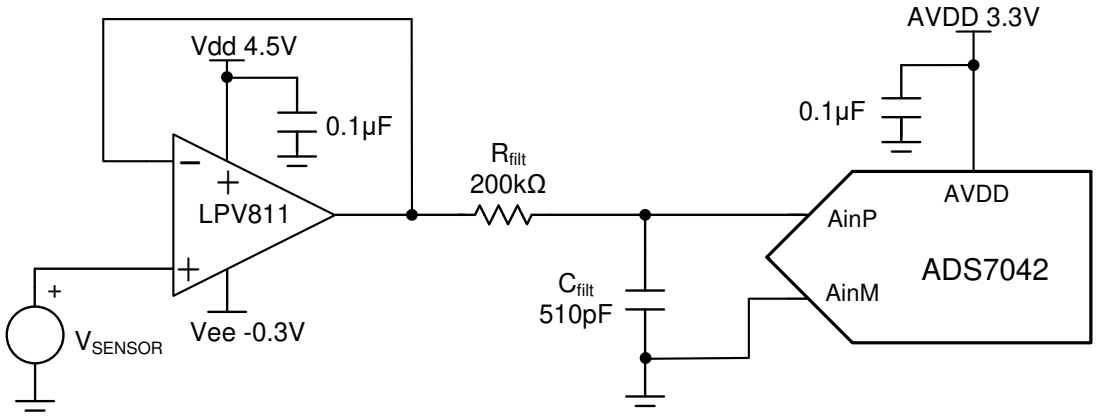
Input	ADC Input	Digital Output ADS7042
V_{inMin} = 0V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
V_{inMax} = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supply

AVDD	V_{ee}	V_{dd}
3.3V	–0.3V	4.5V

Design Description

This design shows an low-power amplifier being used to drive a SAR ADC that consumes only nW of power during operation. This design is intended for systems collecting sensor data and require a low-power signal chain which only burns single-digit µW of power. *PIR sensors*, *gas sensors*, and *blood glucose monitors* are a few examples of power-sensitive systems that benefit from this SAR ADC design. The values in the component selection section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Single Supply* shows a simplified version of this circuit where the negative supply is grounded. The –0.3-V negative supply in this example is used to achieve the best possible linear input signal range. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling (1ksps)	< 0.5 × LSB = 402µV	41.6µV	N/A
AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025µW	N/A	1.942µW
AVDD + VDD System Power (1ksps)	2.784µW	N/A	2.651µW

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the component selection section.
2. Select a COG (NPO) capacitor for Cfilt to minimize distortion.
3. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt (see *Introduction to SAR ADC Front-End Component Selection*). These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. Modifying the design requires selection of a different RC filter.

Component Selection

1. Select a low-power op amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (five times the sampling rate)
   - Unity gain stable
   - LPV811 – 450-nA supply current, 8-kHz gain bandwidth product, unity gain stable
2. Find op amp maximum and minimum output for linear operation:

$$V_{ee} + 0\ V < V_{out} < V_{dd} - 0.9\ V \quad \text{from} \quad \text{LPV811} \quad V_{cm} \quad \text{specification}$$

$$V_{ee} + 10\ mV < V_{out} < V_{dd} - 10\ mV \quad \text{from} \quad \text{LPV811} \quad \text{Vout} \quad \text{swing} \quad \text{specification}$$

$$V_{ee} + 0.3\ V < V_{out} < V_{dd} - 0.3\ V \quad \text{from} \quad \text{LPV811} \quad \text{Aol} \quad \text{linear} \quad \text{region} \quad \text{specification}$$

3. Typical power calculations (at 1ksps) with expected values. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design:

$$P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 230\ nA \times 3.3\ V = 759\ nW$$

$$P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 450\ nA \times [4.5\ V - (-0.3\ V)] = 2.16\ \mu W$$

$$P_{total} = P_{AVDD} + P_{LPV811} = 759\ nW + 2.16\ \mu W = 2.919\ \mu W$$

4. Typical power calculations (at 1ksps) with measured values:

$$P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 214.8\ nA \times 3.3\ V = 708.8\ nW$$

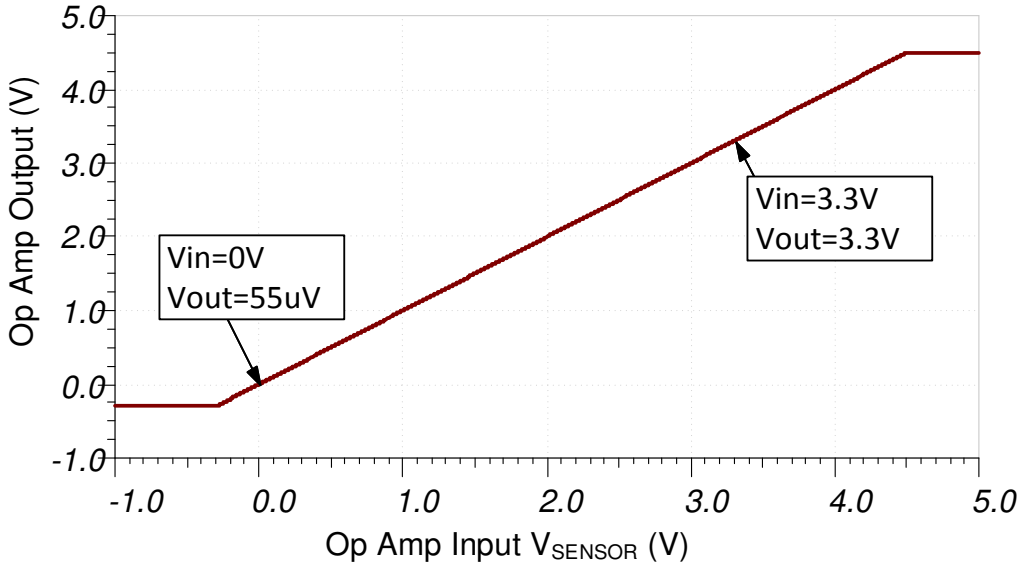
$$P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 431.6\ nA \times [4.5\ V - (-0.3\ V)] = 2.071\ \mu W$$

$$P_{total} = P_{AVDD} + P_{LPV811} = 708.8\ nW + 2.071\ \mu W = 2.780\ \mu W$$

5. Find Rfilt and Cfilt to allow for settling at 1ksps. Refer to *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) for the algorithm to select Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

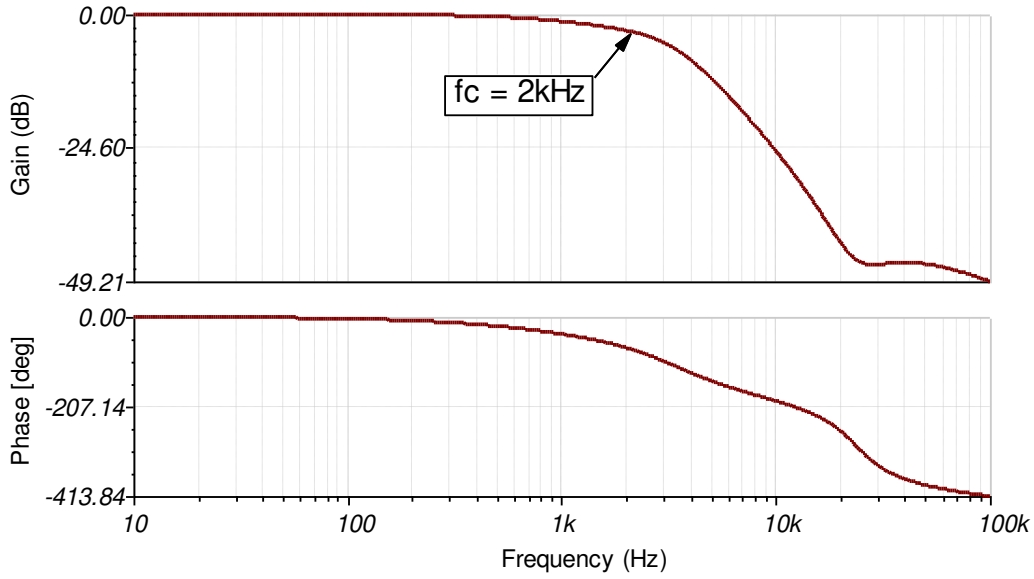
The following graph shows a linear output response for inputs from 0 to 3.3V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



AC Transfer Characteristics

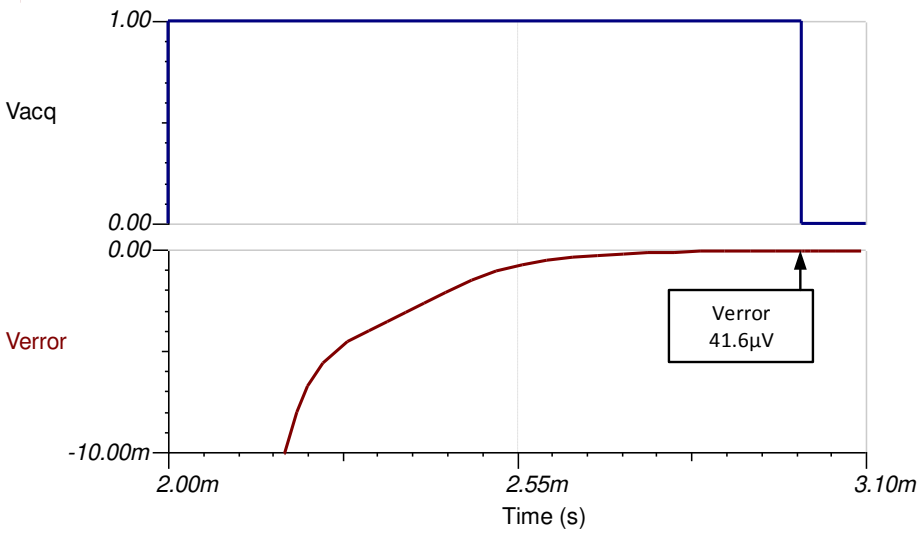
The bandwidth simulation includes the effects of the amplifier output impedance and the RC charge bucket circuit (R_{filt} and C_{filt}).The bandwidth of the RC circuit is shown in the following equation as 1.56kHz. The simulated bandwidth of 2 kHz includes effects from the output impedance interacting with the impedance of the load. See *TI Precision Labs - Op Amps: Bandwidth 1* for more details on this subject.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times (200\ k\Omega) \times (510\ pF)} = 1.56\ kHz$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of an LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



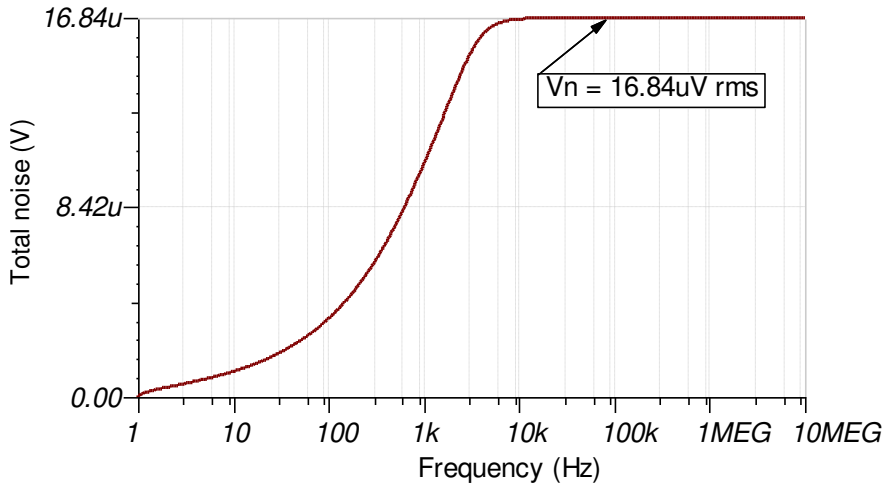
Noise Simulation

This section walks through a simplified noise calculation for a rough estimate. The resistor noise in this calculation is neglected because it is attenuated for frequencies greater than 10 kHz.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times 200\ k\Omega \times 510\ pF} = 1560\ Hz$$

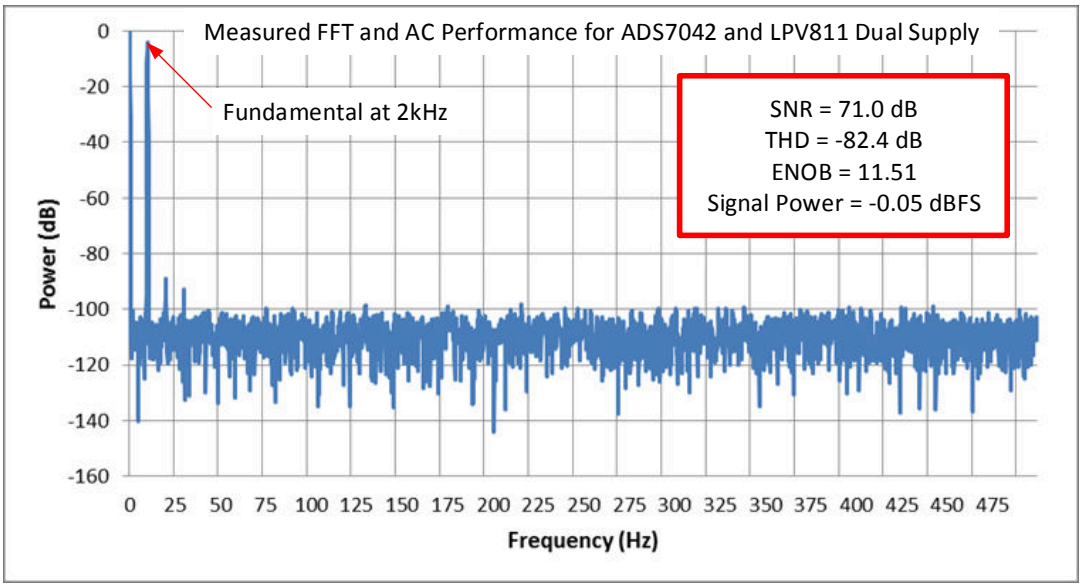
$$E_n = e_{n811} \times \sqrt{K_n \times f_c} = \frac{340\ nV}{\sqrt{Hz}} \times \sqrt{1.57 \times 1560\ Hz} = 16.8\ \mu V$$

Note that the calculated and simulated values match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM with a 10-Hz input sine wave. The AC performance indicates SNR = 71.0dB, THD = –82.4dB, and ENOB (effective number of bits) = 11.51, which matches well with the specified performance of the ADC, SNR = 70dB and THD = –80dB. This test was performed at room temperature. See *Introduction to Frequency Domain* for more details on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7042 (1)	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD reference input range 1.6V to 3.6V.	12-Bit 1MSPS Ultra-Low-Power Ultra-Small-Size SAR ADC With SPI Interface	Analog-to-digital converters (ADCs)
LPV811 (2)	8-kHz bandwidth, rail-to-rail output, 450-nA supply current, unity gain stable	Single Channel 450nA Precision Nanopower Operational Amplifier	Operational amplifiers (op amps)

(1) The ADS7042 uses the AVDD as the reference input. Use a high-PSRR LDO, such as the TPS7A47, as the power supply.
(2) The LPV811 is also commonly used in low-speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across the entire ADC input range.

Link to Key Files (TINA)

Texas Instruments, SBAM342 circuit, design files

Revision History

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Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

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• Downstyle the title and changed title role to 'Data Converters'	1
• Added link to circuit cookbook landing page	1

Trademarks

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Analog Engineer's Circuit

Low-Power Sensor Measurements: 3.3V, 1kSPS, 12-Bit, Single-Ended, Single-Supply Circuit

Reed Kaczmarek

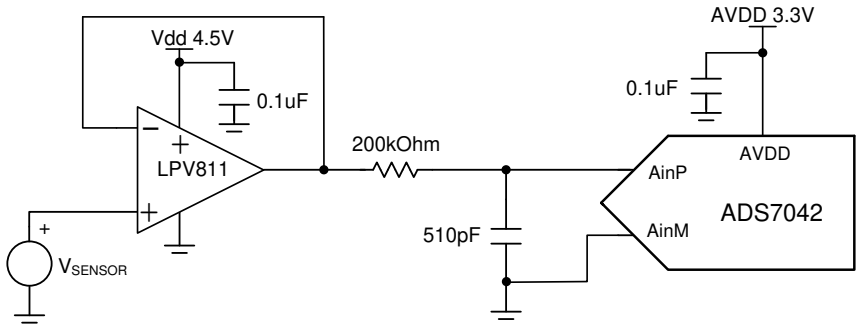
Input	ADC Input	Digital Output ADS7042
VinMin = 0V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
VinMax = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supplies

AVDD	Vee	Vdd
3.3V	0V	4.5V

Design Description

This design shows an ultra-low power amplifier being used to drive a SAR ADC that consumes only nanoWatts of power during operation. This design is intended for collecting sensor data by providing overall system-level power consumption on the order of single-digit microWatts. *PIR sensors, gas sensors,* and *glucose monitors* are a few examples of possible implementations of this SAR ADC design. The values in the *component selection* section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows a more sophisticated version of this circuit where the negative supply is connected to a small negative voltage (–0.3V). The single-supply version has degraded performance when the amplifier output is near zero volts. However, in most cases the single-supply configuration is preferred for its simplicity.



Specifications

Specification	Calculated	Simulated	Measured
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AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025µW	N/A	1.942µW
AVDD + VDD System Power (1ksps)	2.784µW	N/A	2.651µW

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the *component selection* section.
2. Select COG capacitors to minimize distortion.
3. Use 0.1% 20ppm/°C film resistors or better to minimize distortion.
4. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here give good settling and AC performance for the amplifier and data converter in this example. If you modify this design you need to select a different RC filter. Refer to the *Introduction to SAR ADC Front-End Component Selection* training video for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select a low-power operational amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (5 times the sampling rate)
   - Unity gain stable
   - For this cookbook, the LPV811 was selected. It has a 450-nA supply current, 8-kHz gain bandwidth product, and is unity gain stable.
2. Find op amp maximum and minimum output for linear operation

$$V_{ee} + 0V < V_{out} < V_{dd} - 0.9V \quad \text{from LPV811 Vcm specification}$$

$$V_{ee} + 10mV < V_{out} < V_{dd} - 10mV \quad \text{from LPV811 Vout swing specification}$$

$$V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V \quad \text{from LPV811 Aol linear region specification}$$

$$0.3V < V_{in} < 3.4V \quad \text{Combined worst case}$$

Note

The linear range of the LPV811 is 300mV above ground. This means to design a system to establish a full linear range from 0V to 3.3V (full-scale range (FSR) of ADS7042), then a negative supply is required. This design shows that full-measured SNR and THD specifications of the ADS7042 are met without using a negative supply voltage. This testing was only at room temperature and for a more robust system; *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows this design using a negative supply instead of ground.

3. Typical power calculations (at 1ksps) with expected values:

$$P_{AVDD} = I_{AVDD\_Avg} \times AVDD = 230nA \times 3.3V = 759nW$$

$$P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 450nA \times (4.5V - 0V) = 2.025\mu W$$

$$P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.025\mu W = 2.794\mu W$$

4. Typical power calculations (at 1ksps) with measured values:

$$P_{AVDD} = I_{AVDD\_Avg} \times AVDD = 214nA \times 3.3V = 709nW$$

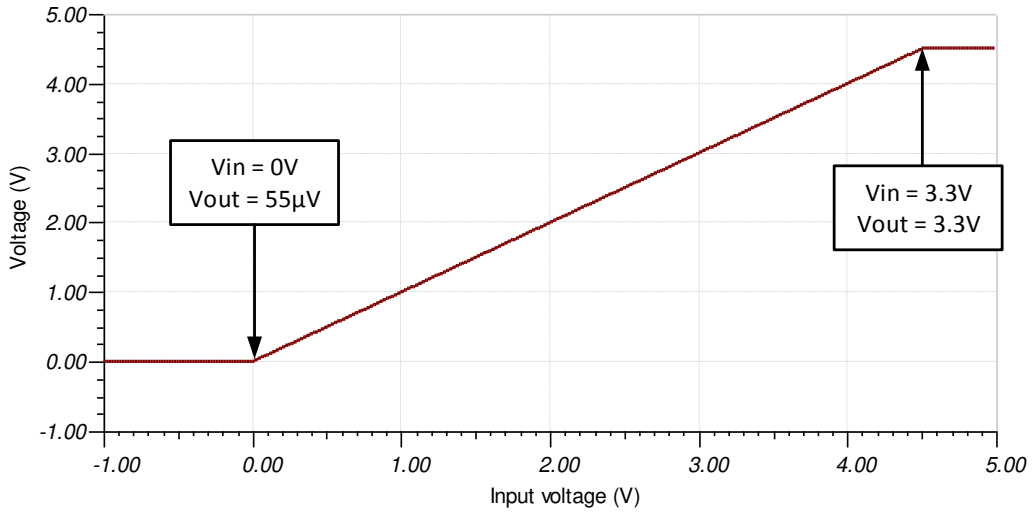
$$P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 431.6nA \times (4.5V - 0V) = 1.942\mu W$$

$$P_{total} = P_{AVDD} + P_{LPV811} = 709nW + 1.942\mu W = 2.651\mu W$$

5. Find Rfilt and Cfilt to allow for settling at 1ksps. *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) showing the algorithm for selecting Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

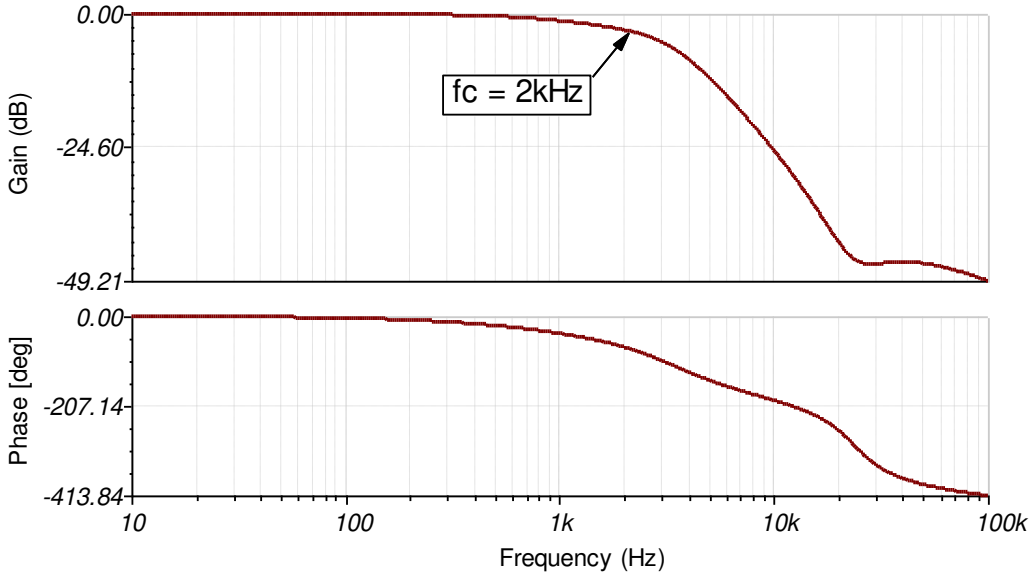
The following graph shows a linear output response for inputs from 0 to 3.3V. The FSR of the ADC falls within the linear range of the op amp.



AC Transfer Characteristics

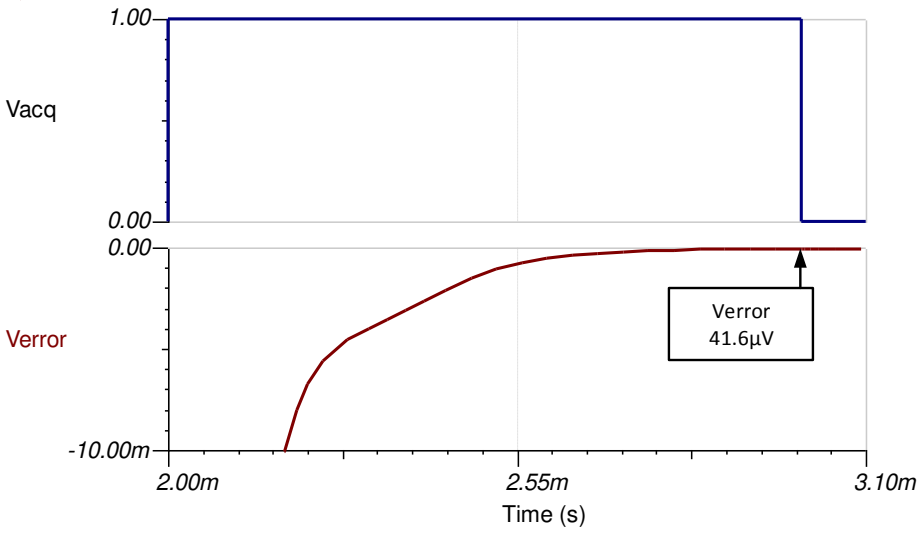
The bandwidth simulation includes the effects of the amplifier output impedance and the RC charge bucket circuit (R_{filt} and C_{filt}).The bandwidth of the RC circuit is shown in the following equation to be 1.56kHz. The simulated bandwidth of 2kHz includes effects from the output impedance interacting with the impedance of the load. See *TI Video Library - Op Amps: Bandwidth 1* for more details on this subject.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (200k\Omega) \cdot (510pF)} = 1.56kHz$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



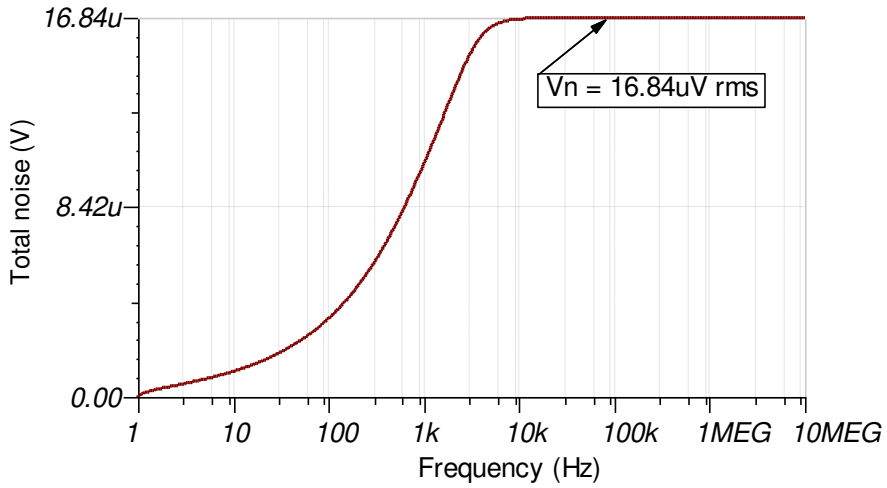
Noise Simulation

This section details a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (200k\Omega) \cdot (510pF)} = 1560.3Hz$$

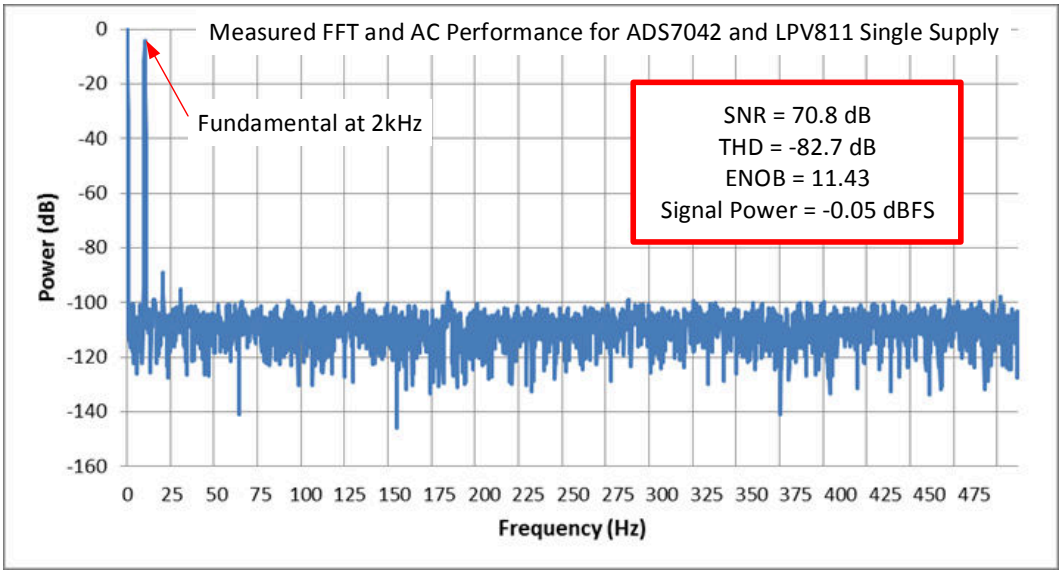
$$E_n = e_{n811} \times \sqrt{2 \times K_n \times f_c} = \left(340nV/\sqrt{Hz}\right) \times \sqrt{1.57 \times (1560Hz)} = 16.8\mu V$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FET

This performance was measured on a modified version of the ADS7042EVM-PDK. The AC performance indicates SNR = 70.8dB, THD = –82.7dB, and ENOB (effective number of bits) = 11.43, which matches well with the specified performance of the ADC of SNR = 70dB.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7042 (1)	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD, Vref input range 1.6V to 3.6V.	12-Bit 1MSPS Ultra-Low-Power Ultra-Small-Size SAR ADC With SPI	ADCS
LPV811 (2)	8kHz bandwidth, Rail-to-Rail output, 450nA supply current, unity gain stable	Single Channel 450nA Precision Nanopower Operational Amplifier	Op amp

(1) The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, can be used as the power supply.
(2) The LPV811 is also commonly used in low speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across all of the ADC input range.

Link to Key Files

Texas Instruments, LPV811 TINA files, software download

Revision History

Changes from Revision A (March 2019) to Revision B (September 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision * (February 2018) to Revision A (March 2019) **Page**

- Changed *AC Transfer Characteristic* section to improve bandwidth confusion and to be more in line with Low-power sensor measurements: 3.3-V, 1-ksps, 12-bit single-ended, dual-supply circuit..... 1
- Changed the title to Data Converters. Added link to circuit cookbook landing page..... 1

Trademarks

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Analog Engineer's Circuit

Circuit for Driving a High-Voltage SAR With an Instrumentation Amplifier

Art Kay

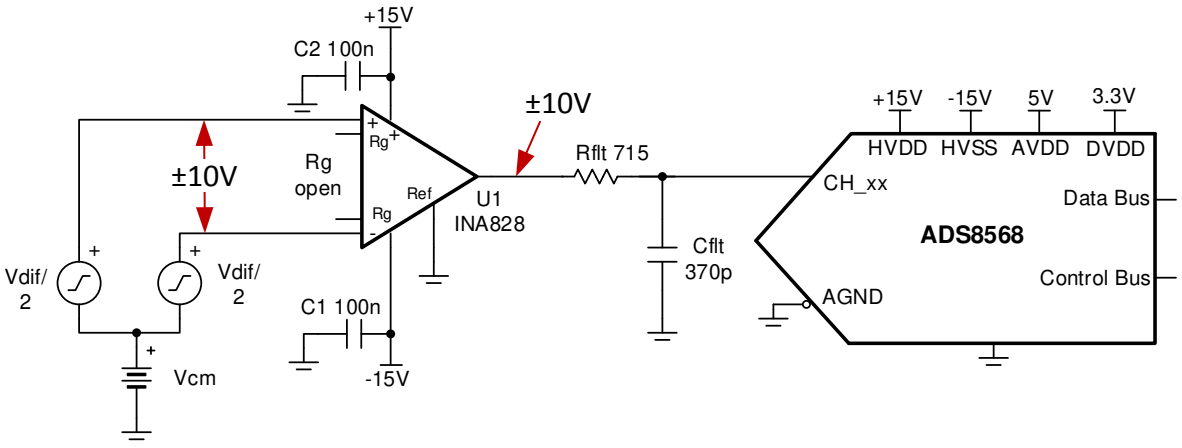
Input	ADC Input	Digital Output ADS7042
–10V	–10V	8000H
+10V	+10V	7FFFH

Power Supplies

AVDD	DVDD	V_{ref}	V_{cc}	V_{ee}
5.0V	3.0V	5.0V	+15V	–15V

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy. The INA828 instrumentation amplifier preforms a differential to single-ended conversion for a ±10-V range. The INA828 has excellent DC performance (that is, offset, drift), as well as good bandwidth. The ADS8568 is ideally suited to work with the INA828 as the ADC can be configured for a ±10-V single-ended input. To achieve the best settling, limit the sampling rate to 200kSPS or lower. For higher sampling rates see *Driving High-Voltage SAR ADC with a Buffered Instrumentation Amplifier*. Also, this design example uses unity gain (G=1) to translate a ±10-V differential input signal to a ±10-V single-ended output. For smaller input signals or higher gains, see *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain*. This circuit implementation is applicable to *Industrial Transportation* and *Analog Input Modules* that require precision signal-processing and data-conversion.



Specifications

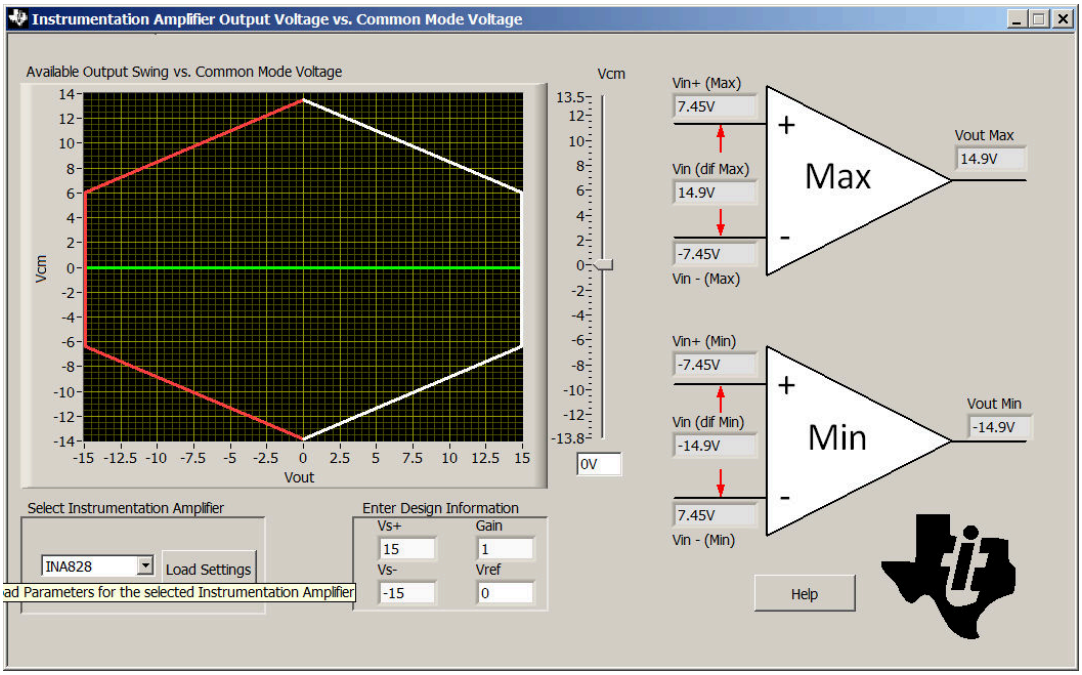
Specification	Goal	Calculated	Simulated
Transient Settling Error	< 1/2 LSB (±152µV)	NA	–105µV
Noise	< 20µV	103µV	86.6µV

Design Notes

1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at higher data rate. In this example, the sampling rate is reduced from 510kSPS to 200kSPS to achieve good settling. For full sampling rate see *Driving High-Voltage SAR ADC with a Buffered Instrumentation Amplifier*.
2. Check the common mode and output range of the instrumentation amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
3. Use a COG type capacitor for C_{filt} to minimize distortion.
4. The *Precision Labs* video series covers methods for selecting the charge bucket circuit C_{flt} and R_{flt}. See the *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

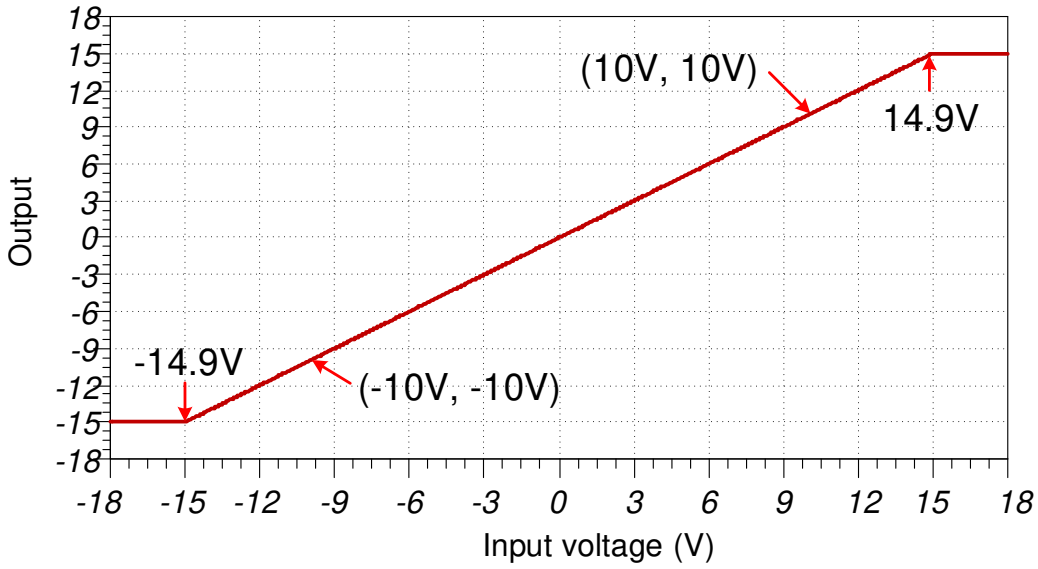
1. The ADS8568 can accept a ±10-V single-ended input signal. The INA828 is used to translate a ±10-V differential signal to a ±10-V single-ended signal. So the INA828 is in unity gain for this example, and no external gain set resistor R_g is needed. See *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain* in cases where the input signal range is small and gain is required.
2. The INA826 reference voltage (V_{ref}) input is used to shift asymmetrical input ranges to match the input range of the ADC. In this case the input range is symmetrical so the V_{ref} pin is grounded (V_{ref} = 0V). See *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain* for an example where the V_{ref} pin is used to adjust asymmetrical input signals.
3. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA828 is violating the common-mode range. The common-mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common mode input.



4. Find the value for C_{filt}, and R_{filt} using TINA SPICE and the methods described in *Introduction to SAR ADC Front-End Component Selection*. The value of R_{filt} and C_{filt} shown in this document will work for these circuits; however, if you use different amplifiers you will have to use TINA SPICE to find new values.

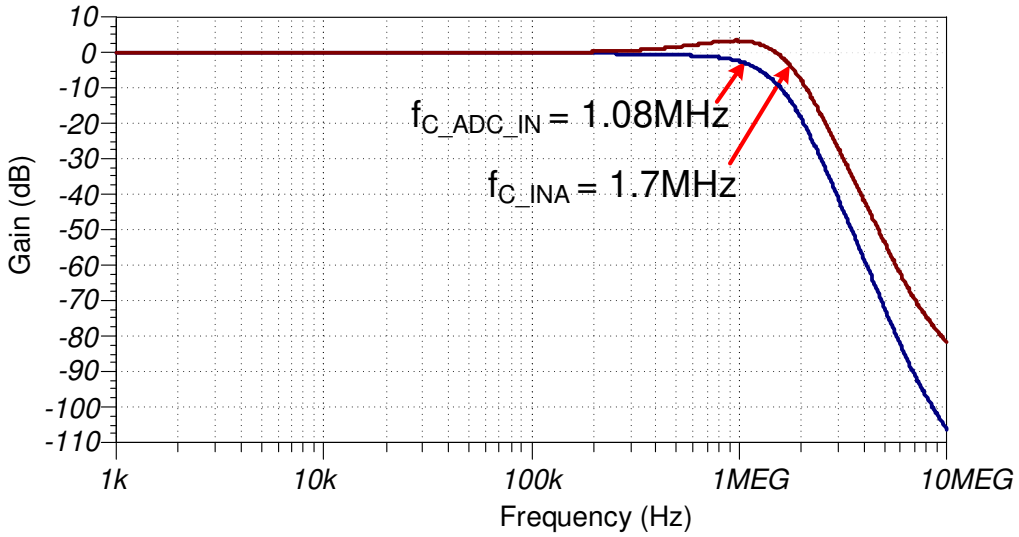
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –14.9V to +14.9V. The input range of the ADC is ±10V, so the amplifiers are linear well beyond the required range. See *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the instrumentation amplifier.



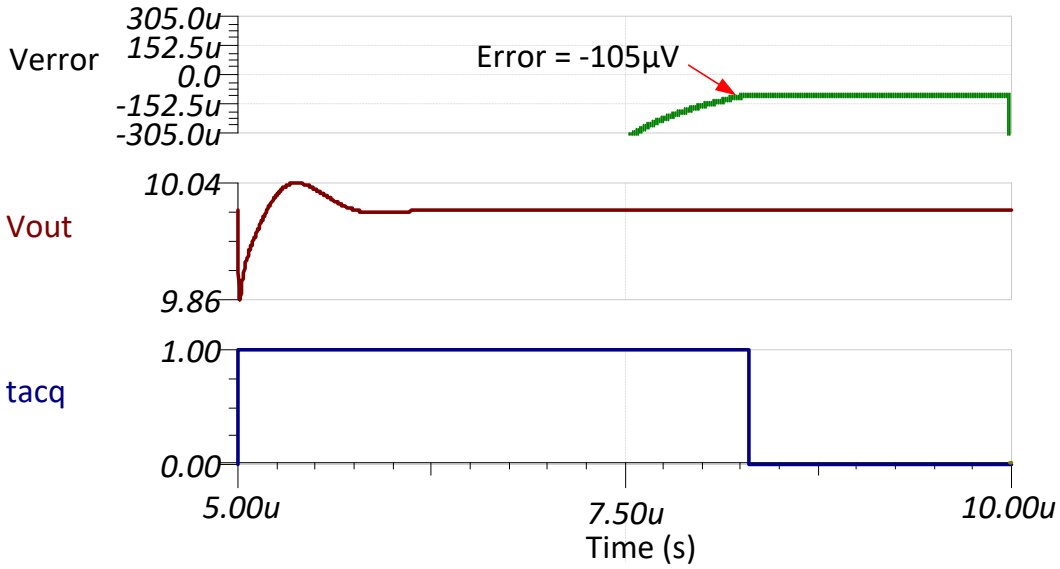
AC Transfer Characteristics

The bandwidth for this circuit is simulated to be 446.75kHz and the gain is 0dB.



Transient ADC Input Settling Simulation (200kSPS)

The following simulation shows settling to a 10-V DC input signal with INA828 and ADS8568. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV) at 200kSPS sampling rate on ADS8568. See the *ADC Front End Component Selection* video series for detailed theory on this subject.



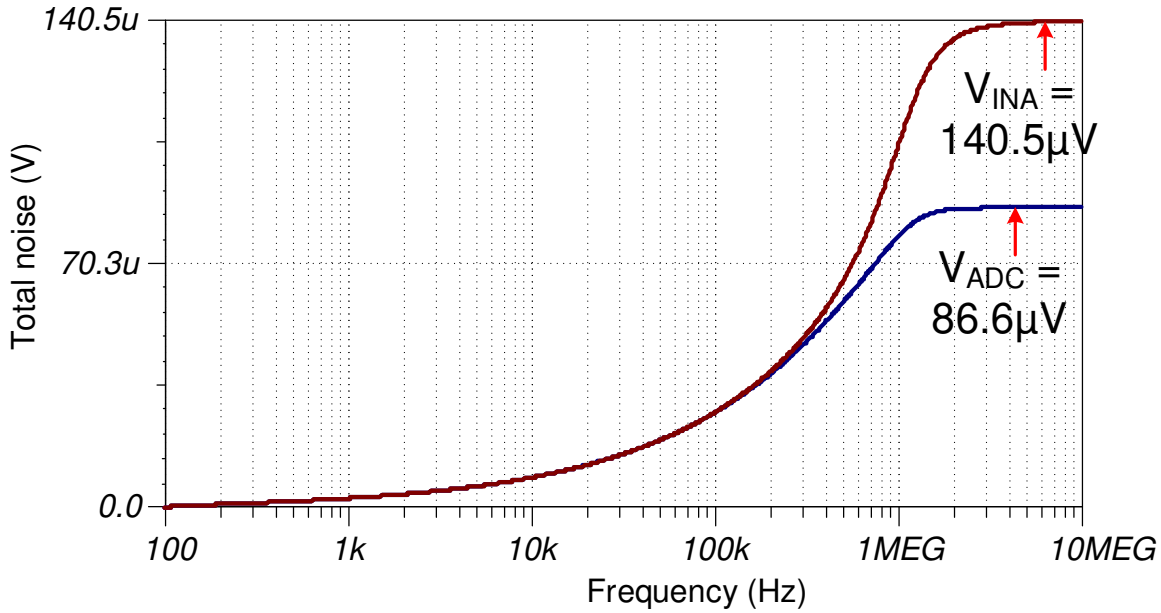
Noise

This section shows a simplified noise calculation for a rough estimate. The bandwidth estimate was taken from the TINA simulation, and the noise density values are from the *INA828 50-µV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier* data sheet. The Kn factor of 1.22 is used because the filter is second order (the INA and output filter both have a pole).

$$E_{n-ADC} \quad Gain \cdot \sqrt{e_{ni}^2 + \left(\frac{e_{no}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_{n-ADC} \quad 1 \cdot \sqrt{\left(7\,nV/\sqrt{Hz}\right)^2 + \left(\frac{90\,nV/\sqrt{Hz}}{1}\right)^2} \cdot \sqrt{1.22 \cdot 1.08MHz} \quad 103\,\mu Vrms$$

Note that simulated and calculated are close but not exact (simulated = 86.6µV, calculated = 103µV). The difference is because the INA has gain peaking and the filter order is approximated as two but in reality the INA and filter poles are not exactly aligned.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8860	16-bit resolution, SPI, 1MSPS sample rate, single-ended input, Vref input range 2.5V to 5.0V	16-bit, 1-MSPS, 1-channel SAR ADC with single-ended input, SPI and daisy chain	Precision ADCs
INA826	Bandwidth 1MHz (G=1), low noise 18nV/√ Hz, low offset ±40µV, low offset drift ±0.4µV/°C, low gain drift 0.1ppm/°C. (Typical values)	Precision, 200-µA Supply Current, 36-V Supply Instrumentation Amplifier	Instrumentation Amplifiers

Link to Key Files

Texas Instruments, Source Files for SBAA999, support software

Trademarks

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Analog Engineer's Circuit

Circuit for Driving High-Voltage SAR ADC With a Buffered Instrumentation Amplifier

Dale Li

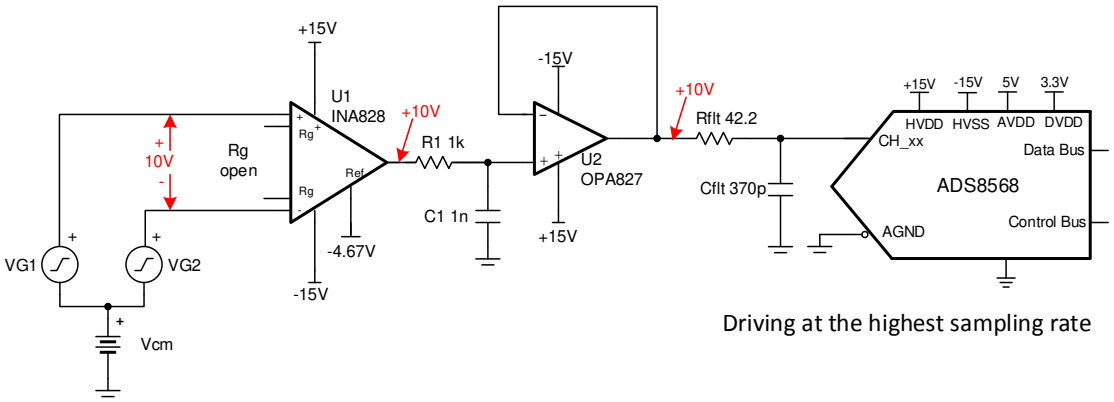
Input	ADC Input	Digital Output ADS7042
VinDiffMin = –10V	CH_x = –10V	8000H
VinDiffMax = +10V	CH_x = +10V	7FFFH

Power Supplies

AVDD	DVDD	HVDD (V_{CC})	HVSS(V_{EE})
5.0V	3.3V	+15V	–15V

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy but these instrument amplifiers may not be able to drive a precision ADC to settle the signal properly during the acquisition time of ADC. This design will show how a wide bandwidth buffer (OPA827) can be used with an instrumentation amplifier to achieve good settling at higher sampling rate. This INA828 instrumentation amplifier with the buffer drives the ADS8568 SAR ADC to implement data capture for a high voltage fully differential signal which may have a wide common-mode voltage range or a bipolar single-ended signal up to ±10V. A related cookbook circuit shows a simplified approach that does not include the wide bandwidth buffer (*Driving High Voltage SAR ADC with an Instrumentation Amplifier*), this simplified approach has limited sampling rate as compared to the buffered design in this document. This circuit implementation is applicable to *industrial transportation* and *analog input modules* that require Precision Signal-Processing and Data-Conversion.



Driving at the highest sampling rate

Specifications

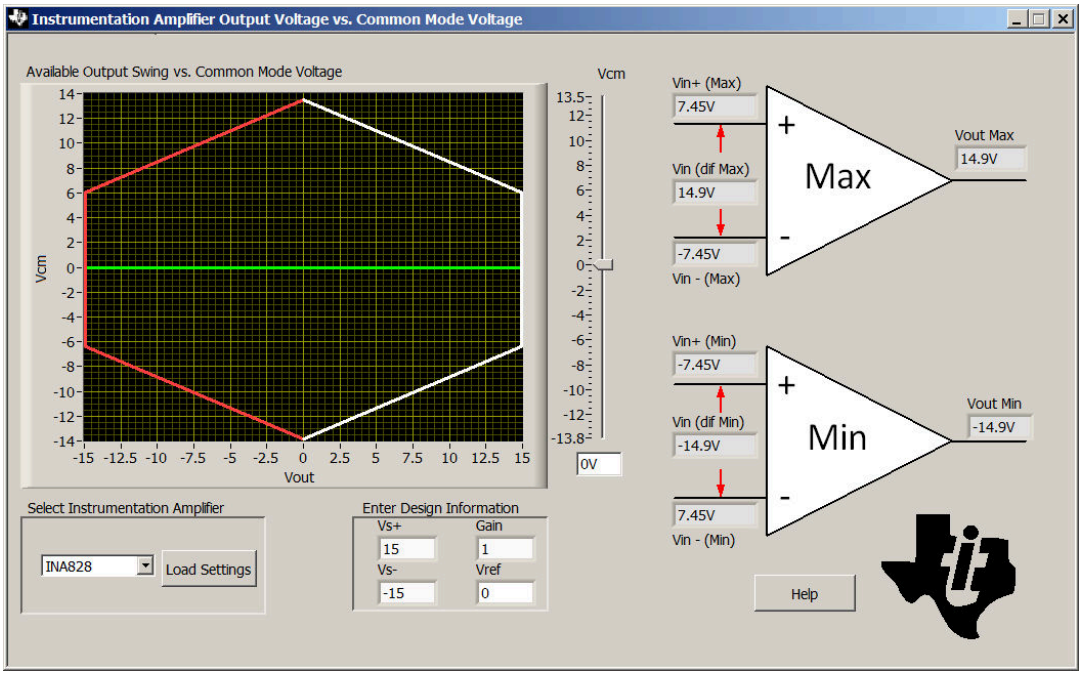
Specification	Goal	Calculated	Simulated
Transient Settling Error	< 1/2LSB (< 152µV)	NA	–346nV
Noise (at ADC Input)	<20μV_{RMS}	47.2μV_{RMS}	46μV_{RMS}

Design Notes

1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at higher data rate, so a wide bandwidth driver is needed because the SAR ADC with switched-capacitor input structure has an input capacitor that needs to be fully charged during each acquisition time. The OPA827 buffer is added to allow the ADC to run at full sampling rate (ADS8568 510kSPS for parallel interface).
2. The ADS8568 can accept a ±10-V single-ended input signal. The INA828 is used to translate a ±10-V differential signal to a ±10-V single-ended signal. So the INA282 is in unity gain for this example, and no external gain set resistor Rg is needed. Refer to *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain* in cases where the input signal range is small and gain is required.
3. Check the common mode range of the amplifier using the *analog engineer's calculator.*
4. Select COG capacitors for C_1 and C_{filt} to minimize distortion.
5. Precision labs video series covers the method for selecting driver amplifier and the charge bucket circuit R_{filt} and C_{filt}. For details, see the *Selecting and Verifying the Driver Amplifier* and *Introduction of SAR ADC Front-End Component Selection* videos.
6. Set the cutoff of the filter between the op amp and instrumentation amplifier for anti aliasing and to minimize noise. See *Aliasing and Anti-aliasing Filters* for more details on aliasing and anti-aliasing filters.

Component Selection

1. Find the gain based on differential input signal and ADC full-scale input range. The input signal in this design is ±10V high voltage signal, so the Gain of INA828 should be set to 1 and no gain resistor (Rg) is needed.
2. Use the *analog engineer's calculator* to determine if the INA828 is violating the common mode range. The common mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common-mode input.

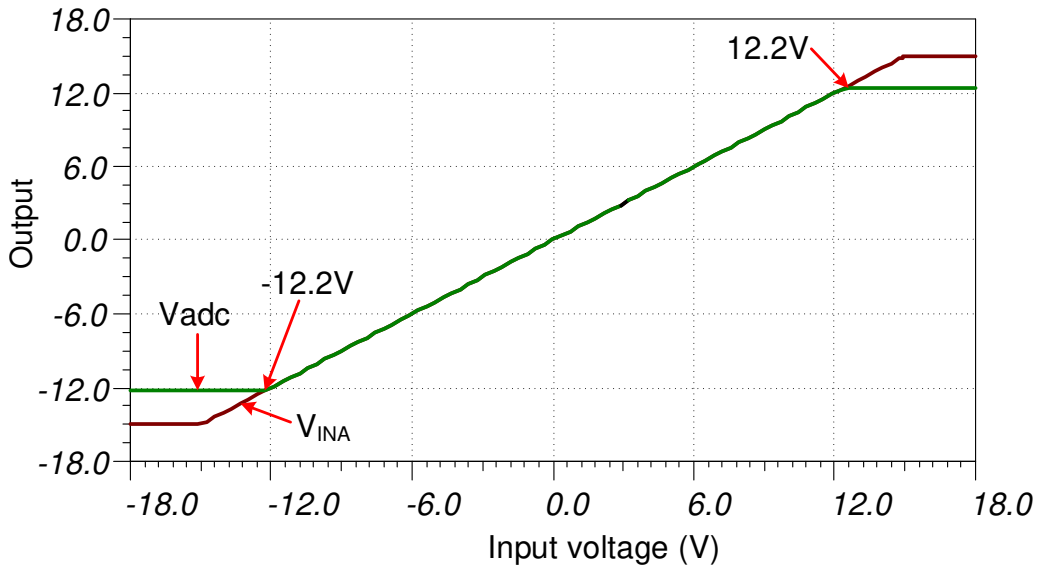


3. Find the value for C_{filt}, and R_{filt} using *TINA SPICE* and the methods described in *SAR ADC Front-End Component Selection.* The value of R_{filt} and C_{filt} shown in this document will work for these circuits; however, if you use different amplifiers you will have to use TINA SPICE to find new values.
4. Select the RC filter between the INA828 and OPA827 based on your system requirements (f_{cRC} = 15.9kHz in this example). Set the cutoff of this filter for anti aliasing and to minimize noise.

$$f_{cRC} = \frac{1}{2\pi \cdot R_1 \cdot C_1} = \frac{1}{2\pi \cdot (1k\Omega) \cdot (1pF)} = 159\,kHz$$

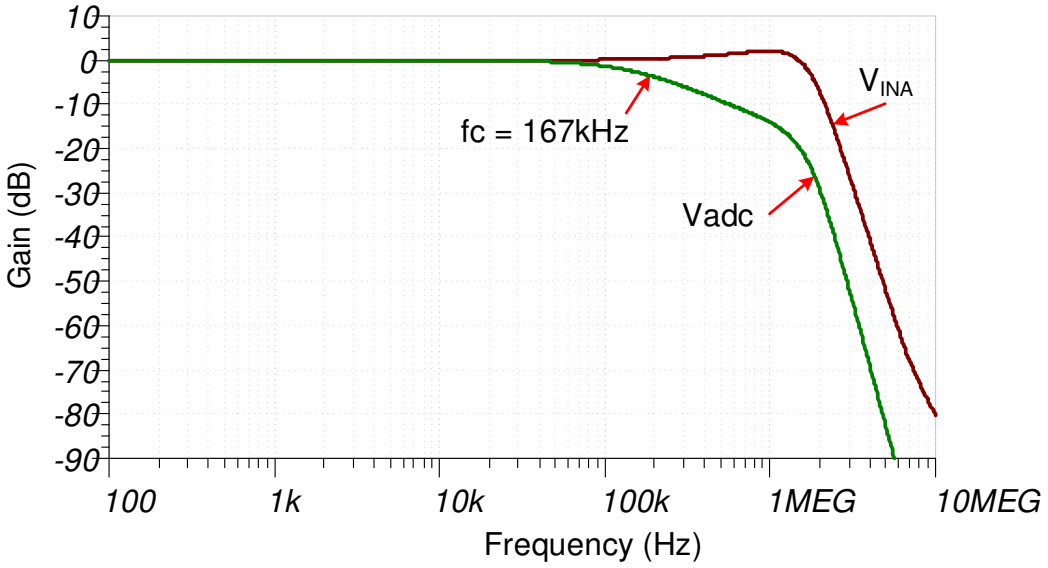
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –12.2V to +12.2V. The input range of the ADC is ±10V, so the amplifiers are linear well beyond the required range. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the Instrumentation Amplifier.



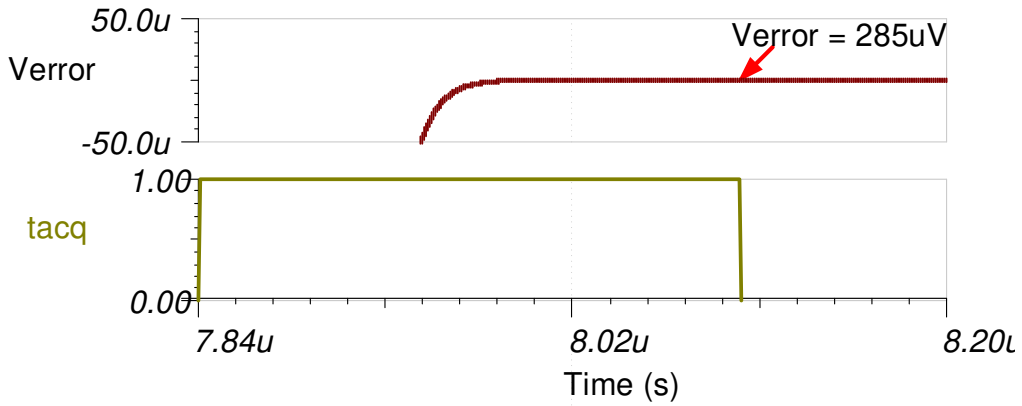
AC Transfer Characteristics

The bandwidth for this system is simulated to be 167kHz and the gain is 0dB. The filter between the OPA827 and INA828 limits the bandwidth to about 167kHz.



Transient ADC Input Settling Simulation (510kSPS)

The OPA827 buffer (22MHz GBW) is used because it is capable of responding to the rapid transients from the charge kickback fromADS8568. The op amp buffer allows the system to achieve the ADS8568 maximum sampling rate of 510kSPS. The following simulation shows settling to a full scale DC input signal with INA828 and OPA827 buffer, and ADS8568.. This type of simulation shows that the sample and hold kickback circuit is properly selected to meet desired ½ of a LSB (152µV). Refer to the *Introduction to SAR ADC Front-End Component Selection* training video series for detailed theory on this subject.



Noise Simulation

The section walks through a simplified noise calculation for a rough estimate. We include both the INA828 and OPA827 noise. Note that the RC filter between the instrumentation amplifier and op amp significantly reduces the total noise. The output filter pole is estimated as a second order filter because the OPA827 (22MHz) bandwidth limit and charge bucket filter cutoff frequency (10.2MHz) is close.

$$E_{n-INA} = G\sqrt{e_{n-in}^{2} + \left(\frac{e_{n-out}}{G}\right)^{2}} \cdot \sqrt{K_n \cdot f_{cRC}}$$

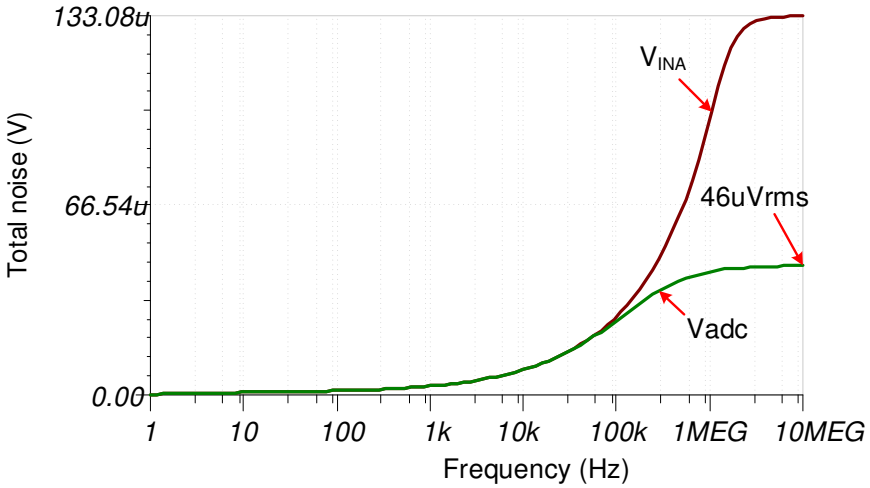
$$E_{n-INA} = 1\sqrt{\left(4nV/\sqrt{Hz}\right)^{2} + \left(\frac{90nV/\sqrt{Hz}}{1}\right)^{2}} \cdot \sqrt{(1.57)\cdot(159kHz)} = 45.1\mu V_{RMS}$$

$$f_{c-adcFilter} = \frac{1}{2\pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2\pi \cdot (42.2\Omega)\cdot(370pF)} = 10.2MHz$$

$$E_{opa} = e_{n-opa}\sqrt{K_n \cdot f_c} = \left(4nV/\sqrt{Hz}\right)\sqrt{(1.22)\cdot(10.2MHz)} = 14.1\mu V_{RMS}$$

$$E_{n-total} = \sqrt{E_{n-INA}^{2} + E_{opa}^{2}} = \sqrt{(45.1\mu V)^{2} + (14.1\mu V)^{2}} = 47.2\mu V_{RMS}$$

Note that calculated and simulated match well- (calculated = 47.2µV, Simulated = 46µV). See *TI Precision Labs* for detailed theory on amplifier noise calculations, and *Calculating Total Noise for ADC Systems* for data converter noise.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8568	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	16-bit, 8-channel, simultaneous-sampling, bipolar-input, SAR analog-to-digital converter (ADC)	Analog-to-digital converters (ADCs)
INA828	Bandwidth 1MHz (G=1), low noise 18nV/rtHz, low offset ±40µV, low offset drift ±0.4µV/°C, low gain drift 0.1ppm/°C (Typical values)	50-µV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	Instrumentation amplifiers
OPA827	Gain bandwidth 22MHz, low noise 4nV/rtHz, low offset ±75µV, low offset drift ±0.1µV/°C (Typical values)	Low-noise, high-precision, JFET-input operational amplifier	Operational amplifiers (op amps)

Links to Key Files

Texas Instruments, sources files for SBAA286, support software

Trademarks

All trademarks are the property of their respective owners.

Application Note

Circuit for driving high-voltage SAR ADCs for high-voltage, true differential signal acquisition

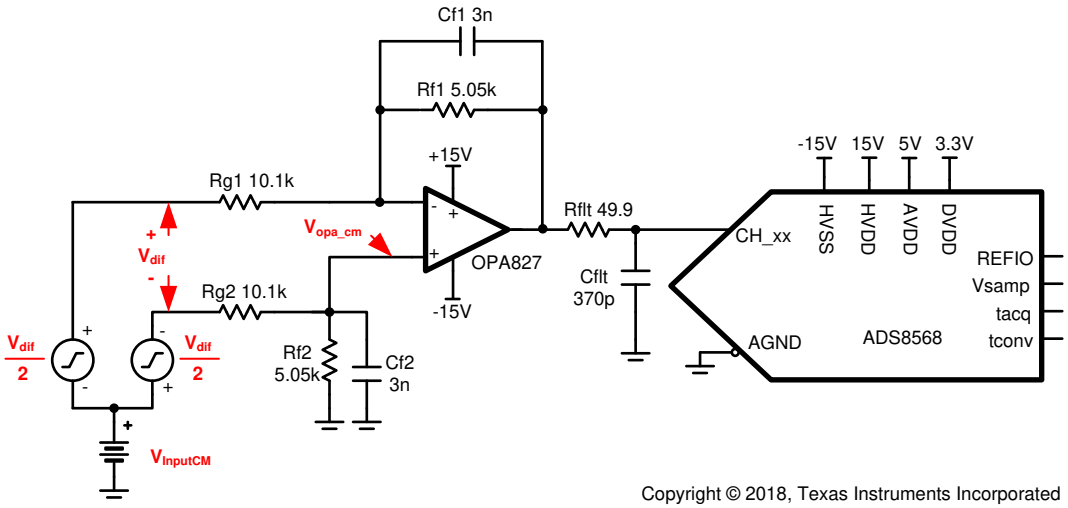
Dale Li

Input	ADC Input	Digital Output ADS7042
VinDiffMin = –20V	CH_x = +10V	$7FFF_H$, or 32767_{10}
VinDiffMax = +20V	CH_x = –10V	8000_H , or 32768_{10}

Power Supplies			
AVDD	**DVDD**	**V_{CC} (HVDD)**	**V_{SS} (HVSS)**
5.0V	3.3V	+15V	–15V

Design Description

This design shows a design to drive high-voltage SAR ADC to implement data capture for high-voltage fully differential signal which can have a wide common-mode voltage range depended on the power supply and input amplitude signal of the amplifier. A general high-voltage precision amplifier performs the differential to single-ended conversion and drives high-voltage SAR ADC single-ended input scale of ±10V at highest throughput. This type of application is popular in end equipment such as: *Multi-Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*. The values in the *component selection* section can be adjusted to allow for different level differential input signal, different ADC data throughput rates, and different bandwidth amplifiers.



Specifications

Specification	OPA827 Calculated	OPA827 Simulated	OPA192 Calculated	OPA192 Simulated
Common Mode Input Range (with Vdif = ±20V)	±26V	±26V	±35V	±35V
Transient ADC Input Settling Error	< 1/2LSB (< 152µV)	0.002 LSB (0.568µV)	< 1/2LSB (< 152µV)	0.006 LSB (1.86µV)
Phase Margin of driver	> 45°	67.1°	> 45°	68.6°

(continued)

Specification	OPA827 Calculated	OPA827 Simulated	OPA192 Calculated	OPA192 Simulated
Noise (at ADC Input)	14.128µVrms	15.88µVrms	5.699µVrms	6.44µVrms

Design Notes

1. Determine the amplifier gain based on the differential input signal level, the ADC's configuration for input range. This is covered in the *component selection* section.
2. Determine amplifier's linear range based on common mode voltage, input swing, and power supplies. This is covered in the *component selection* section.
3. In this design circuit, the common-mode voltage of the input signal can be any value in the range of $V_{InputCM}$. The derivation of this range is provided in the *component selection* section for the OPA827 and OPA192.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion. Review *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
6. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select Rfilt and Cfilt for best settling and AC performance. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. If the design is modified, select a different RC filter.

Component Selection

1. Find the gain based on differential input signal and ADC full-scale input range.

$$Gain_{OPA} = \frac{\pm V_{ADC(range)}}{\pm V_{DifIn(range)}} = \frac{\pm 10V}{\pm 20V} = 0.5V/V$$

2. Find standard resistor values for differential gain. Use the *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$Gain_{OPA} = \frac{R_f}{R_g} = \frac{5.05k\Omega}{10.1k\Omega} = 0.5$$

3. Find the amplifier's maximum and minimum input for linear operation (that is, the common mode range of the amplifier, V_{cm_amp}). For this example, the OPA827 is used.

$$V_- + 3V < V_{cm\_opa} < V_+ - 3V \quad \text{from the OPA827 common mode specification}$$

$$-12V < V_{cm\_opa} < 12V \quad for \quad \pm 15V \quad supplies$$

4. Calculate the maximum common-mode voltage range based on the input range and previously shown configuration of the amplifier. Refer to the schematic diagram on the first page for better understanding of how V_{cm_opa}, $V_{InputCM}$, and V_{dif} relate to the circuit.

$$V_{cm\_opa} = \left(V_{InputCM} \pm \frac{V_{dif}}{2}\right) \cdot \left(\frac{R_f}{R_f + R_g}\right)$$

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

5. Solve the equation for the input common-mode range $V_{InputCM}$ for the amplifier. For this example (OPA827), the common mode input can be ±26V with a ±20-V differential input. Using the same method on OPA192 shows a common mode range of ±35V with a ±20-V differential input. Exceeding this common-mode range distorts the signal. Note that this common-mode range was calculated using ±15-V power supplies. The common mode range can be extended by increasing the supply (maximum ±18V).

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

$$\left(-12V\right)\cdot\left(\frac{5.05k\Omega+10.1k\Omega}{5.05k\Omega}\right)+\frac{20V}{2}<V_{InputCM}<\left(12V\right)\cdot\left(\frac{5.05k\Omega+10.1k\Omega}{5.05k\Omega}\right)-\frac{20V}{2}$$

$$-26V<V_{InputCM}<26V$$

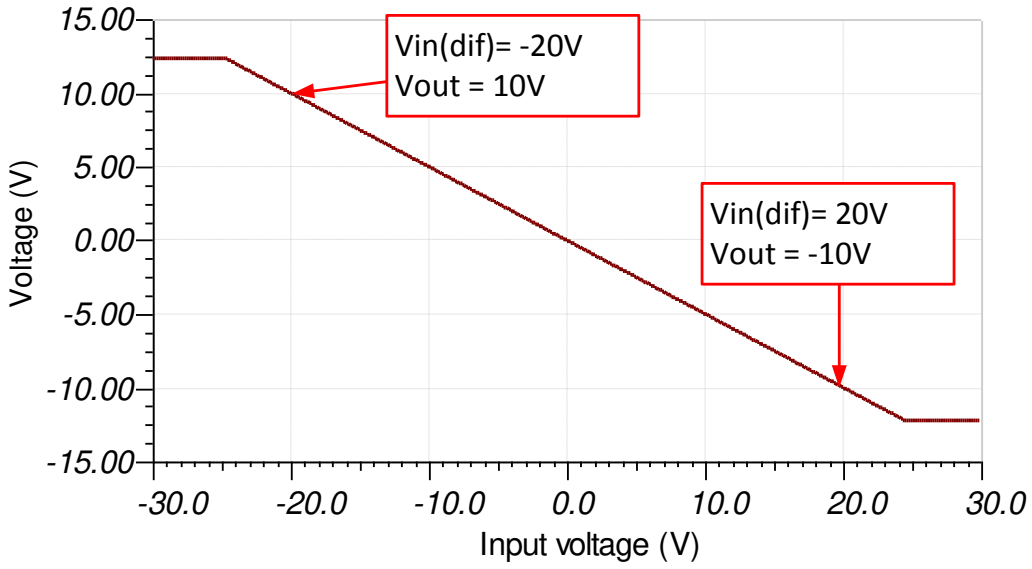
6. Find the value for Cf that achieves the desired closed-loop bandwidth. In this example, users need a 10kHz bandwidth. Note: if users adjust the bandwidth, then users need to verify the charge bucket filter settling (C_{filt} and R_{filt}) as the closed-loop bandwidth effects settling.

$$C_f=\frac{1}{2\cdot\pi\cdot R_f\cdot f_c}=\frac{1}{2\cdot\pi\cdot(5.05k\Omega)\cdot(10kHz)}=3.1nF\quad or\quad 3nF\quad standard\quad value$$

7. Find the value for Cfilt and Rfilt using *TINA SPICE* and the methods described in *Introduction to SAR ADC Front-End Component Selection*. The value of Rfilt and Cfilt shown in this document works for these circuits; however, if users use different amplifiers or different gain settings, then users must use TINA SPICE to find new values.

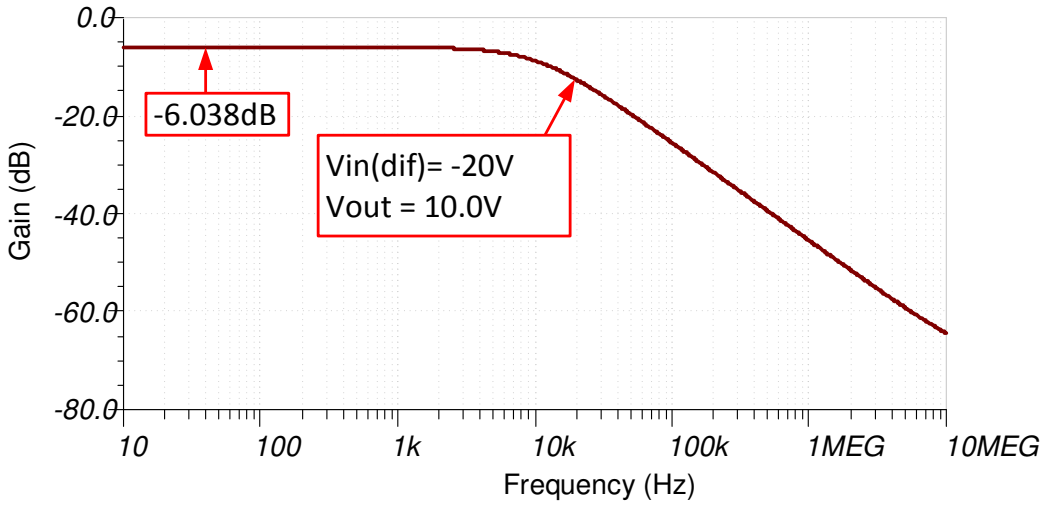
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –20V to +20V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



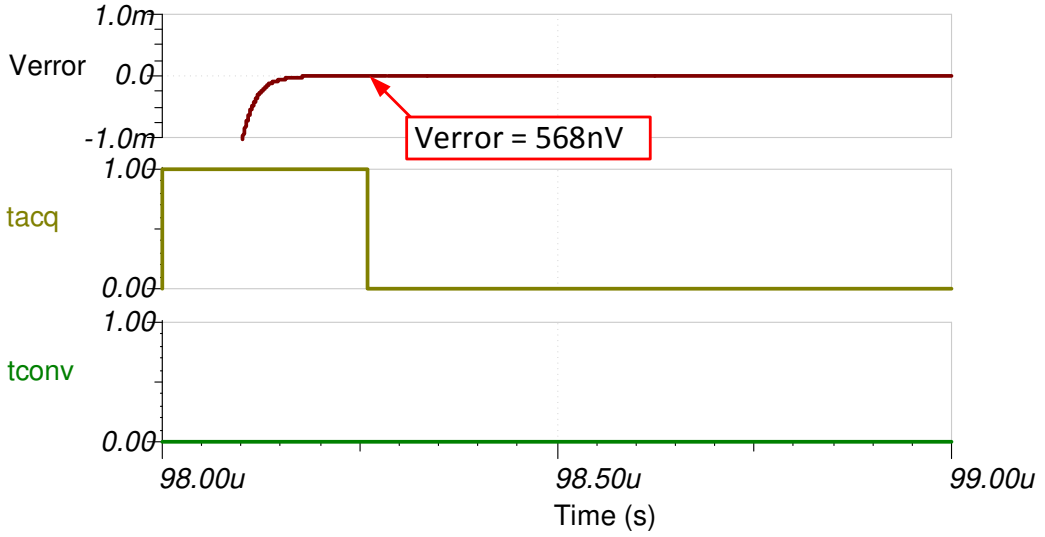
AC Transfer Characteristics

The bandwidth is simulated to be 10.58kHz and the gain is –6.038dB which is a linear gain of 0.5V/V. See the *Op Amps: Bandwidth 1* video for more details on this subject.



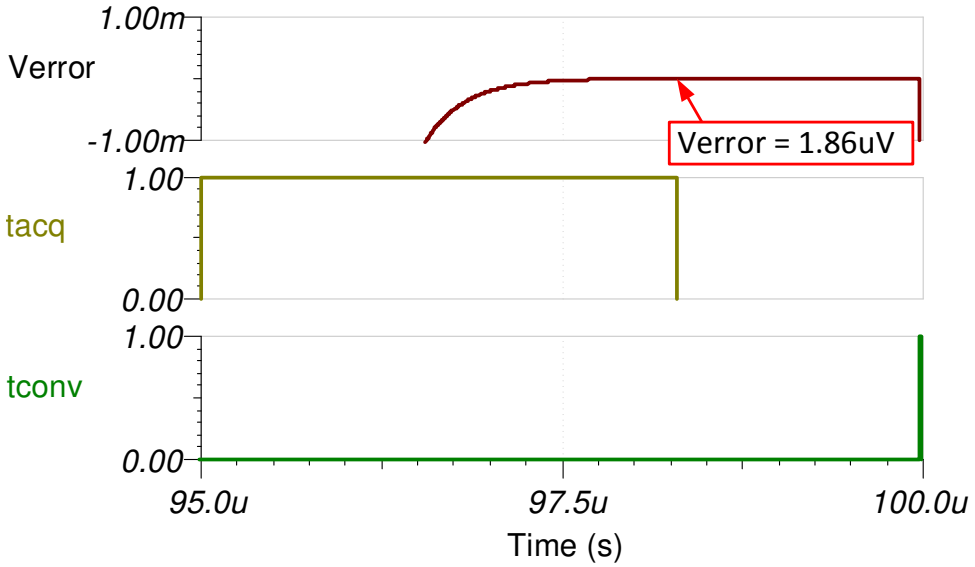
Transient ADC Input Settling Simulation Highest Sampling rate – 510ksps on ADS8568+OPA827

The following simulation shows settling to a 20V DC input signal with OPA827. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV). For detailed theory on this subject, refer to *Introduction to SAR ADC Front-End Component Selection*.



Transient ADC Input Settling Simulation Lower Sampling rate – 200ksps on ADS8568+OPA192

The following simulation shows settling to a 20V DC input signal with OPA192. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV).



Noise Calculation

This section demonstrates a full-noise analysis including resistor noise. Also, look at the noise below f_c (Noise Gain = 1.5), and the noise above f_c (noise Gain = 1). In this example, the noise is dominated by wide band amplifier noise so the resistors do not contribute significantly. However, in many cases the resistor noise can be important, so the full noise calculation is provided. For more detailed theory on this subject, refer to *Calculating the Total Noise for ADC Systems* and *Op Amps: Noise 1*.

Bandwidth for feedback loop:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} = \frac{1}{2 \cdot \pi \cdot (5.05k\Omega) \cdot (3nF)} = 10.6kHz$$

Noise from OPA827: 3.8nV/rtHz

$$E_{n\_amp1} = e_{n\_827} \cdot \sqrt{K_n \cdot f_c} = \left(3.8nV/\sqrt{Hz}\right) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 490nVrms$$

Thermal noise density from feedback loop (R_{f1} and R_{g1}) and RC non-inverting input (R_{f2} and R_{g2}):

$$R_{eq} = R_f \left|\right| R_g \quad = \quad \frac{R_f \cdot R_g}{R_f + R_g} = \frac{(5.05k\Omega) \cdot (10.1k\Omega)}{5.05k\Omega + 10.1k\Omega} = 3.37k\Omega$$

$$e_{n\_feedback} = \sqrt{4 \cdot K_n \cdot T_K \cdot R_{eq}} = \sqrt{4 \cdot \left(1.38 \cdot 10^{-23}\right) \cdot \left(298\right) \cdot \left(3.37k\Omega\right)} = 7.4nV/\sqrt{Hz}$$

$$E_{n\_feedback} = e_{n\_feedback} \cdot \sqrt{K_n \cdot f_c} = \left(7.4nV/\sqrt{Hz}\right) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 0.955\mu Vrms$$

Noise from resistors on the non-inverting input is the same as noise from the feedback resistors.

$$E_{n\_input} = E_{n\_feedback} = 0.955\mu Vrms$$

Total noise (in gain) referred to output of amplifier:

$$E_{n\_below\_fc} = \left(G_n\right)\sqrt{{E_{n\_amp1}}^2 + {E_{n\_feedback}}^2 + {E_{n\_input}}^2}$$

$$E_{n\_below\_fc} = \left(1.5\right)\sqrt{(0.49\mu V)^2 + (0.995\mu V)^2 + (0.995\mu V)^2} = 2.155\mu Vrms$$

Noise above fc is limited by the output filter (cutoff given below):

$$f_{output} = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (49.9\Omega) \cdot (370pF)} = 8.6MHz$$

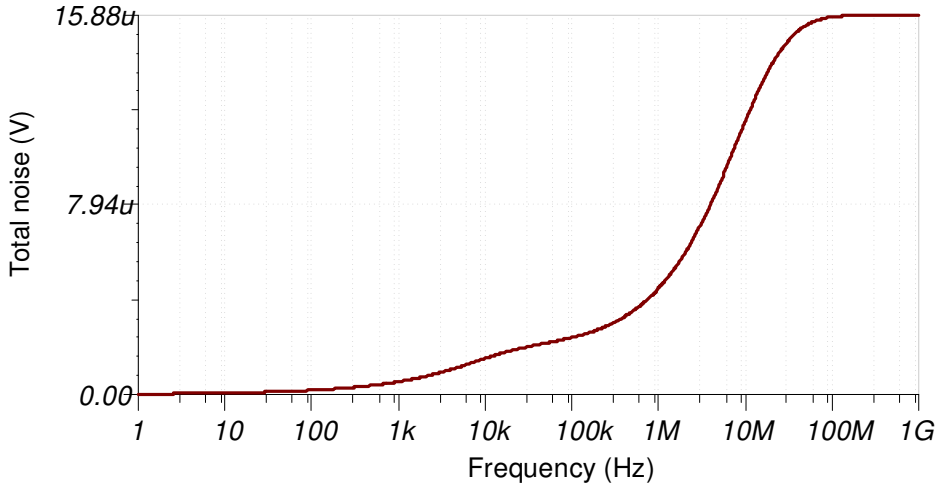
$$E_{n\_above\_fc} = e_{n\_827} \cdot \sqrt{K_n \cdot f_{output}} = \left(2.8nV/\sqrt{Hz}\right) \cdot \sqrt{(1.57) \cdot (8.6MHz)} = 13.963\mu V$$

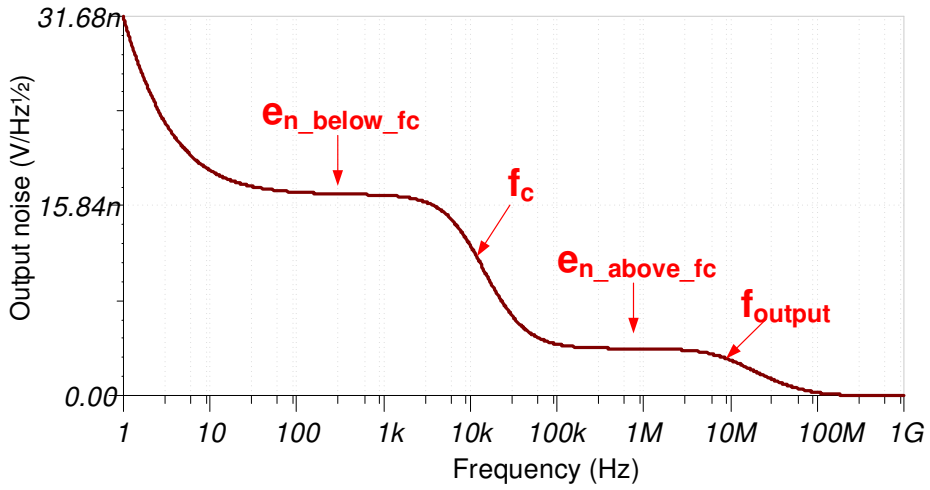
Total noise applied to input of the ADC:

$$E_{n\_total} = \sqrt{{E_{n\_below\_fc}}^2 + {E_{n\_above\_fc}}^2} = \sqrt{(2.155\mu V)^2 + (13.963\mu V)^2} = 14.128\mu Vrms$$

Noise Simulation

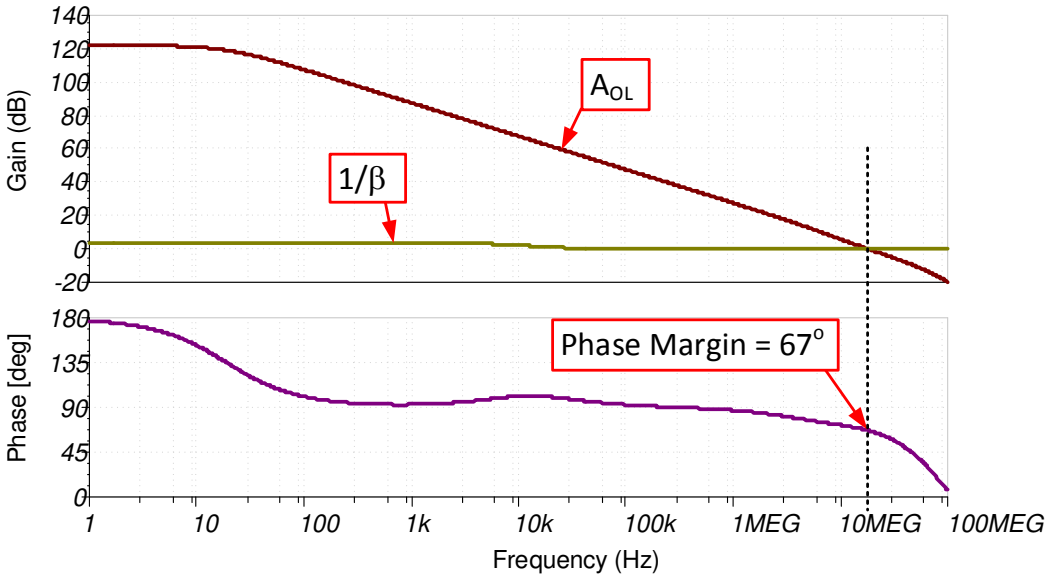
The simulated results compare well with the calculated results (that is, simulated = 15.88µVrms, calculated = 14.128µVrms).

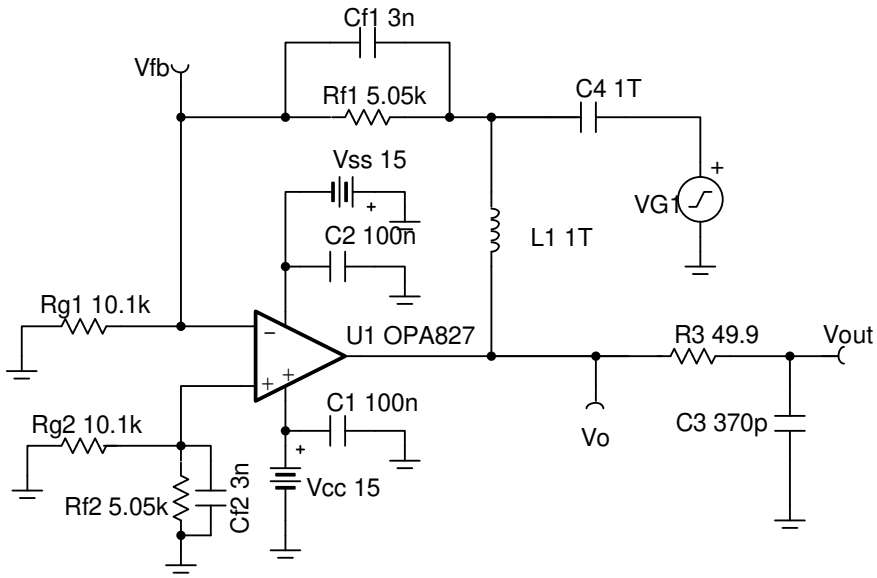




Stability Test

The phase margin for this OPA827 driving circuit is 67.1°, which meets the >45° requirement and is stable. For detailed theory explaining stability analysis, refer to *Op Amps: Stability 1*.





Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8568 (1)	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	www.ti.com/product/ADS8568	www.ti.com/adcs
OPA827	Low-Noise, High-Precision, JFET-Input Operational Amplifier	www.ti.com/product/OPA827	www.ti.com/opamp
OPA192	High-Voltage, Rail-to-Rail Input/Output, 5μV, 0.2μV/°C, Precision operational amplifier	www.ti.com/product/OPA192	www.ti.com/opamp

(1) The ADS8568 has integrated a precision voltage reference which can meet most design requirements, but an external REF5050 can be directly connected to the ADS8568 without any additional buffer because the ADS8568 has a built in internal reference buffer for every ADC channel pair. Also, REF5050 has the required low noise and drift for precision SAR applications. C1 is added to balance CMRR (common-mode rejection ratio). Clean analog power supplies are required to achieve best performance specified in the data sheet of the ADC.

Design References

For TI's comprehensive circuit library, refer to *Analog Engineer's Circuit Cookbooks*.

Link to Key Files (TINA)

Design files for this circuit – http://www.ti.com/lit/zip/sbac180.

Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (January 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to *Data Converters*. Added link to circuit cookbook landing page	1

Analog Engineer's Circuit

Circuit To Increase Input Range on an Integrated Analog Front End (AFE) SAR ADC

Cynthia Sosa

Input	ADC Input	Digital Output
VinMin = –40V	AIN-xP = –10V, AIN-xGND = 0V	-131072_{10} or 20000_{H}
VinMax = 40V	AIN-xP = 10V, AIN-xGND = 0V	131071_{10} or $1FFFF_{H}$

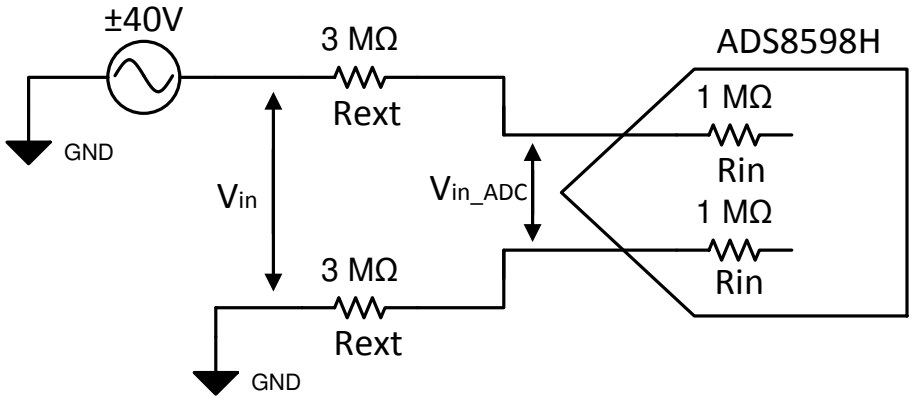
Power Supplies

AVDD	DVDD
5V	3.3V

Design Description

This cookbook design describes how to expand the input range of a SAR ADC with an integrated analog front end (AFE) and decrease the loss of accuracy by implementing a two-point calibration method. This design uses the ADS8598H at the full scale range of ±10V and expands the accessible input range to ±40V. This allows for a wider input range to be used without extra analog circuitry to step down the voltage; instead a simple voltage divider is used to interact with the AFE of the device to step down the voltage near the device input. A calibration method can be implemented to eliminate any error that could occur.

A similar cookbook design, *Reducing Effects of External RC Filter on Gain and Drift Error for Integrated AFE: ±10V, up to 200kHz, 16 bit*, explaining how to measure introduced drift from external components can prove to also be helpful in this application. Increasing the input range that the ADC can measure proves useful in end equipment such as: *Data Acquisition Modules*, *Multi Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*.



Specifications

Specification	Measured Accuracy Without Calibration	Measured Accuracy With Calibration
±40V	0.726318%	0.008237%

Design Notes

1. Use low-drift resistors to decrease any error introduced due to temperature drift, such as 50ppm/°C with 1% tolerance or better. Note that as resistor values increase to 1MΩ and beyond, low-drift precision resistors can become more expensive.
2. An input filter is frequently required for this configuration. Placing it directly after the large input impedance can cause errors because of the capacitor leakage. If an input filtering capacitor is needed, an alternate schematic is shown in this design.

Component Selection

The internal impedance of the device is 1MΩ, the external resistor is selected based on the desired extended input range (Vin), in this case ±40V. This external resistor forms a voltage divider with the internal impedance of the device, stepping down the input voltage at the ADC input pins (Vin_{ADC}) within the device input range of ±10V.

1. Rearrange the voltage divider equation to solve for the external resistor value. This same equation can later be used to calculate the expected Vin_{ADC} value from the input voltage.

$$V_{in_{ADC}} = V_{in} \cdot \frac{R_{in}}{R_{in} + R_{ext}}$$

$$R_{ext} = \frac{V_{in} \cdot R_{in}}{V_{in_{ADC}}} - R_{in}$$

2. Solve for the external resistor value for the desired extended input voltage. Vin = ±40V, Rin = 1M Ω

$$R_{ext} = \frac{40V \cdot 1M\Omega}{10V} - 1M\Omega$$

The input can be extended to a variety of ranges, depending on what external resistor value is used.

Vin	Rext
±40	3MΩ
±30	2MΩ
±20	1MΩ
±12	200kΩ

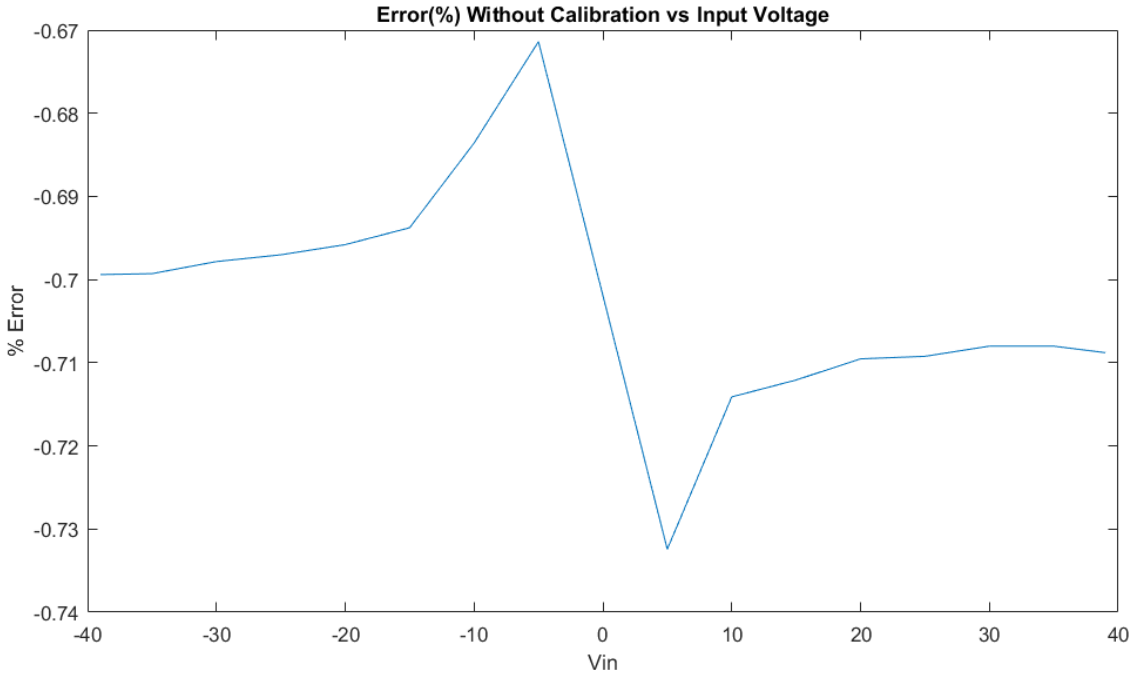
Non-Calibrated Measurements

Different DC input values ranging through the full ±40-V scale were used to measure the ADC voltage input and the accuracy of the measurement. The following equation shows how to calculate the analog voltage read by the ADC. Here the FSR is the system full scale range which is 40V in this case. The factor of 2 is included because this is a bipolar input where the input range is actually ±40V which is a range of 80V. $Vout_{ADC}$ for this equation will range ±40V, which corresponds to the system input.

$$V_{out_{ADC}} = Code_{out} \frac{2 \cdot FSR}{2^N}$$

The percent error of the value is calculated using the next equation:

$$Error(\%) = \frac{V_{in_{ADC}} - V_{out_{ADC}}}{V_{in_{ADC}}} \cdot 100$$



Two-Point Calibration

Calibration can be applied in order to eliminate the reading error introduced by the external resistor. The two-point calibration applies and samples two test signals at 0.25V from the full scale input range within the linear range of the ADC. These sample measurements are then used to calculate the slope and offset of the linear transfer function. Calibration will eliminate both the gain error introduced by the external resistor and the internal device gain error.

1. Apply test signal at –39V:

Vmin	Measured Code
–39V	–128689

2. Apply test signal at 39V:

Vmax	Measured Code
39V	128701

3. Calculate slope and offset calibration coefficients:

$$\text{Error}(\%) = \frac{V_{in_{ADC}} - V_{out_{ADC}}}{V_{in_{ADC}}} \cdot 100$$

$$m = \frac{Code_{max} - Code_{min}}{V_{max} - V_{min}} = \frac{128701 - (-128689)}{39V - (-39V)} = 3299.872$$

$$b = Code_{min} - m \cdot V_{min} = -128689 - 3299.872 \cdot (-39V) = 6.008$$

4. Apply calibration coefficients to all subsequent measurements:

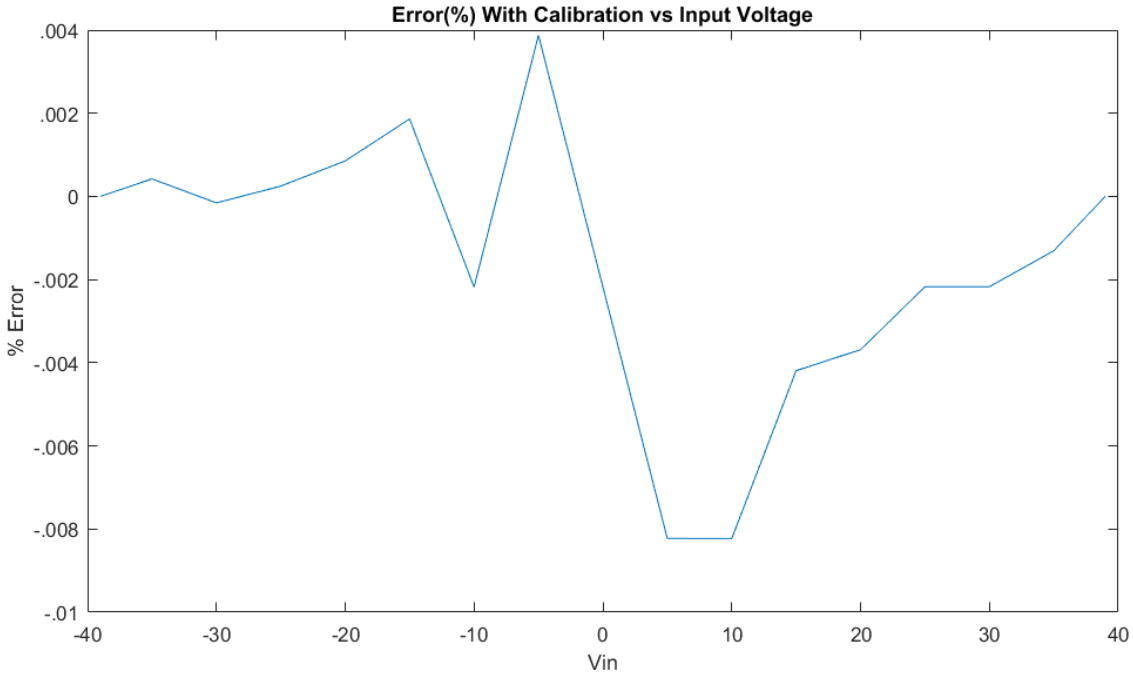
$$V_{in_{Calibrate}} = \frac{Code - b}{m} = \frac{128701 - 6.008}{3299.872} = 38.999$$

Two-Point Calibration Measurements

Calibration Coefficients

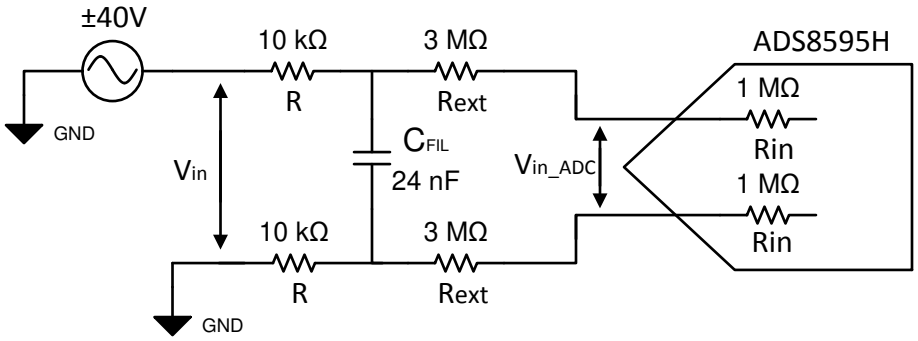
m = 3299.872; *b* = 6.008

When calibration is applied the readings error is dramatically reduced.



Alternate Schematic With Filter Capacitor

Due to the high-value resistors used, introducing a capacitor would lead to significant impact in readings, such as increase drift experienced. This is because of the capacitor leakage. This leakage will vary over time and temperature and will generate errors that are difficult to calibrate out. If an input filter is needed, the alternate schematic can be used to implement it. The capacitor is placed with a balanced resistor-capacitor filter before the external resistors in relation to the input signal.



Alternate Schematic With Filter Capacitor - Component Selection

External anti-aliasing RC filters reduce noise and protect from electrical overstress. A balanced RC filter configuration is required for better common-mode noise rejection; matching external resistors are added to both the negative and positive input paths. These external resistors should also be low-drift resistors as stated in the *Design Notes*.

1. Choose a value of R based on the desired cutoff frequency. This example uses a cutoff frequency of 320Hz, and a resistor value of 10kΩ.

   R = 10kΩ
2. Select C_{FIL}

$$C_{FIL} = \frac{1}{2 \cdot \pi \cdot f_c \cdot 2 \cdot R} = \frac{1}{2 \cdot \pi \cdot 320\text{Hz} \cdot 2 \cdot 10\,\text{k}\Omega} = 24.8\text{nF}$$

   Nearest standard capacitor value available, C_{FIL}= 24nF

Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8598H	18-bit high-speed 8-channel simultaneous-sampling ADC With bipolar inputs on a single supply	18-Bit 500kSPS 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply	Precision ADCs

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024) Page

- Updated the format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision * (February 2019) to Revision A (March 2019) Page

- Changed test signal values, equations, calibration coefficients, and graph in the Two-Point Calibration section..... 1
- Added text and an equation to the Non Calibrated Measurements section..... 1
- Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page... 1

Trademarks

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Analog Engineer's Circuit

High Common-Mode Differential Input Voltage to ±10-V ADC Input Circuit

Aaron Estrada

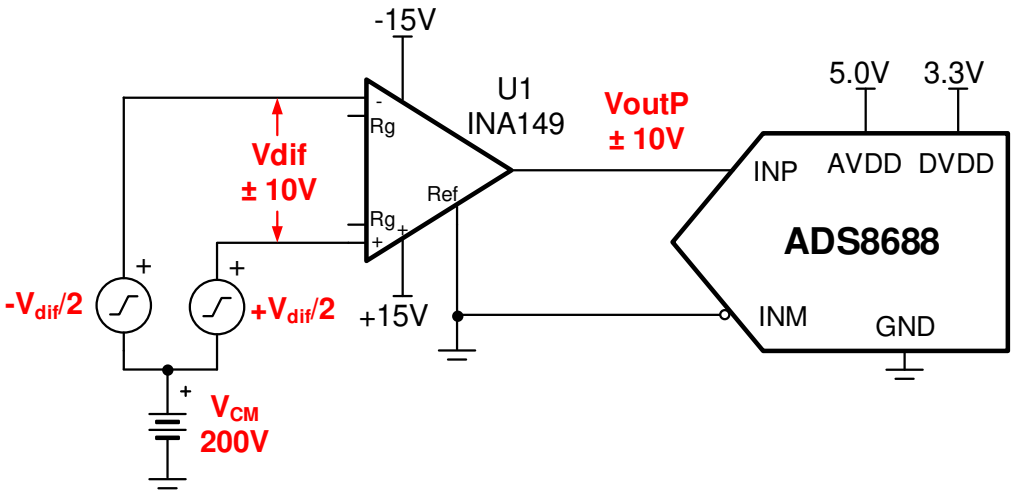
Input	ADC Input	Digital Output ADS8688
VinDiffMin = –10.24V	CH_x = –10.24V	0000_H
VinDiffMax = +10.24V	CH_x = +10.24V	$FFFF_H$

Power Supplies

AVDD	DVDD	AGND	DGND
5.0V	3.3V	GND	GND

Design Description

The purpose of this cookbook is to demonstrate the advantages and disadvantages of using difference amplifiers or instrumentation amplifiers to translate a signal with a high common mode voltage (Vcm) to a level that the ADS86XX family can accept. The ADS86XX family cannot support a high Vcm so using a difference or instrumentation amplifier to drive the ADC solves this issue. The INA828 device is an instrumentation amplifier with very high input impedance (100GΩ), excellent DC precision, and low noise. The INA828 can accept common-mode signals in the range of its supply voltage (±15V). The INA149 device is a unity-gain difference amplifier with a high input common-mode voltage range of up to ±275V, but the input impedance is lower than the INA828 device (differential = 800kΩ, common mode = 200kΩ). The ADS86XX family of ADCs has an integrated analog front end (AFE) and multiplexer which makes it an excellent candidate for a PLC (analog input module), protection relay, grid automation, and other various industrial applications.



Specifications

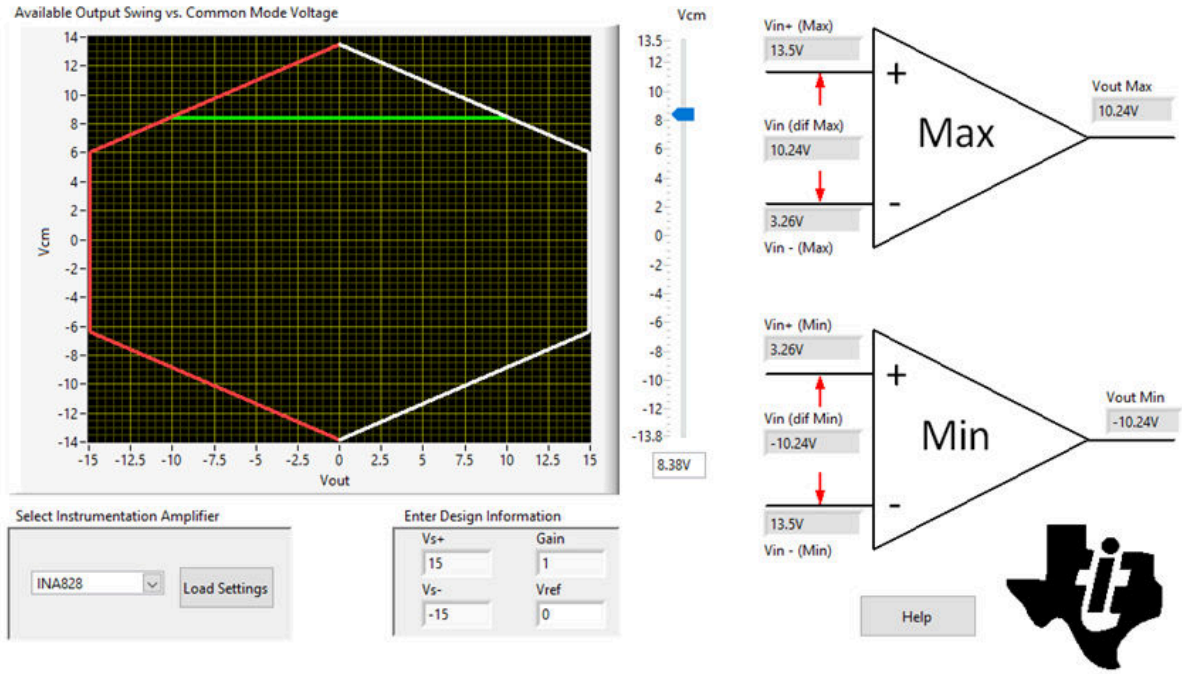
Specification	Calculated	Simulated	Measured
INA149 Common-Mode Voltage (VCM)	275V	275V	275V
INA828 Common-Mode Voltage (VCM)	8.38V	8.38V	7.5V
INA149 Integrated Noise	487µV	487.3µV	488µV
INA828 Integrated Noise	150µV	150µV	154µV

Design Notes

1. The ADS86XX family of HV SAR ADCs was selected because of the integrated analog front end and multiplexer. The integrated AFE eliminates the use of extra components to drive the ADC.
2. The INA149 device was selected to provide a very high common-mode voltage (Vcm = ±275V).
3. Comparing the INA828 device to the INA149 shows that the INA828 device has high input impedance (100GΩ), and the INA149 device has lower input impedance (differential = 800kΩ, common mode = 200kΩ). Also, the INA149 device has very wide common mode (Vcm = ±275V) but the INA828 common mode range is limited to the supply range (for example, ±15V). In cases where high input impedance is required, the INA828 device can be used, but be careful to not violate common-mode range. Note that high input impedance is important when the sensor output impedance is high as this creates a voltage divider effect and introduce error.
4. In this example, the input signal is ±10.24V. Therefore, resistor Rg is not needed to set the Gain = 1 for the INA828 device. If the input signal is smaller, use the appropriate resistor value to set the gain with a proper reference voltage on reference pin to achieve an input swing that matches the input range of the ADC.
5. Check the common mode range of the instrumentation amplifier using the Common-Mode Input Range Calculator for Instrumentation Amplifiers software tool.
6. If gain is required, use 0.1% 20ppm/°C film resistors or better for the gain setting resistor (Rg) to achieve best gain accuracy and low gain drift.

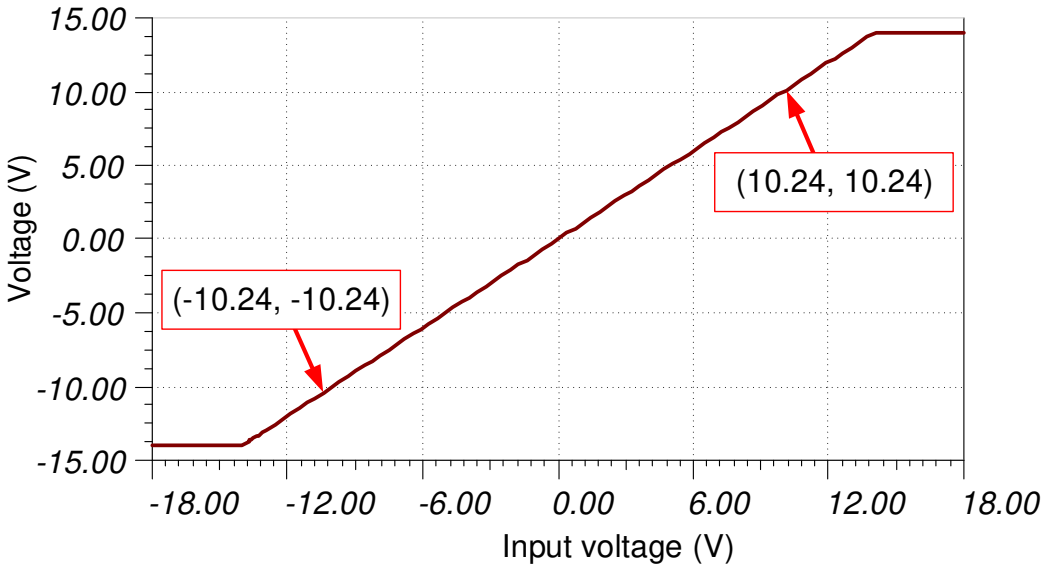
Component Selection

1. The ADS86XX can accept a single-ended input signal of ±10.24V. In this example, the input signal is ±10.24V so no external gain set resistor is required for the INA828 device. The INA149 device is a unity gain difference amplifier so no extra components are necessary.
2. The INA828 reference voltage input is used to shift inputs to match the input range of the ADC. In this example, the ADC input range is symmetrical so the reference pin is grounded.
3. Determine if the INA828 device is violating the common-mode range by using the Common-Mode Input Range Calculator for Instrumentation amplifiers. In this example, the INA828 device shows that you can achieve a maximum VCM of 8.38V with ±15V supplies, Gain = 1, and Vref = 0V.



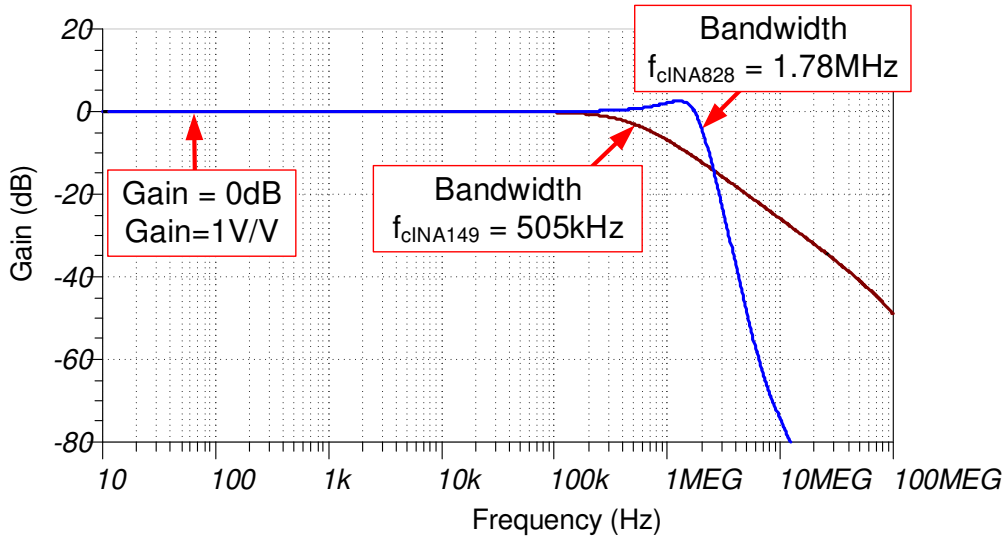
DC Transfer Characteristics

The following graphs show a linear output response for the INA149 device. The input range of the ADC is ±10.24V so the amplifier is linear well beyond the range the ADC requires. Refer to Determining a SAR ADC's Linear Range when using instrumentation amplifiers for detailed theory on this subject.



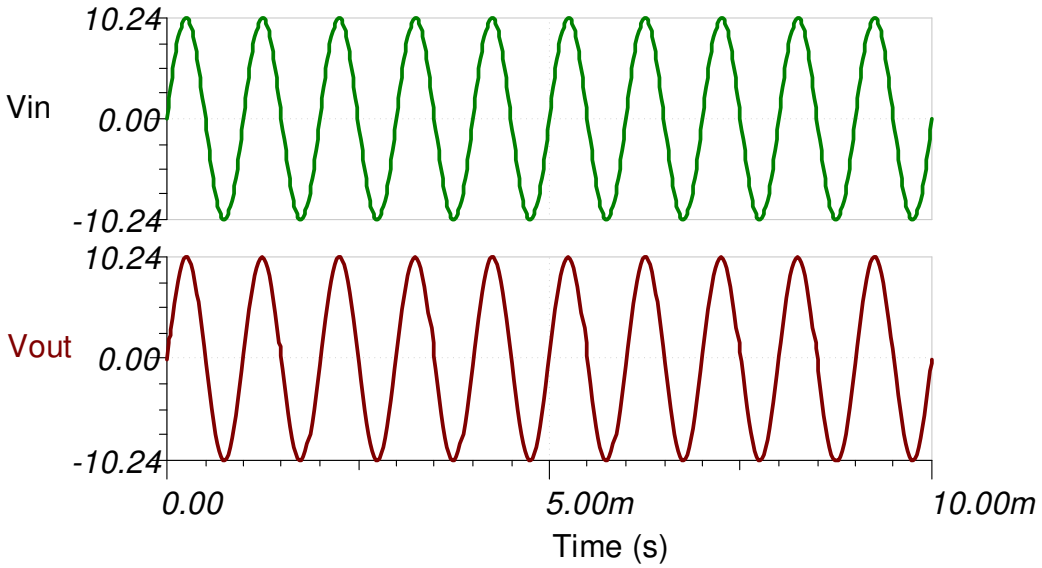
AC Transfer Characteristics

The simulated bandwidth for the INA149 device is 505kHz at gain = 1V/V, or 0dB. The simulated bandwidth for the INA828 device is 1.78MHz at a gain of 0dB. Both of the simulated bandwidths closely match the respective data sheets. See *Amplifier Bandwidth Video Series* for more details on this subject.

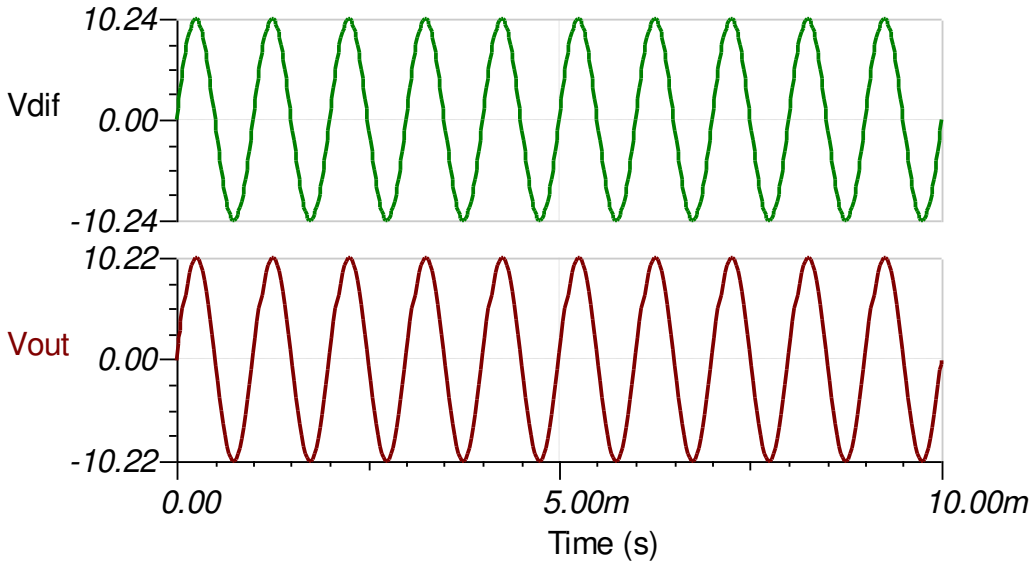


Transient ADC Input Settling Simulation

The INA149 device was simulated with a ±10.24-V differential input and a 275-V common-mode voltage. The following TINA simulation shows the differential input as well as the single-ended output for the INA149 device. The device has no issue with a common-mode voltage of 200V.



The INA828 device was simulated with a ±10.24-V differential input and a 7.75-V common-mode voltage. The following TINA simulation shows the differential input as well as the single-ended output for the INA828 device.



Noise Simulation

The section provides simplified noise calculations for the INA149 and INA828 devices. The simulated results closely match the calculated results. Refer to Op Amps: Noise 4 for detailed theory on amplifier noise calculations, and Calculating the Total Noise for ADC Systems for data converter noise.

INA149 integrated noise :

$$E_{nINA149} = e_{ni}\sqrt{f_c \cdot K_n} = \left(550nV / \sqrt{Hz}\right)\sqrt{505kHz \cdot 1.57} = 489\mu V_{RMS}$$

INA828 integrated noise :

$$E_{nINA828} = Gain\sqrt{e_{ni}^2 + e_{no}^2}\sqrt{f_c \cdot K_n} = (1)\sqrt{\left(7nV / \sqrt{Hz}\right)^2 + \left(90nV / \sqrt{Hz}\right)^2}\sqrt{1.78MHz \cdot 1.57} = 151\mu V_{RMS}$$

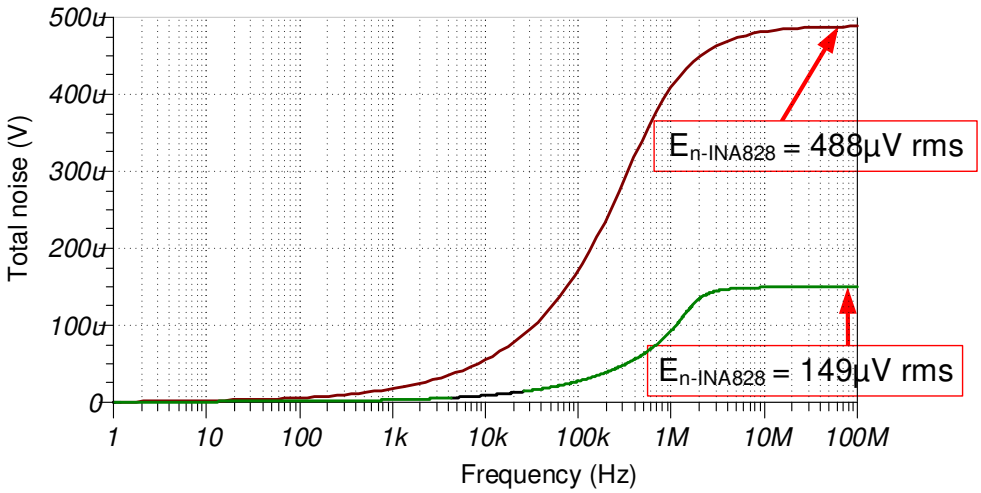
The ADS8688 device has an internal second-order 15-kHz LPF. This filter significantly reduces the noise from the instrumentation amplifiers.

INA149 integrated noise :

$$E_{nINA149} = e_{ni}\sqrt{f_c \cdot K_n} = \left(550nV / \sqrt{Hz}\right)\sqrt{15kHz \cdot 1.22} = 74.4\mu V_{RMS}$$

INA828 integrated noise :

$$E_{nINA828} = Gain\sqrt{e_{ni}^2 + e_{no}^2}\sqrt{f_c \cdot K_n} = (1)\sqrt{\left(7nV / \sqrt{Hz}\right)^2 + \left(90nV / \sqrt{Hz}\right)^2}\sqrt{15kHz \cdot 1.22} = 12.2\mu V_{RMS}$$



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS86XX	16-Bit Resolution, 4-,8-Channel MUX, SPI, 500ksps sample rate, on-chip 4.096V Reference	16-bit, 500-kSPS, 8-channel, single-supply SAR ADC with bipolar input ranges	Analog-to-digital converters (ADCs)
INA149	500kHz BW, Very High VCM, excellent nonlinearity	High Common Mode Voltage Difference Amplifier	Fully differential amplifiers
INA828	2MHz BW, Low Power12nV/√Hz noise	50-µV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	Instrumentation amplifiers

Link to Key Files

Texas Instruments, SBAC224 source files, software support

Trademarks

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Analog Engineer's Circuit

High-Current Battery Monitor Circuit: 0A – 10A, 0kHz – 10kHz, 18 Bit

Luis Chioye

Sense Resistor Current	INA Out, Amplifier Input	ADC Input	Digital Output ADS8910B
MinCurrent = ±50mA	Out = ±10mV	VoutDif = ±21.3mV	233_H 563_{10}, $3FDCB_H$ -564_0
MaxCurrent = +10A	Out = ±2V	VoutDif = ± 4.3V	$1B851^H$ 112722_{10} $247AE_H$ -112722_{10}

Table 1-1. Supply and Reference

Vs	Vee	Vref	Vcm
5.3 V <Vs <5.5V	0V	5V	2.5V

Design Description

This single-supply current sensing solution can measure a current signal in the range of ±50 mA to ±10 A across a shunt resistor. The current sense amplifier can measure shunt resistors over a wide common-mode voltage range from 0V to 75V. A fully differential amplifier (FDA) performs the single-ended to differential conversion and drives the SAR ADC differential input scale of ±5V at full data rate of 1MSPS. The values in the component selection section can be adjusted to allow for different current levels.

This circuit implementation is applicable in accurate voltage measurement applications such as battery maintenance systems, battery analyzers, *battery cell formation and test equipment, automatic test equipment*, and Remote Radio Units (RRU) in wireless base stations.

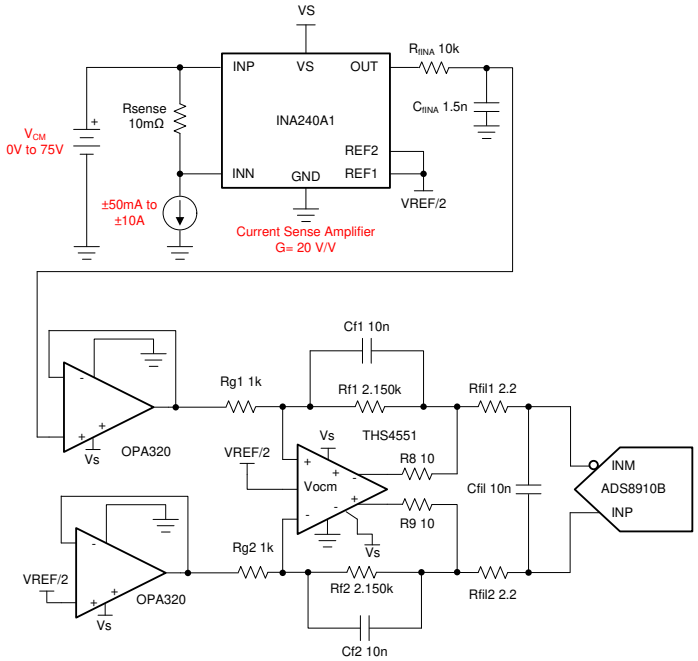


Table 1-2. Specifications

Error Analysis	Calculated	Simulated	Measured
Transient ADC Input Settling	> 1LSB > 38µV	6.6µV	N/A
Noise (at ADC Input)	221.8µV rms	207.3µV rms	227µV rms
Bandwidth	10.6kHz	10.71kHz	10.71kHz

Design Notes

1. Determine the shunt sense resistor value and select the current sense amplifier based on the input current range and input common mode voltage requirements. This is covered in the *component selection* section.
2. Determine the fully differential amplifier gain based on the current sense amplifier output, the ADC full-scale range input and the output swing specifications of the fully differential amplifier. This is covered in the *component selection* section.
3. Select COG capacitors to minimize distortion.
4. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion.
5. The TI Precision Labs training video series covers methods for error analysis. Review the following links for methods to minimize gain, offset, drift, and noise errors: *Error and Noise.*
6. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and ac performance for the amplifier, gain settings, and data converter in this example. If the design is modified, select a different RC filter. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and ac performance.

Component Selection for Current Sense Circuit

1. Choose the Rsense resistor and find the gain for the current sense amplifier (bidirectional current).

$$R_{sh} = \frac{V_{sh(max)}}{I_{load(max)}} = \frac{100mV}{10A} = 0.01\Omega$$

$$\pm V_{out(range)} = \pm \frac{V_{REF}}{2} = \pm \frac{5V}{2} = \pm 2.5V$$

$$G_{INA} = \frac{\pm V_{out(range)}}{I_{load(max)} \times R_{sh}} = \frac{\pm 2.5V}{10A \times 0.01\Omega} = 25V/V$$

2. Calculate the current sense amplifier output range.

$$V_{ina\_outmax} = G_{INA} \times \left(I_{load(max)} \times R_{sh}\right) + \frac{V_{ref}}{2} = \left(20V/V\right) \times \left(10A \times 0.01\Omega\right) + \frac{5V}{2} = 4.5V$$

$$V_{ina\_outmax} = G_{INA} \times \left(I_{load(max)} \times R_{sh}\right) + \frac{V_{ref}}{2} = \left(20V/V\right) \times \left(-10A \times 0.01\Omega\right) + \frac{5V}{2} = 0.5V$$

3. Find ADC full-scale input range and results from step 3.

$$ADC_{Full-Scale\ Range} = \pm V_{REF} = \pm 5V$$

4. Find FDA maximum and minimum output for linear operation.

$$0.23V < V_{out} < 4.77V \quad \text{from THS4551 output low/high specification for linear operation}$$

$$V_{out\_FDA\_max} = 4.77V - 0.23V = 4.54V \quad \text{Differential max output}$$

$$V_{out\_FDA\_min} = -V_{out\_FDA\_max} = -4.54V \quad \text{Differential min output}$$

5. Find differential gain based on ADC full-scale input range, FDA output range and results from step 3.

$$Gain = \frac{V_{out\_FDA\_max} - V_{out\_FDA\_min}}{V_{INA\_outmax} - V_{INA\_outmin}} = \frac{4.54V - (-4.54V)}{4.5V - 0.5V} = 2.77V/V$$

$$\text{Gain} \approx 2.15\text{V/V} \quad \text{for} \quad \text{margin}$$

6. Find standard resistor values for differential gain.

$$\text{Gain}_{\text{FDA}} = \frac{R_f}{R_g} = 2.15\text{V/V}$$

$$\frac{R_f}{R_g} = 2.15\text{V/V} = \frac{2.15\text{k}\Omega}{1.00\text{k}\Omega} = 2.15\text{V/V}$$

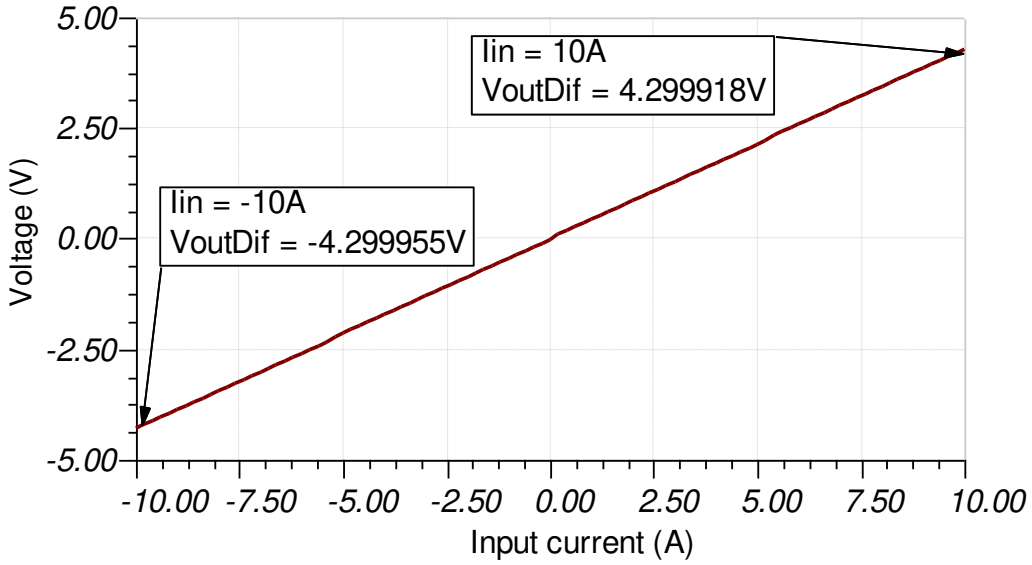
7. Find R_{flNA}, C_{flNA} for cutoff frequency.

$$C_{flNA} = \frac{1}{2 \times \pi \times f_c \times R_{flNA}} = \frac{1}{2 \times \pi \times 10\text{kHz} \times 10\text{k}\Omega} = 1.591\text{nF} \quad \text{or} \quad 1.5\text{nF} \quad \text{for} \quad \text{standard} \quad \text{value}$$

$$f_{fina} = \frac{1}{2 \times \pi \times C_{flNA} \times R_f} = \frac{1}{2 \times \pi \times 1.5\text{nF} \times 10\text{k}\Omega} = 10.6\text{kHz}$$

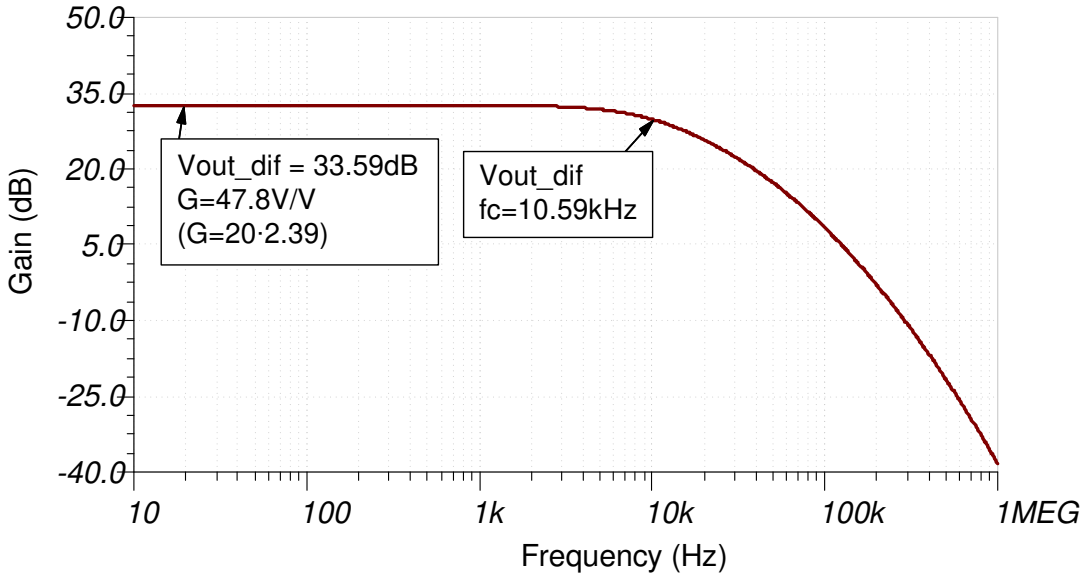
Fully Differential DC Transfer Characteristics

The following graph shows a linear output response for inputs from –10A to +10A.



AC Transfer Characteristics

The bandwidth is simulated to be 10.5kHz and the gain is 32.66dB which is a linear gain of 43V/V (G = 20×2.15V/V).



Noise Simulation

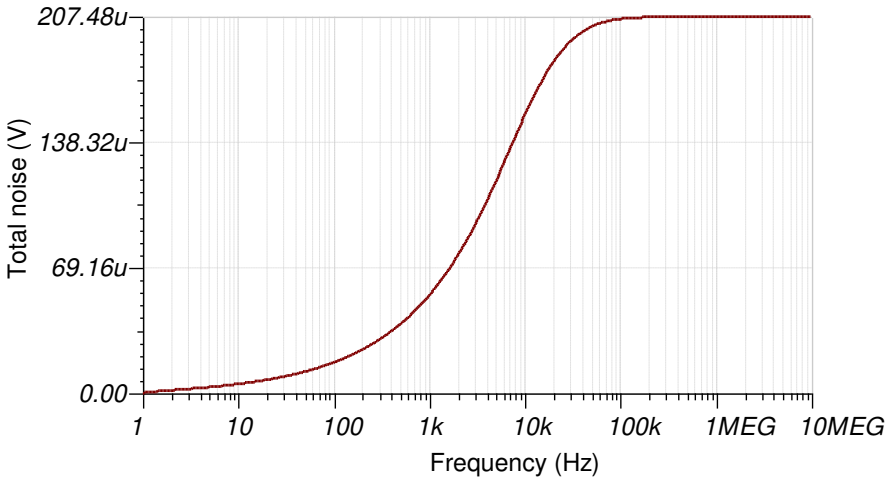
The following simplified noise calculation is provided for a rough estimate. Since the current sense amplifier INA240 is the dominant source of noise, the noise contribution of the OPA320 buffers and THS4521 is omitted in the noise estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10.6kHz.

$$f_c = \frac{1}{2\pi \times R_{flNA} \times C_{flNA}} = \frac{1}{2\pi \times 10k\Omega \times 1.5nF} = 10.6kHz$$

$$E_{nINA240} = e_{nINA240} \times G_{INA} \times \sqrt{K_n \times f_c} = \left(40nV \div \sqrt{Hz}\right) \times \left(20V \div V\right) \times \sqrt{1.57 \times 10.6kHz} = 103.2\mu V$$

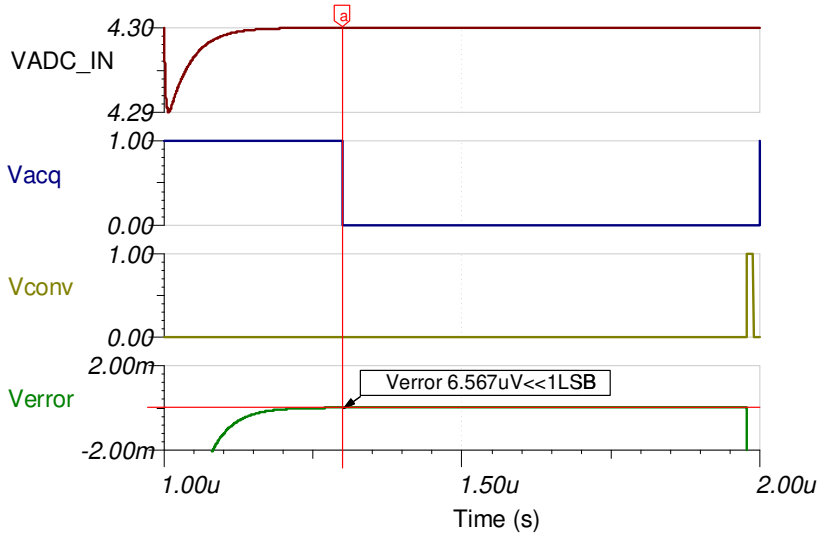
$$E_{nADCIN} = E_{nINA240} \times G_{FDA} = \left(103.2\mu Vrms\right) \times \left(2.15V/V\right) = 221.8\mu Vrms$$

Note that calculated and simulated match well. Refer to *Noise - Lab* for detailed theory on amplifier noise calculations, and *ADC noise measurement, methods and parameters* for data converter noise.



Transient ADC Input Settling Simulation

The following simulation shows settling to a 10-A DC input signal (ADC differential input signal +4.3V). This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Final SAR ADC Drive Simulations* for detailed theory on this subject.



Design Featured Devices:

Device	Key Features	Link	Similar Devices
ADS8910B (1)	18-bit resolution, 1-Msps sample rate, integrated reference buffer, fully differential input, Vref input range 2.5V to 5V	18-Bit, 1-MSPS, 1-Ch SAR ADC with Internal VREF Buffer, Internal LDO and Enhanced SPI Interface	Precision ADCs
INA240	High- and low-Side, bi-directional, zero-drift current sense amp, GainError = 0.20%, Gain = 20V/V, wide common-mode = –4V to 80V	-4 to 80V, bidirectional, ultra-precise current sense amplifier with enhanced PWM rejection	Instrumentation amplifiers
THS4551	Fully differential amplifier (FDA), 150-MHz bandwidth, Rail-to-Rail output, VosDriftMax = 1.8 µV/°C, e_n = 3.3 nV/rtHz	Low Noise, Precision, 150MHz, Fully Differential Amplifier	Operational amplifiers (op amps)
OPA320	20-MHz bandwidth, Rail-to-Rail with zero crossover distortion, VosMax = 150 µV, VosDriftMax = 5 µV/C, e_n = 7 nV/rtHz	Precision, zero-crossover, 20-MHz, 0.9-pA Ib, RRIO, CMOS operational amplifier	Operational amplifiers (op amps)
REF5050	3 ppm/°C drift, 0.05% initial accuracy, 4 µVpp/V noise	5-V, 3-µVpp/V noise, 3-ppm/°C drift precision series voltage reference	Series voltage references

(1) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR applications. The INA240 offers high common-mode range and low gain error in current sensing solutions. The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. The OPA320 is required to isolate the INA240 from any residual charge kickback at the inputs of the FDA.

Link to Key Files

Texas Instruments, ADS8900B Design File, software support

Trademarks

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Analog Engineer's Circuit

High-Input Impedance, True Differential, Analog Front End (AFE) Attenuator Circuit for SAR ADCs

Luis Chioye

Input Voltage (OPA197 Buffers)	THS4551 Output, ADC Input	ADS8912B Digital Output
VinP = –12V, VinN = +12V, VinMin (Dif) = –24V	VoutDif = –4.00V, VoutP = 0.25V, VoutN = 4.25V	$238E3_H$ -116509_{10}
VinP = +12V, VinN = –12V, VinMax (Dif) = +24V	VoutDif = +4.0V, VoutP = 4.25V, VoutN = 0.25V	$1C71C_H$ +116508_{10}

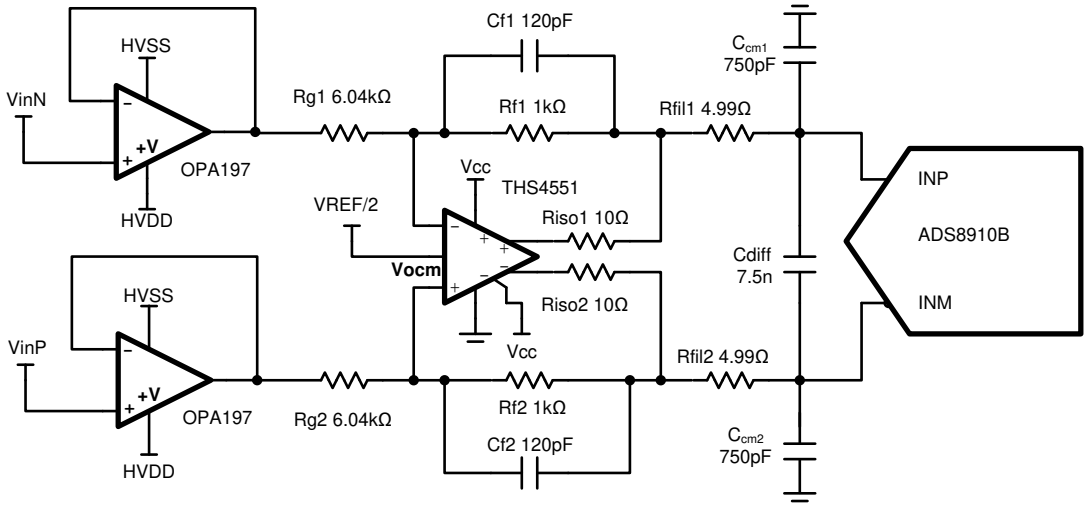
Supplies and Reference

HVDD	HVSS	Vcc	Vee	Vref	Vcm
+15V	–15V	+5.0V	0V	+4.5V	2.5V

Design Description

This analog front end (AFE) and SAR ADC data acquisition solution can measure true differential voltage signals in the range of ±24V (or absolute input range VinP = ±12V, VinN = ±12V) offering high-input impedance supporting data rates up to 500ksps with 18-bit resolution. A precision, 36-V rail-to-rail amplifier with low-input bias current is used to buffer the inputs of a fully-differential amplifier (FDA). The FDA attenuates and shifts the signal to the differential voltage and common-mode voltage range of the SAR ADC. The values in the *component selection* section can be adjusted to allow for different input voltage levels.

This circuit implementation is used in accurate measurement of true differential voltage in *parametric measurement units (PMUs)*, *precision multifunction input and output DAQs*, and *analog input modules* used in *Programmable Automation Control (PAC)*, *Discrete Control System (DCS)*, and *Programmable Logic Control (PLC)* applications.



Specifications

Specification	Goal	Calculated	Simulated
Transient ADC Input Settling (500ksps)	<< 1 LSB; << 34µV	N/A	0.5µV
Noise (at ADC Input)	$10\mu V_{RMS}$	$9.28\mu V_{RMS}$	$9.76\mu V_{RMS}$
Bandwidth	1.25MHz	1.25MHz	1.1MHz

Design Notes

1. Verify the linear range of the op amp (buffer) based on the common mode, output swing specification for linear operation. This is covered in the *component selection* section. Select an amplifier with low input bias current.
2. Find ADC full-scale range and common-mode range specifications. This is covered in the *component selection*.
3. Determine the required attenuation for the FDA based on the input signal amplitude, the ADC full-scale range and the output swing specifications of the FDA. This is covered in the *component selection* section.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion.
6. *Understanding and Calibrating the Offset and Gain for ADC Systems* covers methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors
7. *Introduction to SAR ADC Front-End Component Selection* covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to the *Precision Labs* videos for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection and Settings for Buffer Amplifier and FDA

1. Verify the buffer amplifier input range for linear operation:

   Select Supplies $(V-) = -15V$, $(V+) = +15V$ to allow VinP = ±12V VinN = ±12V range

   $(V-) - 0.1V < V_{cm} < (V+) - 3V$ from OPA197 common-mode voltage specification

   $-15.1V < V_{cm} < +12V$ allows required ±12V input voltage range

2. Verify the buffer amplifier output range for linear operation:

   $(V-) + 0.6V < V_{out} < (V+) - 0.6V$ from OPA197 Aol specification for linear operation

   $-14.4V < V_{out} < 14.4V$ allows required ±12V output voltage range

3. Find ADC full-scale input range. In this circuit, $V_{REF} = 4.5V$:

   $ADC_{Full\text{-}Scale\ Range} = \pm V_{REF} = \pm 4.5V$ from ADS8910B data sheet

4. Find the required ADC common-mode voltage:

   $$V_{CM} = \frac{+V_{REF}}{2} = +2.25V$$ from ADS8910B data sheet, therefore set FDA VCOM = 2.25V

5. Find FDA absolute output voltage range for linear operation:

   $0.23 < V_{out} < 4.77V$ from THS4551 output low / high specification for linear operation

   However, the positive range is limited by $ADC_{Full\text{-}Scale\ Range} = \pm 4.5V$, therefore

   $0.23V < V_{out} < 4.5V$ where $V_{outMin} = 0.23V$, $V_{outMax} = 4.5V$

6. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit follow:

$$V_{outMin} = \frac{V_{outDifMin}}{2} + V_{cm} \text{ and } V_{outMax} = \frac{V_{outDifMax}}{2} + V_{cm}$$

Re-arrange the equations and solve for $V_{outDifMin}$ and $V_{outDifMax}$.

Find maximum differential output voltage range based on worst case:

$$V_{outDifMax} = 2 \times V_{outMax} - 2 \times V_{cm} = 2 \times (4.5V) - 2 \times (2.25V) = 4.5V$$

$$V_{outDifMin} = 2 \times V_{outMin} - 2 \times V_{cm} = 2 \times (0.23V) - 2 \times (2.5V) = -4.04V$$

Based on combined worst case, choose $V_{outDifMin}$ = -4.04V and $V_{outDifMax}$ = +4.04V

7. Find the FDA differential input voltage range:

$$V_{inDifMax} = V_{inPmax} - V_{inNmin} = +12V - (-12V) = +24V$$

$$V_{inDifMin} = V_{inPmin} - V_{inNmax} = -12V - (+12V) = -24V$$

8. Find FDA required attenuation ratio:

$$Gain_{FDA} = \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} = \frac{(+4.04V) - (-4.04V)}{(+24V) - (-24V)} = 0.166 \frac{V}{V} \approx \frac{1}{6} \frac{V}{V}$$

9. Find standard resistor values to set the attenuation:

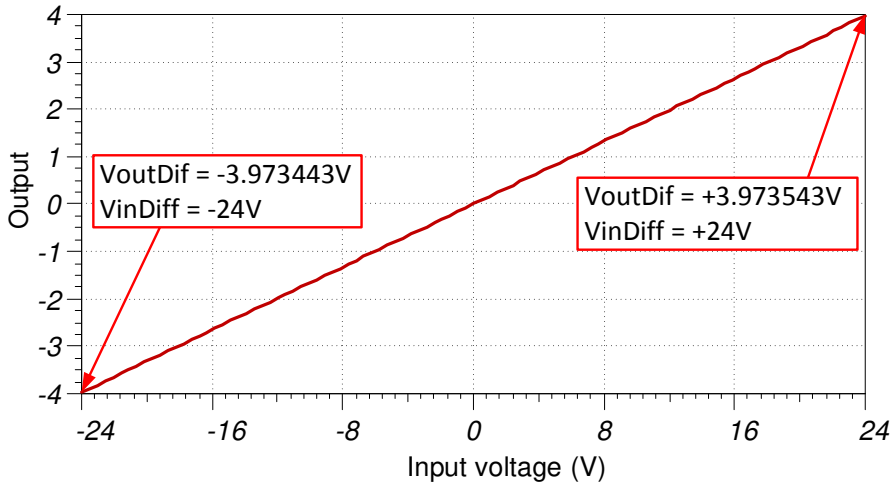
$$Gain_{FDA} = \frac{R_f}{R_g} = \frac{1}{6} V/V \Rightarrow \frac{R_g}{R_f} = \frac{1.00k\Omega}{6.04k\Omega} = \frac{1}{6.04} V/V$$

10. Find C_f for cutoff frequency f_c, R_{fINA} = 1kΩ:

$$C_f = \frac{1}{2 \cdot \pi \cdot f_c \cdot R_{fINA}} = \frac{1}{2 \cdot \pi \cdot (1.25MHz) \cdot (1k\Omega)} = 127pF \text{ or } 120pF \text{ standard value}$$

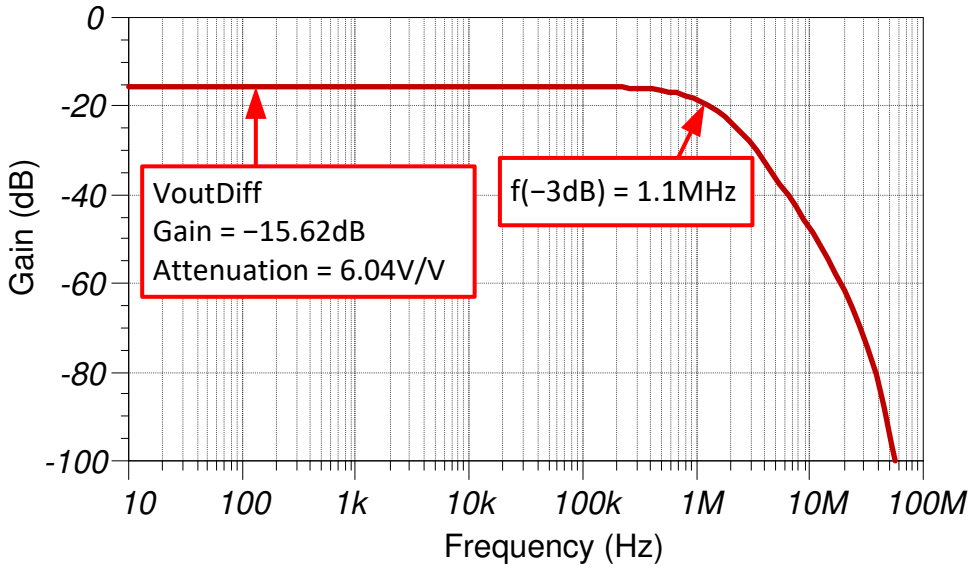
DC Transfer Characteristics

The following graph shows a linear output response for differential inputs from +24V to –24V.



AC Transfer Characteristics

The simulated bandwidth is approximately 1.1MHz and the gain is –15.62dB which is a linear gain of approximately 0.166V/V (attenuation ratio 6.04V/V).



Noise Simulation

Simplified Noise calculation for rough estimate :

$$f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} = \frac{1}{2 \cdot \pi \cdot (1\text{k}\Omega) \cdot (120\text{pF})} = 1.33\text{MHz}$$

Noise contribution of OPA197 buffer referred to ADC input

$$E_{nOPA197} = e_{nOPA197} \cdot \sqrt{K_n \cdot f_c} \cdot Gain_{FDA}$$

$$E_{nOPA197} = \left(5.5\text{nV} / \sqrt{\text{Hz}}\right) \cdot \sqrt{1.57 \cdot 1.33\text{MHz}} \cdot 0.166\text{V} / \text{V} = 1.319\mu V_{RMS}$$

Noise of THS4551 FDA referred to ADC input

$$\text{Noise gain} : NG = 1 + R_f / R_g = 1 + \frac{1.00\,\text{k}\Omega}{6.04\,\text{k}\Omega} = 1.166\text{V} / \text{V}$$

$$e_{noFDA} = \sqrt{\left(e_{nFDA} \cdot NG\right)^2 + 2\left(i_{nFDA} \cdot R_f\right)^2 + 2\left(4kTR_f \cdot NG\right)}$$

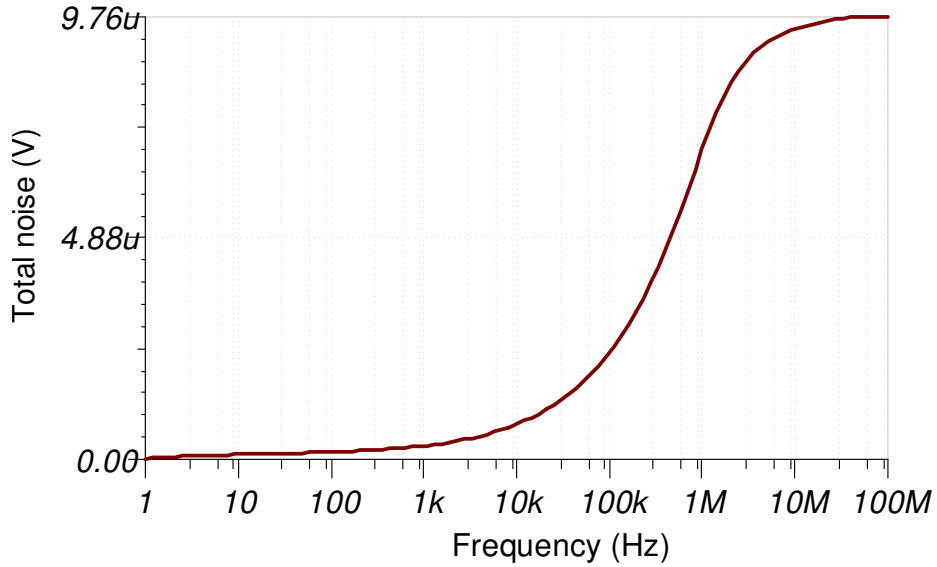
$$e_{noFDA} = \sqrt{\left(3.4\text{nV} / \sqrt{\text{Hz}} \cdot 1.166\text{V} / \text{V}\right)^2 + 2\left(0.5\text{pA} / \sqrt{\text{Hz}} \cdot 1\text{k}\Omega\right)^2 + 2\left(16.56 \cdot 10^{-18} \cdot 1.166\text{V} / \text{V}\right)}$$

$$e_{noFDA} = 7.4\text{nV} / \sqrt{\text{Hz}}$$

$$E_{nFDA} = e_{noFDA} \cdot \sqrt{K_n \cdot f_c} = \left(7.40\text{nV} / \sqrt{\text{Hz}}\right) \cdot \sqrt{1.57 \cdot 1.33\text{MHz}} = 9.28\mu V_{RMS}$$

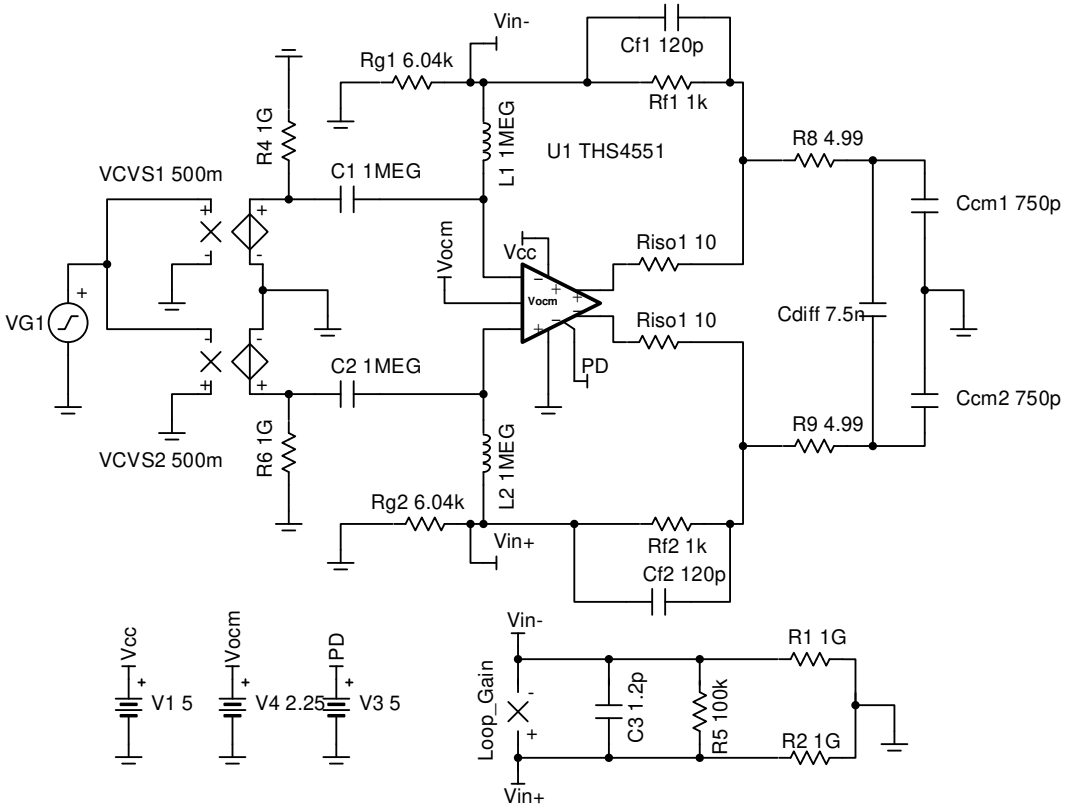
$$\text{Total Noise} = \sqrt{E_{nFDA}{}^2 + E_{nOPA197}{}^2} = \sqrt{\left(9.28\mu V_{RMS}\right)^2 + \left(1.32\mu V_{RMS}\right)^2} = 9.37\mu V_{RMS}$$

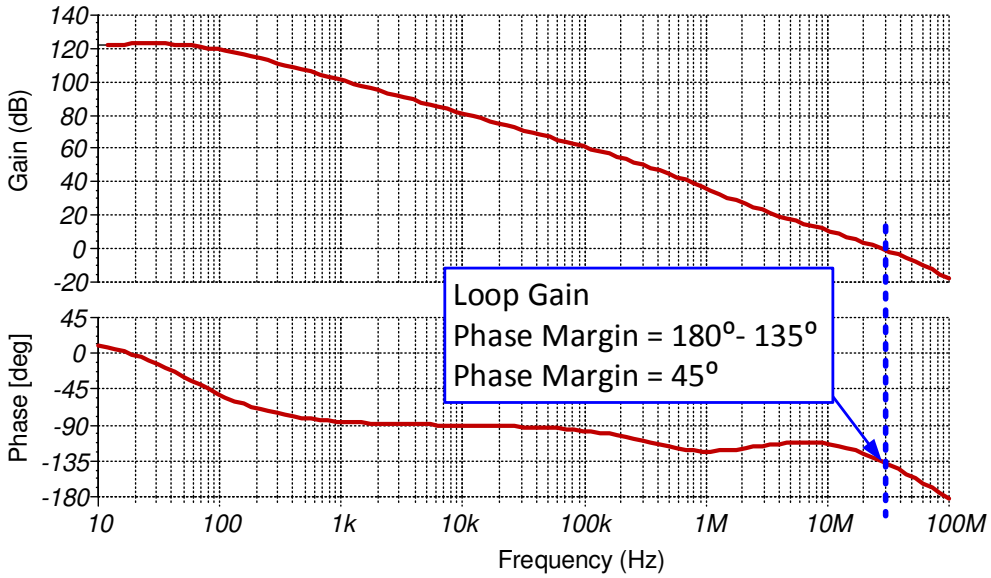
Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Stability Simulation

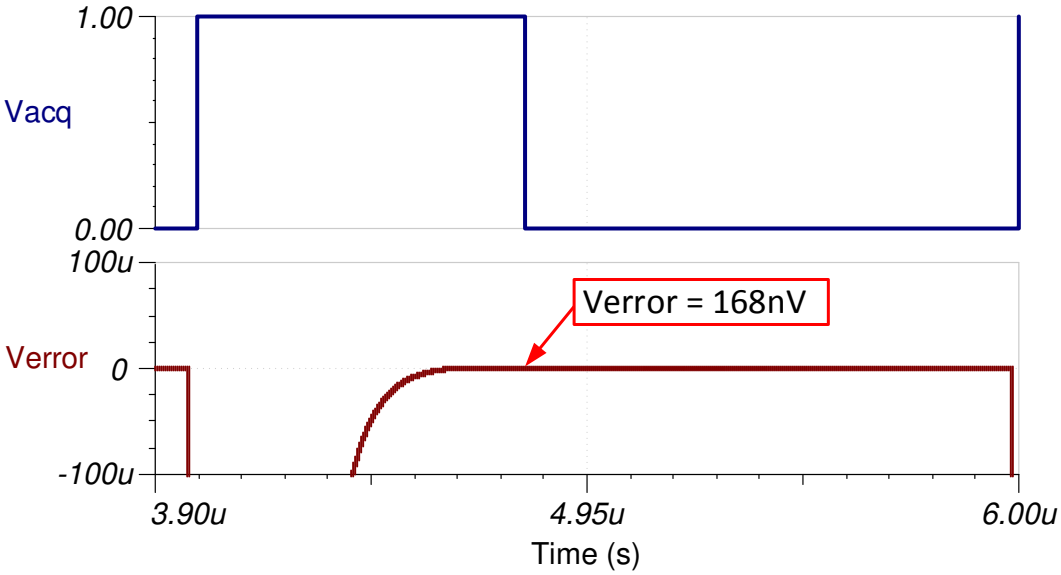
The following circuit is used in TINA to measure loop gain and verify phase margin using AC transfer analysis in TINA. Resistors R_{ISO} = 10Ω are used inside the feedback loop to increase phase margin. The circuit has 45 degrees of phase margin. Refer to *TI Precision Labs - Op Amps: Stability 4* for detailed theory on this subject.





Transient ADC Input Settling Simulation

The following simulation shows settling to a 24-V DC differential input signal with the OPA197 buffers inputs set at +12V and –12V. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8912B (1)	18-bit resolution, 500-ksps sample rate, integrated reference buffer, fully-differential input, Vref input range 2.5V to 5V.	18-Bit, 1MSPS, 1-Ch SAR ADC with Internal VREF Buffer, Internal LDO and Enhanced SPI Interface	Analog-to-digital converters (ADCs)
THS4551	FDA, 150-MHz bandwidth, Rail-to-Rail Output, VosDriftMax = 1.8µV/°C, e_n = 3.3nV/rtHz	Low Noise, Precision, 150MHz, Fully Differential Amplifier	Operational amplifiers (op amps)
OPA197	36V, 10-MHz bandwidth, Rail-to-Rail Input/Output, VosMax = ±250µV, VosDriftMax = ±2.5µV/°C, bias current = ±5pA	Single, 36V, precision, rail-to-rail input output, low offset voltage op amp	Operational amplifiers (op amps)
REF5045	VREF = 4.5V, 3 ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	4.5V, 3-µVpp/V noise, 3-ppm/°C drift precision series voltage reference	Series voltage references

(1) The REF5045 can be directly connected to the ADS8912B without any buffer because the ADS8912B has a built in internal reference buffer. Also, the REF5045 has the required low noise and drift for precision SAR applications. The THS4551 provides the attenuation and common-mode level shifting to the voltage range of the SAR ADC. In addition, this FDA is commonly used in high-speed precision fully-differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. The OPA197 is a 36-V operational amplifier that provides a very high input impedance front end, buffering the FDA inputs

Link to Key Files

Texas Instruments, SBAC183 source files, software support

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (February 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to Data Converters and added link to circuit cookbook landing page	1

Trademarks

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Analog Engineer's Circuit

High-Voltage Battery Monitor Circuit: ±20V, 0–10kHz, 18-Bit Fully Differential

Bryan McKay, Arthur Kay

Input	ADC Input	Digital Output ADS8910
VinMin = –20V	VoutDif = 4.8V, VoutP = 4.9V, VoutN = 0.1V	$1EB85_H$ or 125829_{10}
VinMax = 20V	VoutDif = –4.8V, VoutP = 0.1V, VoutN = 4.9V	$2147B_H$ or $–125829_{10}$

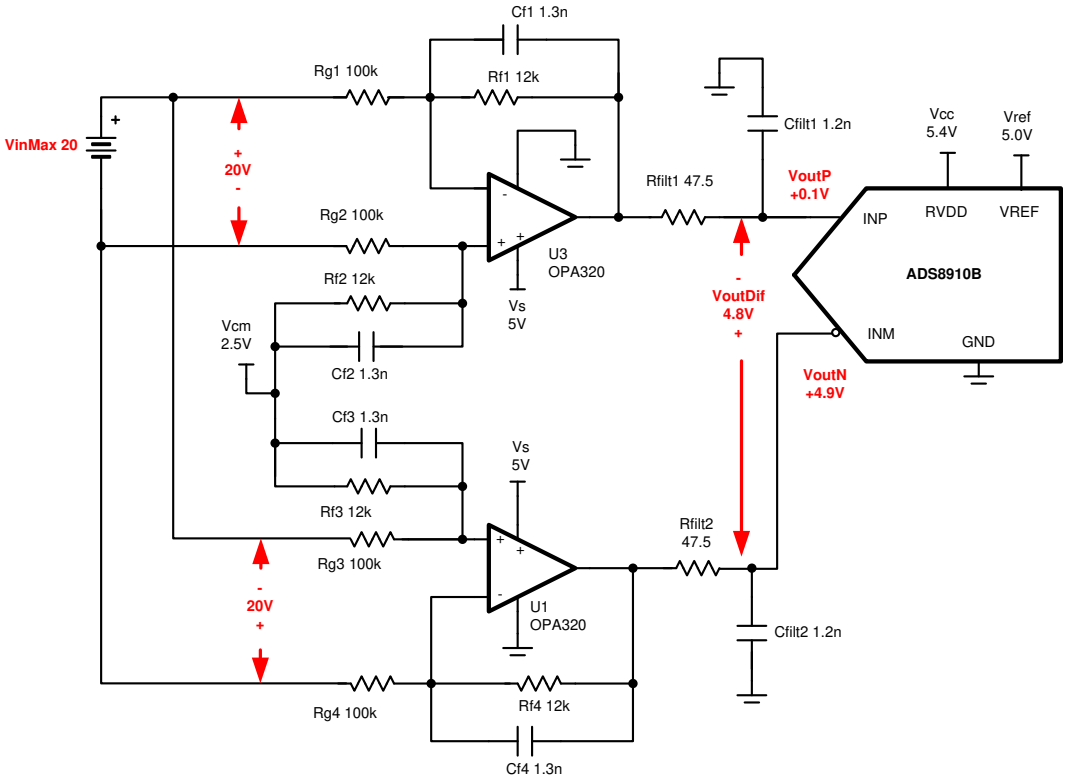
Power Supplies

Vcc	Vee	Vref	Vcm
5.3V	0V	5V	2.5V

Design Description

This design translates an input bipolar signal of ±20V into a fully differential ADC differential input scale of ±4.8V, which is within the output linear operation of amplifiers. The values in the component selection section can be adjusted to allow for different input voltage levels.

This circuit implementation is applicable in accurate voltage measurement applications such as Battery Maintenance Systems, Battery Analyzers, *battery cell formation and test equipment*, *ATE*, and Remote Radio Units (RRU) in wireless base stations.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling	< 0.5LSB or 19µV	6.6µV	N/A
Noise	20.7µVrms	20.65µVrms	30.8µVrms
Bandwidth	10.2kHz	10.4kHz	10.4kHz

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
2. For capacitors in the signal path, select COG type to minimize distortion. In this circuit Cf1, Cf2, Cf3, Cf4, Cfilt1, and Cfilt2 need to be COG type.
3. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.
4. Precision labs video series covers methods for error analysis. Review the *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
5. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, select a different RC filter. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. The general equation for this circuit.

$$V_{outMinOpa} = \frac{V_{outDifMin}}{2} + V_{cm}$$

$$V_{outMaxOpa} = \frac{V_{outDifMax}}{2} + V_{cm}$$

$$V_{outDif} = V_{inDif} \times Gain_{dif}$$

$$Gain_{dif} = 2 \times \frac{R_f}{R_g}$$

2. Find op amp maximum and minimum output for linear operation.

$$-0.1\ V < V_{cm} < 5.1V \quad \text{from OPA320 Vcm specification}$$

$$0.035\ V < V_{out} < 4.965\ V \quad \text{from OPA320 Vout swing specification}$$

$$0.1\ V < V_{out} < 4.9\ V \quad \text{from OPA320 Aol specification for linear operation}$$

$$0.1\ V < V_{out} < 4.9\ V \quad \text{Combined worst case}$$

3. Rearrange the equation from part 1 and solve for VoutDifMin and VoutDifMax. Find maximum and minimum differential output voltage based on combined worst case from step2.

$$V_{outDifMax} = 2 \times V_{outMaxOpa} - 2 \times V_{cm} = 2 \times (4.9\ V) - 2 \times (2.5\ V) = 4.8\ V$$

$$V_{outDifMax} = 2 \times V_{outMinOpa} - 2 \times V_{cm} = 2 \times (0.1\ V) - 2 \times (2.5\ V) = -4.8\ V$$

4. Find differential gain based on results from step 3.

$$Gain = \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} = \frac{(4.8\ V) - (-4.8\ V)}{(20\ V) - (-20\ V)} = 0.24$$

5. Find standard resistor values for differential gain. Use *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$\frac{Gain_{dif}}{2} = \frac{R_f}{R_g} = \frac{0.24}{2} = 0.12$$

$$\frac{R_f}{R_g} = 0.12 = \frac{12\ \text{k}\Omega}{100\ \text{k}\Omega} = 0.12$$

6. Find Cf for cutoff frequency.

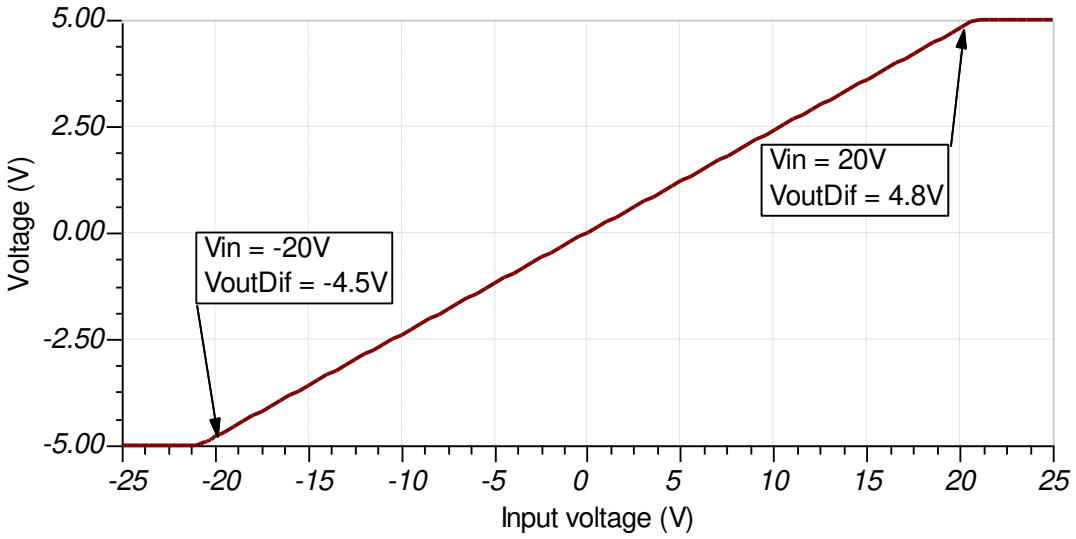
$$f = \frac{1}{2 \times \pi \times C_f \times R_f} = \frac{1}{2 \times \pi \times (1.3\text{nF}) \times (12\text{k}\Omega)} = 10.2\ \text{kHz}$$

$$C_f = \frac{1}{2 \times \pi \times f_c \times R_f} = \frac{1}{2 \times \pi \times (10\ \text{kHz}) \times (12\ \text{k}\Omega)} = 1.326\ \text{nF}\ \text{ or 1.3 nF for standard value}$$

$$f = \frac{1}{2 \times \pi \times C_f \times R_f} = \frac{1}{2 \times \pi \times (1.3\ \text{nF}) \times (12\text{k}\Omega)} = 10.2\text{kHz}$$

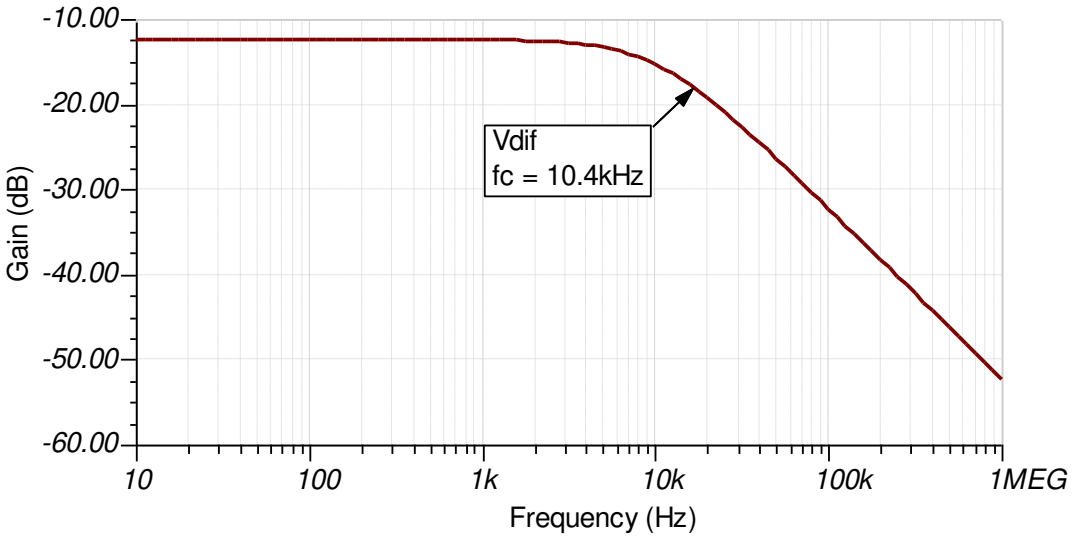
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –20V to +20V. Refer to *Determining a SAR ADC's linear range when using operational amplifiers* for detailed theory on this subject.



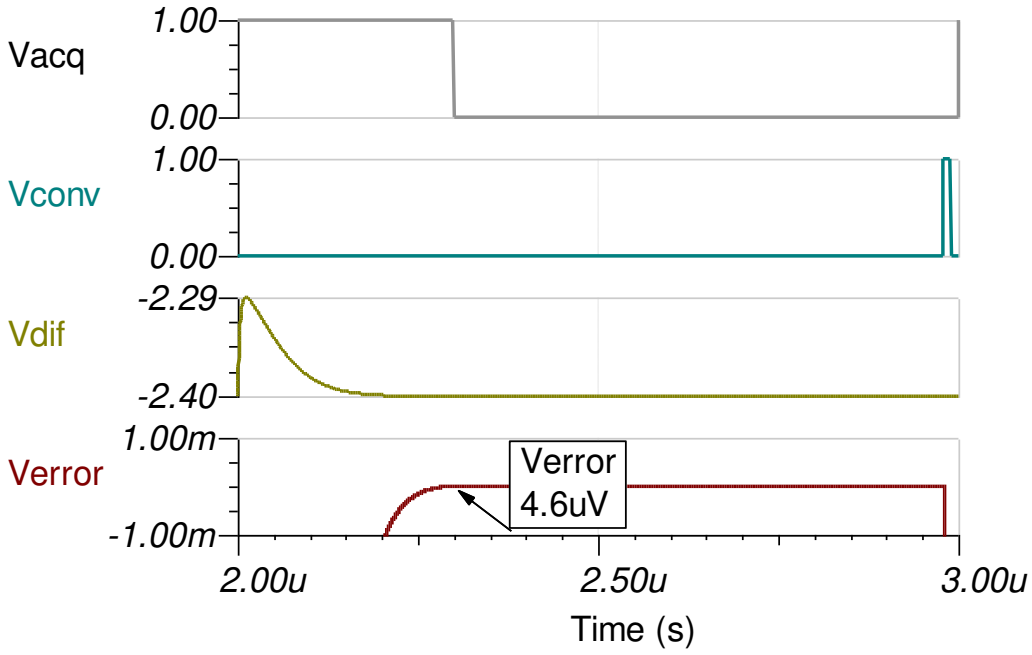
AC Transfer Characteristics

The bandwidth is simulated to be 10.4 kHz, and the gain is –12.4dB which is a linear gain of 0.12. See *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a –20V dc input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Noise Simulation

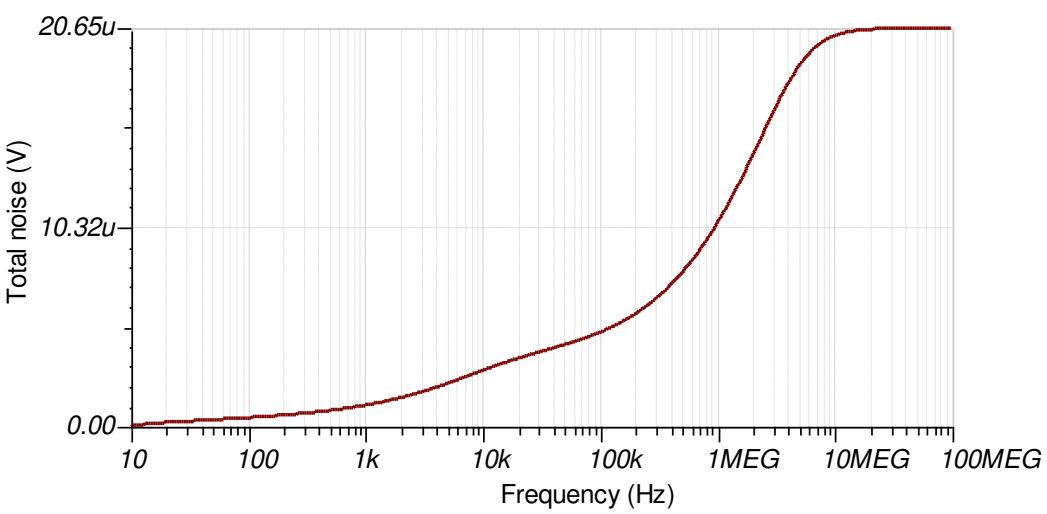
The following simplified noise calculation is provided for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times (47.5\Omega) \times (1.2nF)} = 2.8MHz$$

$$E_{n\_se} = e_{n320} \times \sqrt{K_n \times f_c} = \left(7nV \div \sqrt{Hz}\right) \times \sqrt{(1.57) \times (2.8MHz)} = 14.7\mu Vrms \quad \text{for a single ended input}$$

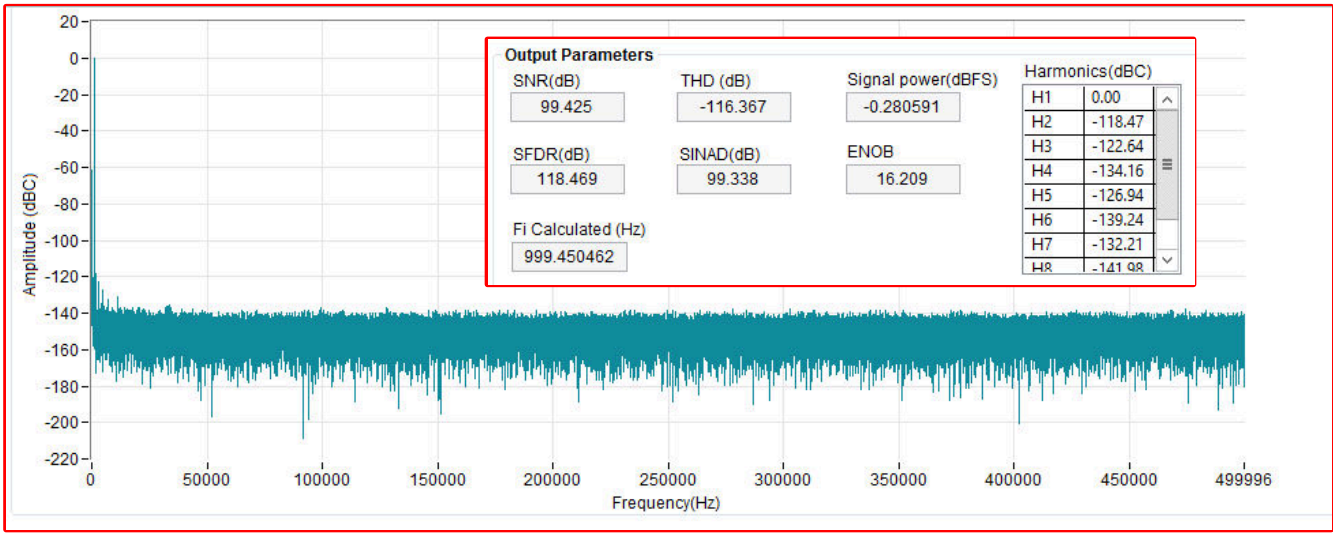
$$E_{n\_tot} = \sqrt{{E_{n\_se}}^2 + {E_{n\_se}}^2} = \sqrt{(14.7\mu V)^2 + (14.7\mu V)^2} = 20.7\mu V \quad rms \quad \text{Total noise for differential amplifier}$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS8910BEVM. The AC performance indicates SNR = 99.4dB, and THD = –116.4dB. See *Introduction to Frequency Domain* for more details on this subject.

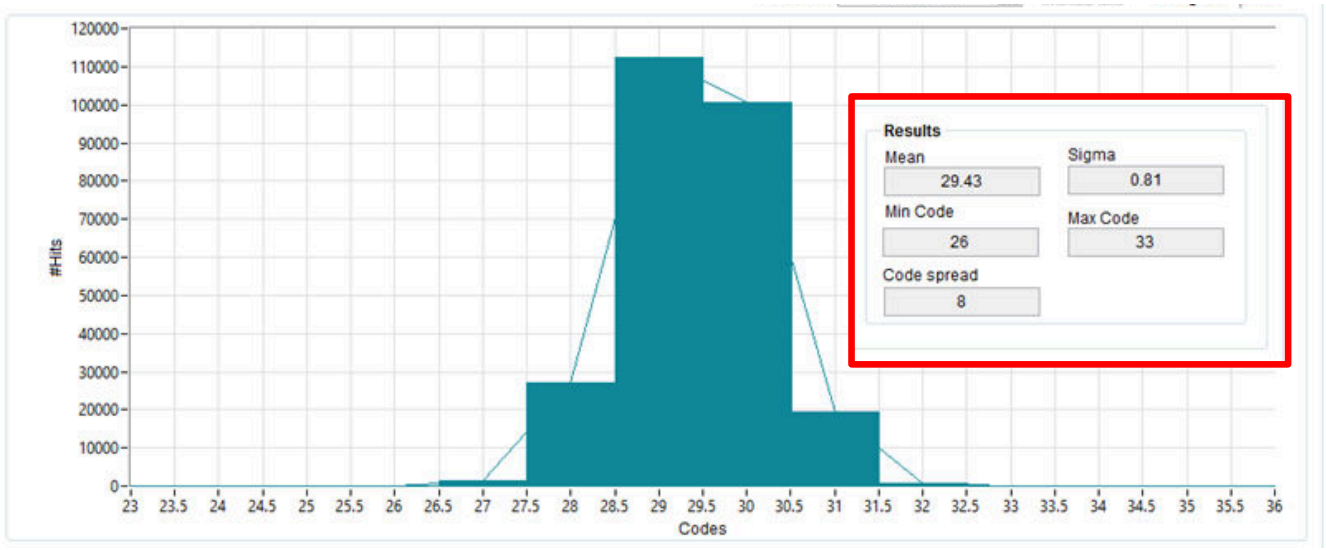


Noise Measurement

The following measured result is for both inputs connected to ground. The histogram shows the system offset and noise. The standard deviation in codes is given by the EVM GUI (0.81), and this can be used to calculate the RMS noise (30.9µV rms) as shown in the following equation.

$$\mathrm{LSB} = \frac{\mathrm{FSR}}{2^{\mathrm{N}}} = \frac{10\ \mathrm{V}}{2^{18}} = 38.14\mu\mathrm{V}$$

$$\mathrm{E_{n\_measured}} = \mathrm{E_{nSigma}} \times \mathrm{LSB} = \left(0.81\right) \times \left(34.14\ \ \mu\mathrm{V}\right) = 30.9\mu\mathrm{Vrms}$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8900B (1)	18-bit resolution, 1-Msps sample rate, Integrated reference buffer, fully differential input, Vref input range 2.5V to 5V.	20-bit, 1MSPS, one-channel SAR ADC with internal VREF buffer, internal LDO and enhanced SPI	Precision ADCs
OPA320 (2)	20-MHz bandwidth, Rail-to-Rail with Zero Crossover Distortion, VosMax = 150µV, VosDriftMax = 5uV/°C, en = 7nV/rtHz	Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, CMOS operational amplifier	Precision op amps (Vos<1mV)
REF5050 (3)	3ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	5V, 3µVpp/V noise, 3ppm/°C drift precision series voltage reference	Voltage references

(1) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. Furthermore, the zero crossover distortion rail-to-rail input allows for linear swing across most of the ADC input range.
(2) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.
(3) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.

Link to Key Files for High Voltage Battery Monitor

Texas Instruments, SBAC171 design files, software support

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (December 2017) to Revision A (January 2019)	Page
• Downstyle title, update title role content, added link to circuit cookbook library page	1

Trademarks

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Analog Engineer's Circuit

Single-Ended to Differential Signal Conversion Using an Op Amp and FDA for Unipolar Signals

Evan Sawyer

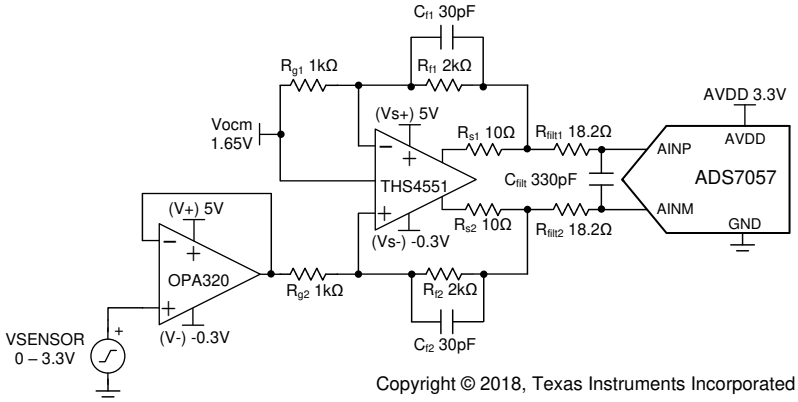
Input	ADC Input	Digital Output ADS7057
V_{in} Min = –3.3V	AINP = 0V AINM = 3.3V	2000_H 8192_{10}
V_{in} Max = 3.3V	AINP = 3.3V AINM = 0V	$1FFF_H$ 8191_{10}

Power Supplies

AVDD	GND	DVDD
3.3V	0V	1.8V

Design Description

This design is intended to demonstrate how to convert a unipolar, single-ended signal into a unipolar, fully-differential signal and drive a differential ADC (for more information on these and other signal types, please refer to the *TI Precision Labs* training titled *SAR ADC Input Types*). Compared to a single-ended device, a fully-differential ADC has twice the dynamic range which improves the AC performance of the converter. Many common systems, for example *Sonar Receivers*, *Flow Meters*, and *Motor Controls*, benefit from the higher performance of a differential ADC. The equations and explanation of component selection in this design can be customized based on system specifications and needs. For more information on a similar design using a bipolar input, see the cookbook circuit titled *Single-Ended to Differential Using an Op Amp and FDA for Bipolar Signals*.



Specifications

Specification	Calculated	Simulated
Transient ADC Input Settling (at 250ksps)	< 0.5 × LSB = 201µV	144.8µV
Conditioned Signal Range (at 250ksps)	> 99% ADC FSR = > 6.53V	6.60V
Noise	43.8µV ÷ √Hz	44.3µV ÷ √Hz

Design Notes

1. The ADS7057 was selected because of its throughput (2.5Msps), size (2.25mm²), and low-latency (successive approximation register, or SAR, architecture).
2. Determine the linear range of the fully-differential amplifier (ADC driver) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
3. Determine the linear range of the op amp (signal conditioning) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
4. Select COG (NPO) capacitors for C_{filt}, to minimize distortion.
5. For best performance, consider using a 0.1% 20ppm/°C film resistor, or better, to minimize distortion.
6. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{filtx} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify the design you will need to select a different RC filter. Refer to *Introduction to SAR ADC Front-end Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select a fully-differential amplifier capable of driving the ADC:
   THS4551 – Low noise, precision, 150MHz, fully-differential amplifier
   - Wide input common-mode voltage:

$$V_{s-} - 0.1V < V_{cm} < V_{s+} - 1.3V$$

   - Linear output (requirement: 0V to 3.3V at each output):

$$V_{s-} + 0.22V < V_{out} < V_{s+} - 0.22V$$

2. Select a wide bandwidth operational amplifier:
   OPA320 – Precision, zero-crossover, 20MHz, RRIO, operational amplifier
   - Gain bandwidth product >12.5MHz (>5 times the sampling rate)
   - Input common-mode voltage (requirement: 0 - 3.3V):

$$V_{-} - 0.1V < V_{cm} < V_{+} + 0.1V$$

   - Linear output:

$$V_{-} + 0.03V < V_{out} < V_{+} - 0.03V$$

$$V_{-} + 0.2V < V_{out} < V_{+} - 0.2V$$

   - Combined worst-case linear range (calculated from supplies used with OPA320):

$$-0.1V < V_{out} < 4.8V$$

Note

The operational amplifier is used to protect the sensor from any charge kickbacks that occur when the ADC connects or disconnects the sampling capacitor. This amplifier may not be needed if the sensor has a high-output impedance. A negative rail is used for both the OPA320 and THS4551 based on the assumption that the sensor is operating with a negative rail; this also provides the highest performance from the ADC by providing the full scale input range.

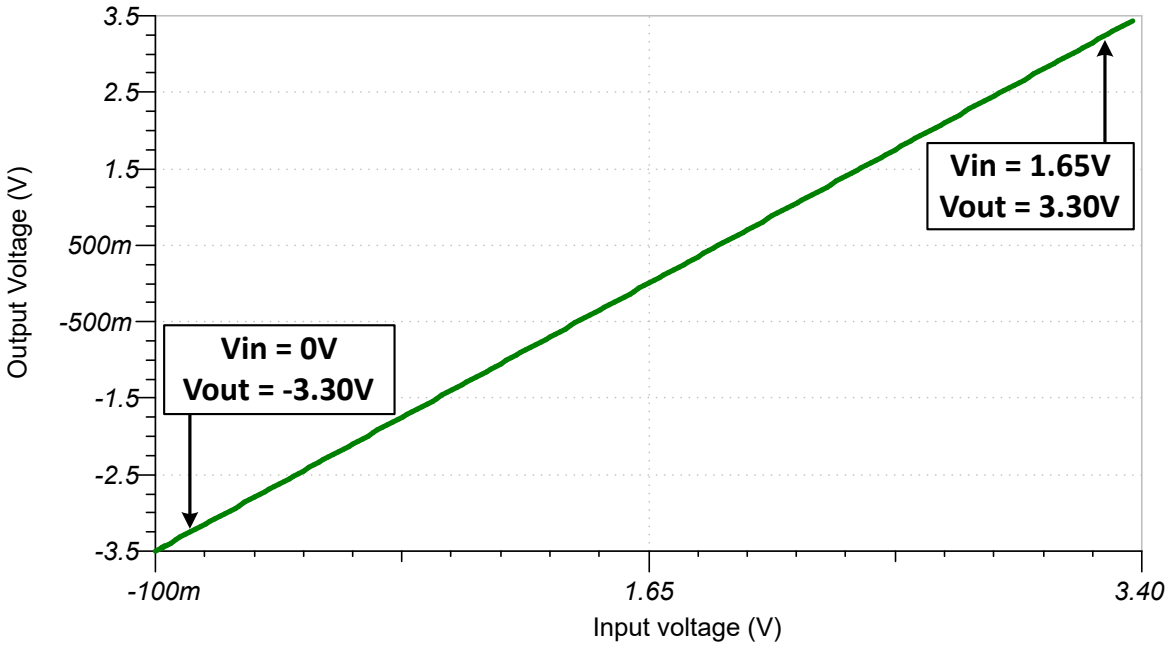
3. Select R_{fx} and R_{gx}
   - The combination of R_{fx} and R_{gx} sets the gain of the system. With an input range of 0V - 3.3V and an ADC full scale of ±3.3V, a gain of 2 was selected for this system.
   - The values of R_{fx} = 2k and R_{gx} = 1k were selected to both provide the desired gain as well as limit the current through the feedback network, thus minimizing power consumption of the system.
4. Select R_{sx}

- It is important to connect small resistors at the output of the amplifier, in this case 10Ω, to flatten the output impedance and improve stability of the system.

5. Select R_{filtx} and C_{filt} values for settling of 250-kHz input signal and sample rate of 2.5Msps:
   - *Refine the R_{filt} and C_{filt} Values* is a Precision Labs Video showing the methodology for selecting R_{filtx} and C_{filt}. The final value of 18.2Ω and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

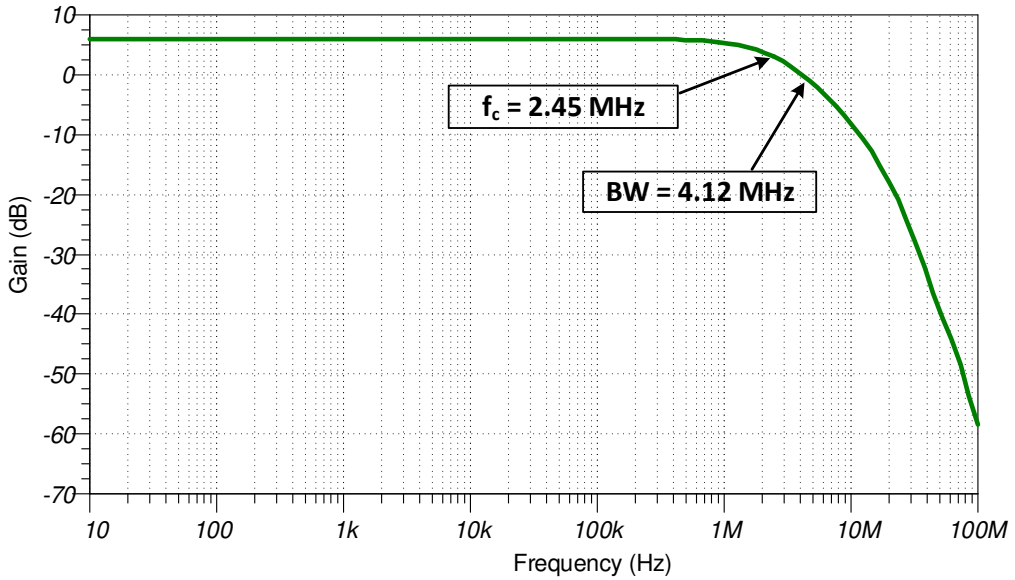
DC Transfer Characteristics

The following graph shows the simulated output for a 0 - 3.3V input. The analog front end has a linear output of ±3.3V which matches the full-scale range (FSR) of the ADC (with AVDD = 3.3V).



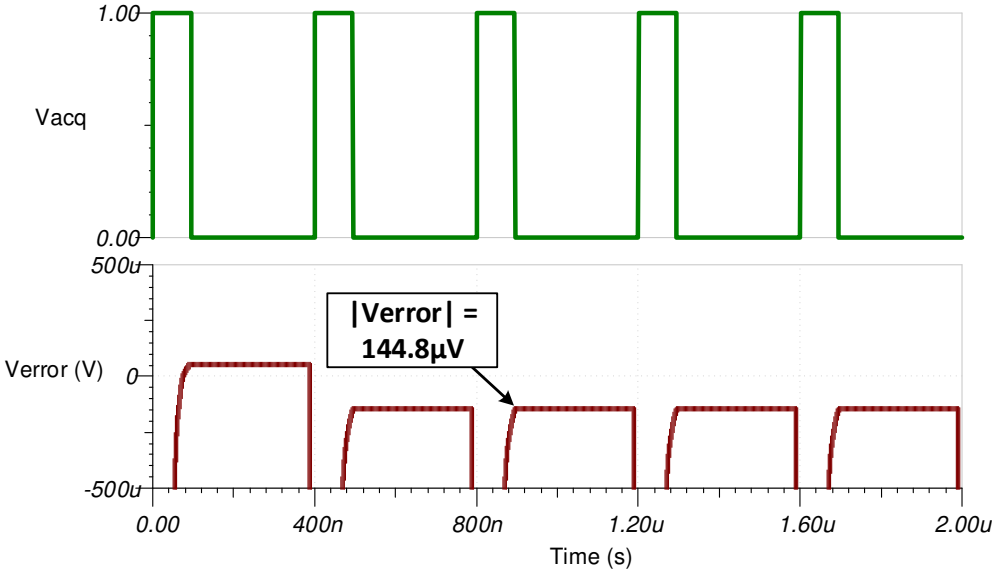
AC Transfer Characteristics

The bandwidth of the analog front end is simulated to be 4.12MHz at the gain of 0dB which is a linear gain of 1. This bandwidth allows the inputs of the ADC to adequately settle for a 250-ksps input signal.



Transient ADC Input Settling Simulation

The following simulation shows the ADC sample and hold capacitor settling for a 3.3-V DC input signal. This simulation shows that the analog front end is able to drive the ADC with a large step input (from 0V to 3.3V) so it settles to within ½ of an LSB (approximately 200µV) in the allotted acquisition time (95ns). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject, and follow the link at the end of this design to download these simulation files.



Noise Simulation

This section walks through a simplified noise calculation, providing a rough estimate to compare with the simulated result. The resistor noise is included in this calculation as it is a significant portion of the overall noise of the system. Note that the resistor noise can be reduced by using smaller value resistors, but at the expense of increased power consumption through the feedback network.

$$f_c = \frac{1}{2\times\pi\times R_{filt}\times C_{filt}} = \frac{1}{2\times\pi\times 2\,k\Omega\times 30pF} = 2.65MHz$$

$$E_n = e_{OPA320}\times\sqrt{2\times K_n\times f_c} = \left(7nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} = 20.2\mu V/\sqrt{Hz}$$

$$E_{n\_OPA320} = E_n\times Gain = 20.2\mu V/\sqrt{Hz}\times 2 = 40.4\mu V/\sqrt{Hz}$$

$$E_{n\_THS4551} = e_{nTHS4551}\times\sqrt{2\times K_n\times f_c} = \left(3.3nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} = 9.52\mu V/\sqrt{Hz}$$

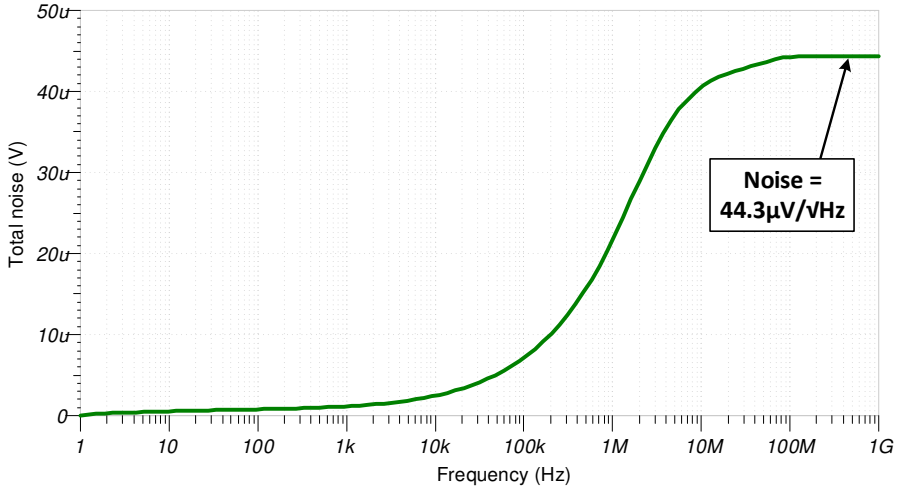
$$E_{Rg} = \frac{\sqrt{4\times k\times T\times R_g}}{1\times 10^{-9}}\times\frac{R_f}{R_g}\times\sqrt{2} = \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 1000}}{1\times 10^{-9}}\times\frac{2000}{1000}\times\sqrt{2} = 11.47\mu V/\sqrt{Hz}$$

$$E_{Rf} = \frac{\sqrt{4\times k\times T\times R_f}}{1\times 10^{-9}}\times\sqrt{2} = \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 2000}}{1\times 10^{-9}}\times\sqrt{2} = 8.11\mu V/\sqrt{Hz}$$

Total noise at output equation:

$$E_n = \sqrt{E_{nOPA320}{}^2 + E_{n\_THS4551}{}^2 + E_{Rg}{}^2 + E_{Rf}{}^2} = \sqrt{40.4^2 + 9.52^2 + 11.47^2 + 8.11^2} = 43.8\mu V/\sqrt{Hz}$$

Note that calculated and simulated match well. Refer to the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7057	14 bit, 2.5 Msps, fully-differential input, SPI, 2.25mm^2 package	14-Bit, 2.5MSPS, Differential Input, Small-Size Low-Power SAR ADC	Precision ADCs
THS4551	150MHz, 3.3nV/√Hz input voltage noise, fully-differential amplifier	Low Noise, Precision, 150MHz, Fully Differential Amplifier	Fully differential amplifiers
OPA320	Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, operational amplifier	Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, CMOS operational amplifier	Operational amplifiers (op amps)

Note

The ADS7057 uses the AVDD as the reference input. Use a high-PSRR LDO, such as the TPS7A47, as the power supply.

Link to Key files (TINA):

Texas Instruments, design files for SBAA264, SBAC188 software support

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (January 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page	1

Trademarks

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Analog Engineer's Circuit

Single-ended-to-differential circuit using an op amp and fully-differential amplifier (FDA) for bipolar signals

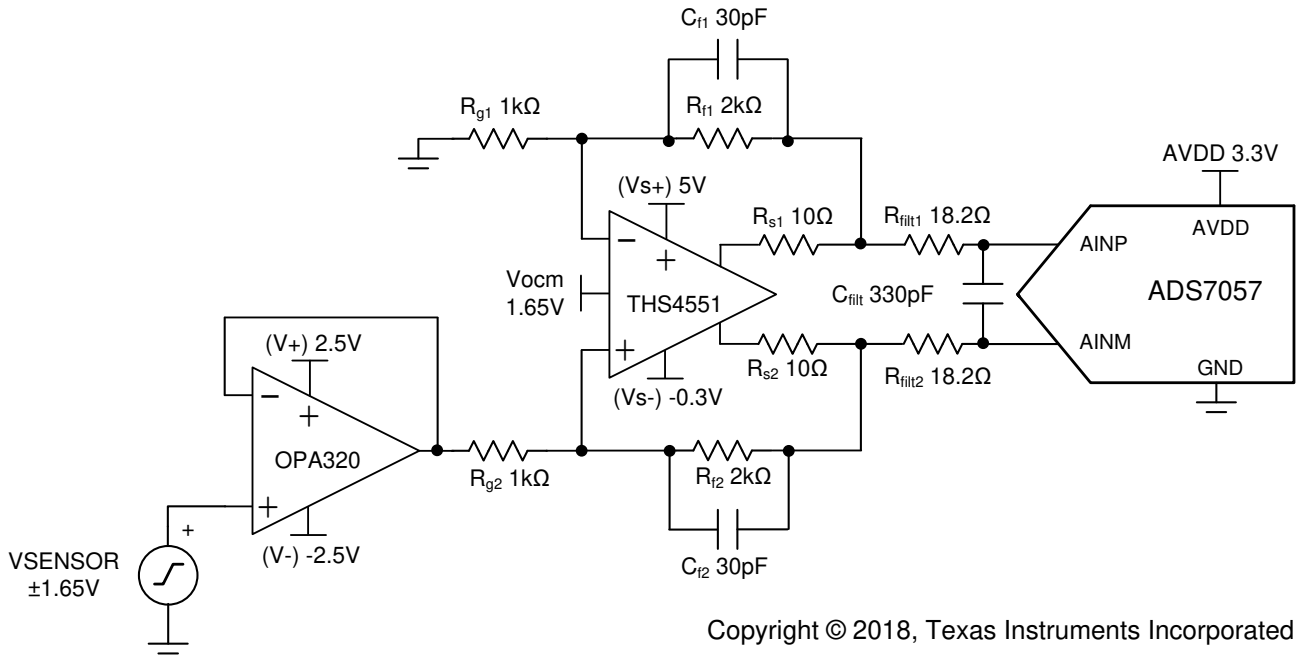
Evan Sawyer

Input	ADC Input	Digital Output ADS7057
V_{in} Min = –3.3V	AINP = 0V AINM = 3.3V	2000_H 8192_{10}
V_{in} Max = 3.3V	AINP = 3.3V AINM = 0V	$1FFF_H$ 8191_{10}

Power Supplies		
AVDD	**GND**	**DVDD**
3.3V	0V	1.8V

Design Description

This design is intended to demonstrate how to convert a bipolar, single-ended signal into a unipolar, fully-differential signal and drive a differential ADC (for more information on these and other signal types, please refer to the *TI Precision Labs* training titled *SAR ADC Input Types*). Compared to a single-ended device, a fully-differential ADC has twice the dynamic range which improves the AC performance of the converter. Many common systems, for example *Sonar Receivers*, *Flow Meters*, and *Motor Controls*, benefit from the higher performance of a differential ADC. The equations and explanation of component selection in this design can be customized based on system specifications and needs. For more information on a similar design using a unipolar input signal, see the cookbook circuit titled *Single-Ended to Differential Signal Conversion for Unipolar Inputs*.



Specifications

Specification	Calculated	Simulated
Transient ADC Input Settling (at 250ksps)	< 0.5 · LSB = 201µV	134.7µV
Conditioned Signal Range (at 250ksps)	> 99% ADC FSR = > 6.53V	6.60V
Noise	43.8µV / √Hz	44.3µV / √Hz

Design Notes

1. The ADS7057 was selected because of the throughput (2.5Msps), size (2.25mm²) and low-latency (successive approximation register, or SAR, architecture).
2. Determine the linear range of the fully-differential amplifier (ADC driver) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
3. Determine the linear range of the op amp (signal conditioning) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
4. Select COG (NPO) capacitors for C_{filt}, to minimize distortion.
5. For best performance, consider using a 0.1% 20ppm/°C film resistor, or better, to minimize distortion.
6. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{filtx} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to *Introduction to SAR ADC Front-end Component Selection* (a *TI Precision Labs* training video) for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select a fully-differential amplifier capable of driving the ADC:
   THS4551 – Low noise, precision, 150MHz, fully-differential amplifier
   - Wide input common-mode voltage:

   $$V_{s-} - 0.1V < V_{cm} < V_{s+} - 1.3V$$

   - Linear output (requirement: 0V to 3.3V at each output):

   $$V_{s-} + 0.22V < V_{out} < V_{s+} - 0.22V$$

2. Select a wide bandwidth operational amplifier:
   OPA320 – Precision, zero-crossover, 20MHz, RRIO, operational amplifier
   - Gain bandwidth product > 12.5MHz (> 5 times the sampling rate)
   - Input common-mode voltage (requirement: ±1.65V):

   $$V_{-} - 0.1V < V_{cm} < V_{+} + 0.1V$$

   - Linear output:

   $$V_{-} + 0.03V < V_{out} < V_{+} - 0.03V$$

   $$V_{-} + 0.2V < V_{out} < V_{+} - 0.2V$$

   - Combined worst-case linear range (calculated from supplies used with OPA320):

   $$-2.3V < V_{out} < 2.3V$$

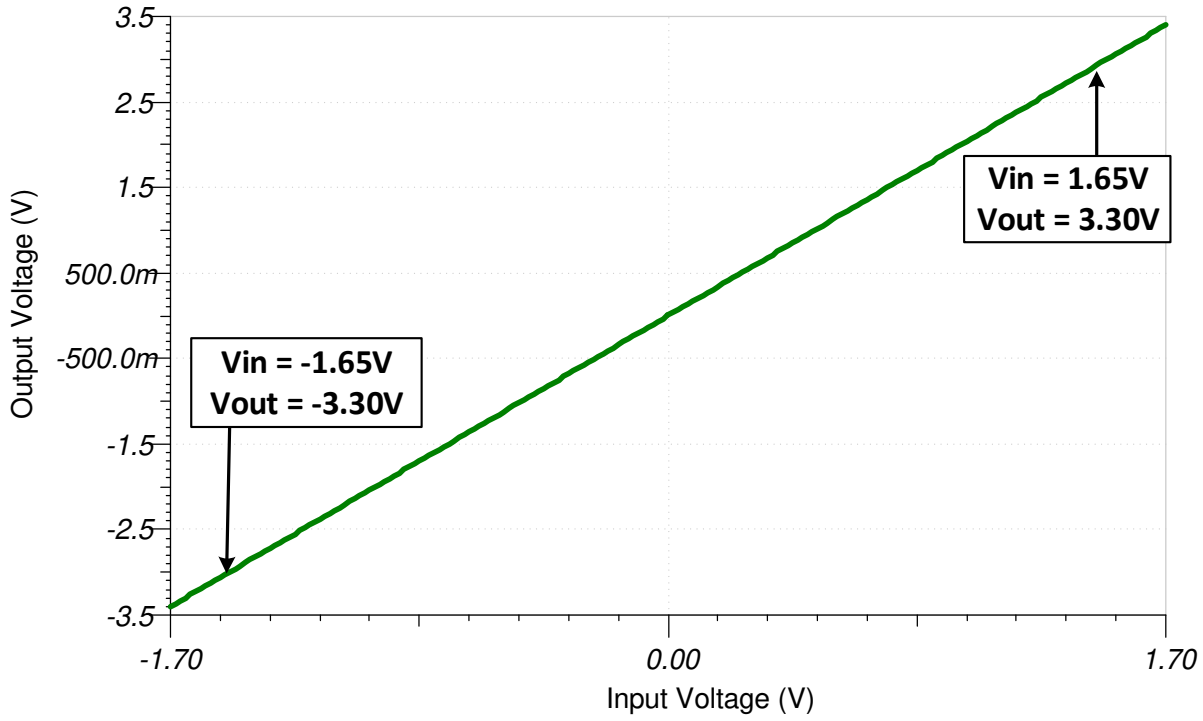
Note

The operational amplifier is used to protect the sensor from any charge kickbacks that occur when the ADC connects or disconnects the sampling capacitor. There is a possibility that this amplifier is not needed if the sensor has a high output impedance. A negative rail is used for both the OPA320 and THS4551 based on the assumption that the sensor is operating with a negative rail. This also provides the highest performance from the ADC by providing the full scale input range.

3. Select R_{fx} and R_{gx}
   - The combination of R_{fx} and R_{gx} sets the gain of the system. With an input range of ±1.65V and an ADC full scale of ±3.3V, a gain of 2 was selected for this system.
   - The values of R_{fx} = 2k and R_{gx} = 1k were selected to both provide the desired gain as well as limit the current through the feedback network, thus minimizing power consumption of the system.
4. Select R_{sx}
   - Connecting small resistors at the output of the amplifier is important and, in this case 10Ω, to flatten the output impedance and improve stability of the system.
5. Select R_{filtx} and C_{filt} values for settling of 250kHz input signal and sample rate of 2.5Msps:
   - *Refine the R_{filt} and C_{filt} Values* is a *TI Precision Labs* video showing the methodology for selecting R_{filtx} and C_{filt}. The final value of 18.2Ω and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

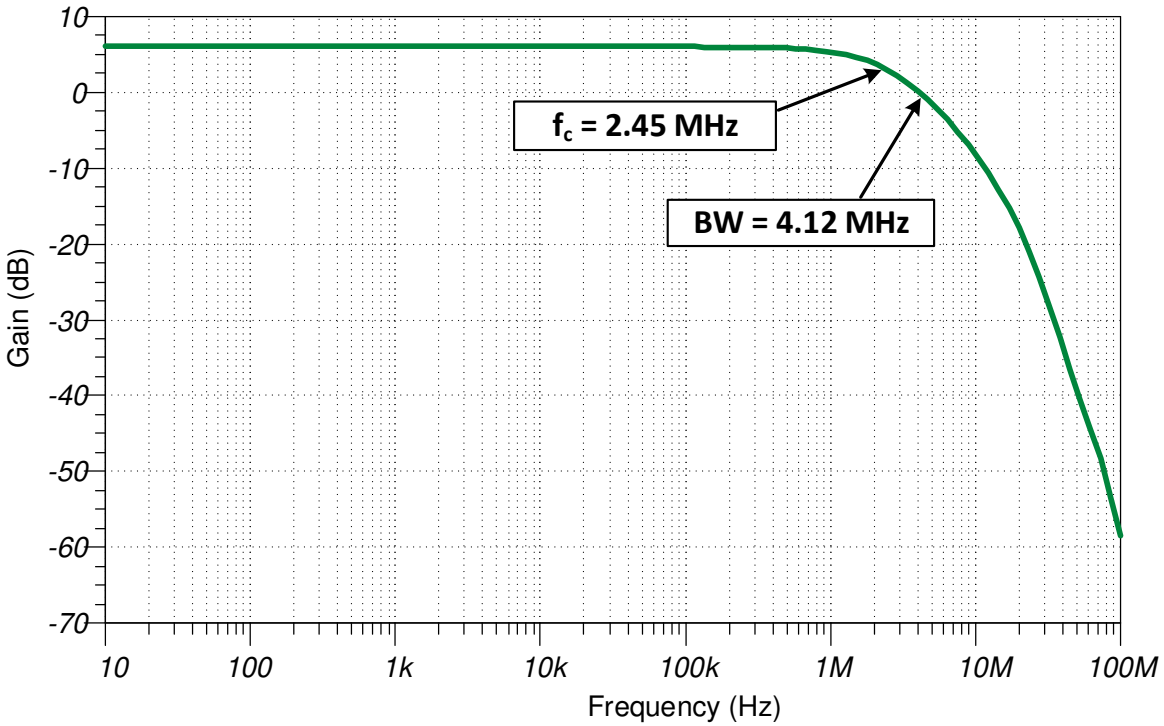
DC Transfer Characteristics

The following graph shows the simulated output for a ±1.65-V input. The analog front end has a linear output of ±3.3V which matches the full-scale range (FSR) of the ADC (with AVDD = 3.3V).



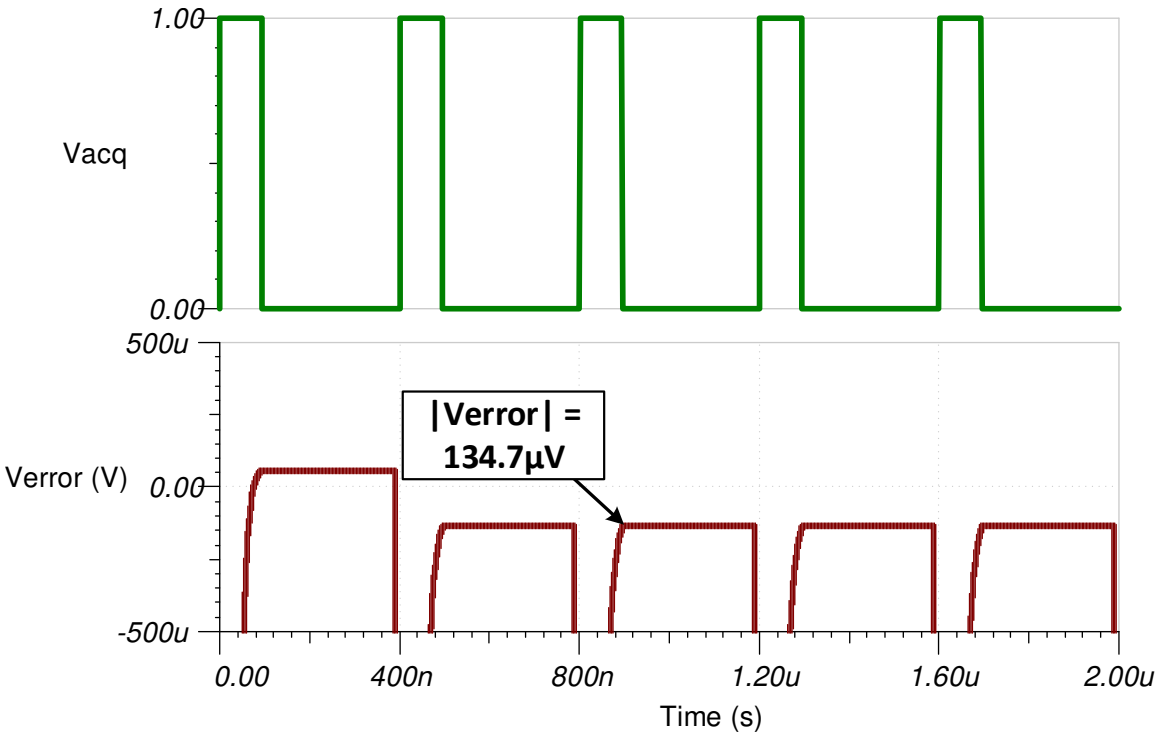
AC Transfer Characteristics

The bandwidth of the analog front end is simulated to be 4.12MHz at the gain of 0dB which is a linear gain of 1. This bandwidth allows the inputs of the ADC to adequately settle for a 250-ksps input signal.



Transient ADC Input Settling Simulation

The following simulation shows the ADC sample and hold capacitor settling for a 3.3V DC input signal. This simulation shows that the analog front end is able to drive the ADC with a large step input (from 0V to 3.3V) so the ADC settles to within ½ of an LSB (approximately 200µV) in the allotted acquisition time (95ns). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject, and follow the link at the end of this design to download these simulation files.



Noise Simulation

This section details through a simplified noise calculation, providing a rough estimate to compare with the simulated result. The resistor noise is included in this calculation as the resistor noise is a significant portion of the overall noise of the system. Note that the resistor noise can be reduced by using smaller value resistors, but at the expense of increased power consumption through the feedback network.

$$f_c = \frac{1}{2\times\pi\times R_{filt}\times C_{filt}} = \frac{1}{2\times\pi\times 2\,k\Omega\times 30pF} = 2.65MHz$$

$$E_n = e_{OPA320}\times\sqrt{2\times K_n\times f_c} = \left(7nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} = 20.2\mu V/\sqrt{Hz}$$

$$E_{n\_OPA320} = E_n\times Gain = 20.2\mu V/\sqrt{Hz}\times 2 = 40.4\mu V/\sqrt{Hz}$$

$$E_{n\_THS4551} = e_{nTHS4551}\times\sqrt{2\times K_n\times f_c} = \left(3.3nV/\sqrt{Hz}\right)\times\sqrt{2\times 1.57\times 2.65MHz} = 9.52\mu V/\sqrt{Hz}$$

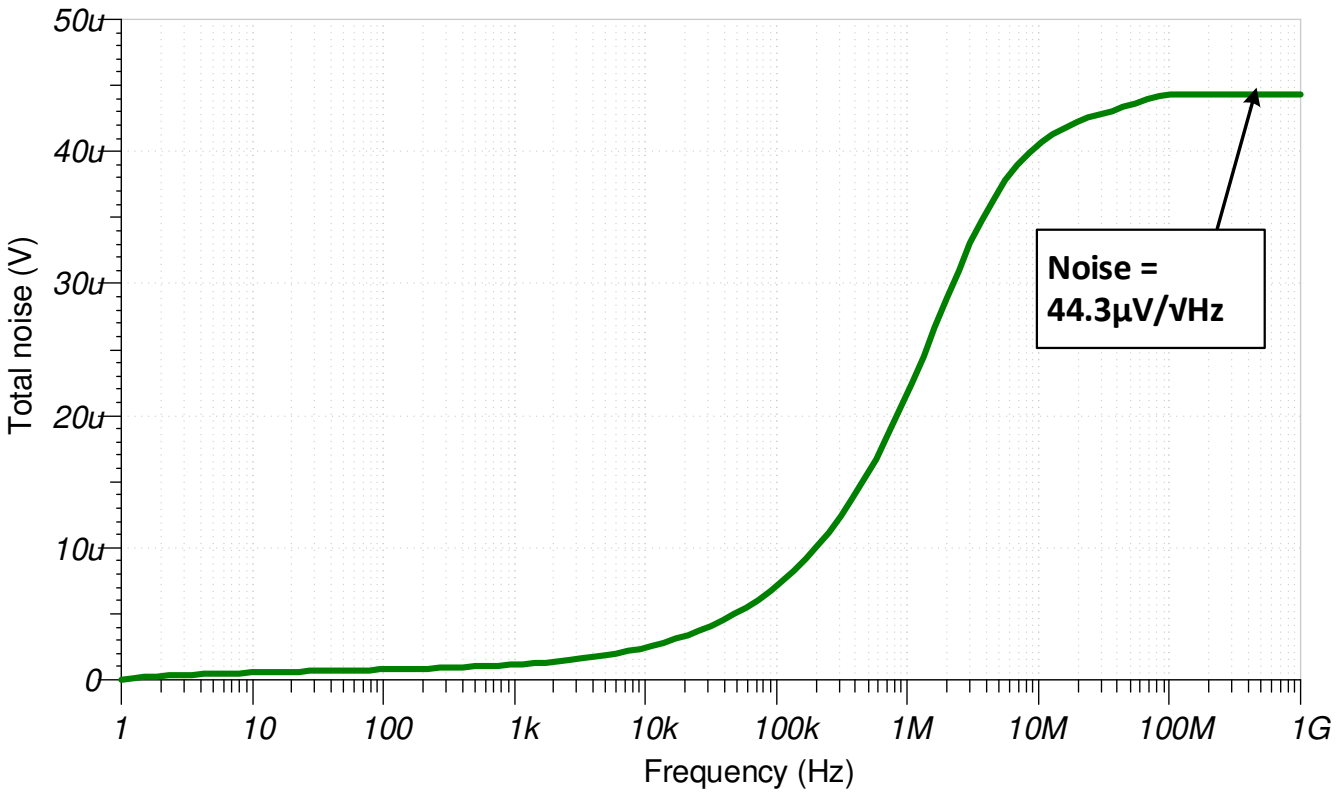
$$E_{Rg} = \frac{\sqrt{4\times k\times T\times R_g}}{1\times 10^{-9}}\times\frac{R_f}{R_g}\times\sqrt{2} = \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 1000}}{1\times 10^{-9}}\times\frac{2000}{1000}\times\sqrt{2} = 11.47\mu V/\sqrt{Hz}$$

$$E_{Rf} = \frac{\sqrt{4\times k\times T\times R_f}}{1\times 10^{-9}}\times\sqrt{2} = \frac{\sqrt{4\times 1.38\times 10^{-23}\times(273.15+25)\times 2000}}{1\times 10^{-9}}\times\sqrt{2} = 8.11\mu V/\sqrt{Hz}$$

Total noise at output equation:

$$E_n = \sqrt{E_{nOPA320}{}^2 + E_{n\_THS4551}{}^2 + E_{Rg}{}^2 + E_{Rf}{}^2} = \sqrt{40.4^2 + 9.52^2 + 11.47^2 + 8.11^2} = 43.8\mu V/\sqrt{Hz}$$

Note that calculated and simulated match well. Refer to the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7057	*14 bit, 2.5 Msps, fully-differential input, SPI, 2.25mm^2 package*	www.ti.com/product/ADS7057	www.ti.com/adcs
THS4551	*150MHz, 3.3nV/√Hz input voltage noise, fully-differential amplifier*	www.ti.com/product/THS4551	www.ti.com/opamp
OPA320	*Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, operational amplifier*	www.ti.com/product/OPA320	www.ti.com/opamp

Note

The ADS7057 uses the AVDD as the reference input. Use a high-PSRR LDO, such as the TPS7A47, as the power supply.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to key files (TINA):

Design files for this circuit – http://www.ti.com/lit/zip/sbac181.

Link to Related Cookbooks

Single-Ended to Differential Signal Conversion for Unipolar Input

Trademarks

All trademarks are the property of their respective owners.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (January 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page	1

Analog Engineer's Circuit

Single-Ended to Differential Using a Two Op-Amp Circuit

Bryan McKay, Art Kay

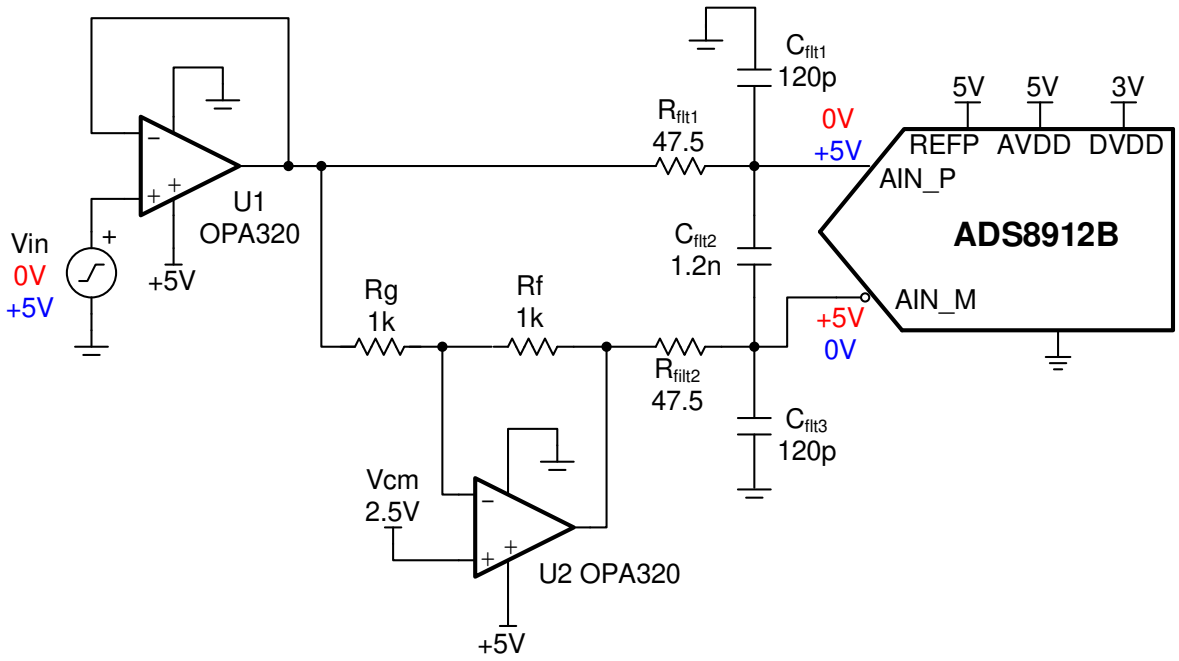
Input	ADC Differential Input (Vdif)	ADC Common-Mode Input (Vcm)	Digital Output ADS9110
0V	–5V	2.5V	20000_H
5V	+5V	2.5V	$1FFFF_H$

Power Supplies

V+ (op amp)	AVDD	DVDD	REFP
5V	5V	3V	5V

Design Description

This circuit uses two OPA320 op amps to perform a single-ended to differential conversion for driving the ADS8912B fully-differential ADC. Another approach to solve this problem uses a fully-differential amplifier (FDA). See *Single-Ended to Differential Conversion Using an Op Amp and FDA for Unipolar Signals* for the FDA example. Since there are many thousands of different types of op amps available, finding an op amp the meets your specific requirements may be easer than finding an fully-differential amplifier. Most FDAs, for example, do not have as good swing to the rail, offset, bias current, and drift as many precision op amps have. On the other hand, the op-amp approach has an asymmetrical group delay in the inverting and non-inverting paths. Furthermore, FDA amplifiers often have better distortion and ADC drive characteristics. In general, the FDA approach will achieve best SNR and THD, and the op-amp approach will achieve best DC characteristics. Nevertheless, the specific op amp or FDA will impact the comparison of the two typologies.



Specifications

Specification	Goal	Calculated	Simulated
Transient ADC Input Settling (1MSPS)	< 0.5LSB = 19.1µV	NA	5µV
Input Output Range	NA	NA	$0.1 < V_{IN} < 4.9V$ $–4.8V < V_{OUT} < 4.8V$
Noise	NA	$30.5µV_{RMS}$	$28.4µV_{RMS}$

Design Notes

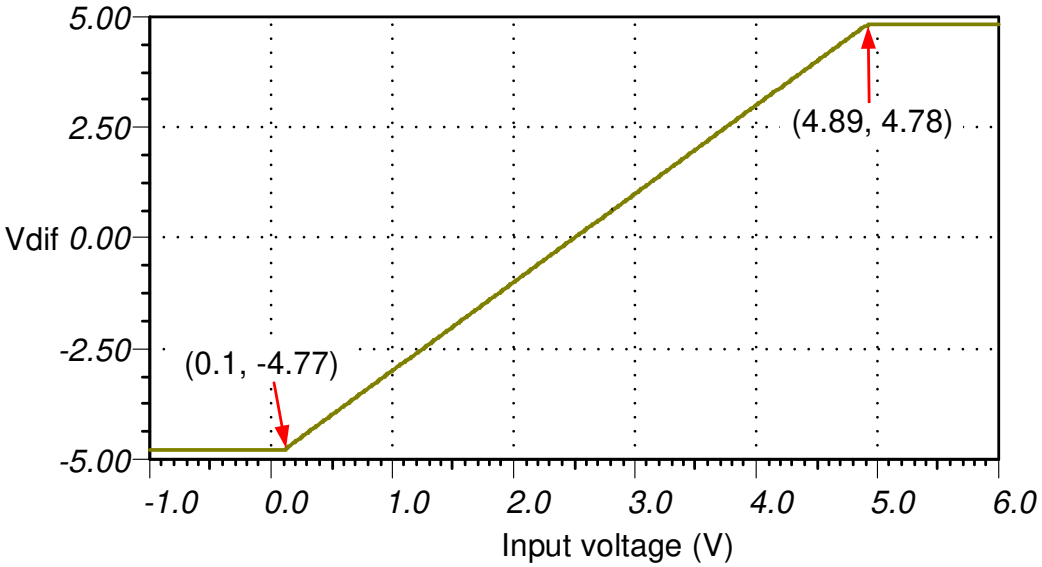
1. Use 0.1% resistors for R1 and Rg to minimize gain error and drift on U2.
2. Select COG (NPO) capacitors for C_{filt1}, C_{filt2}, and C_{filt3} to minimize distortion.
3. The *Precision labs series: Analog-to-digital converters (ADCs)*training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify this design you will need to select a different RC filter. See the *Introduction to SAR ADC Front-End Component Selection* training video for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select an op amp to meet the system requirements. Key specifications to consider follow:
   - Swing to rail - For 5-V supply rails it is common to use a rail-to-rail zero crossover distortion device (for example, OPA320, OPA325, and OPA365).
   - Offset voltage and Drift - One of the advantages of this circuit over the FDA approach is that some op-amps can have very good DC performance.
   - Bandwidth and quiescent current - Another advantage of this circuit over the FDA approach is that a wide range of op-amp bandwidth and related quiescent currents are available. For lower sampling rate a low bandwidth low current op amp may be a good choice.
2. Choose Rg and Rf to minimize noise. The gain of this circuit is always 1, so Rg = Rf. The main consideration here is to minimize noise while keeping the load resistance reasonable. Set the resistor noise to be roughly ⅓ of the amplifier noise. In this example Rf = Rg = 1kΩ gives a noise of 2.8nV/$\sqrt{\text{Hz}}$ which is approximately ⅓ of the 7nV/$\sqrt{\text{Hz}}$ op-amp noise. Also, the maximum load current is 2.5mA (5V ÷ 2kΩ = 2.5mA) which is low compared to the op-amp short-circuit limit (65mA).
3. Find R_{filt} and C_{filt} to allow for settling at 1kSPS. See *Refine the Rfilt and Cfilt Values* for the algorithm to select R_{filt} and C_{filt}. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

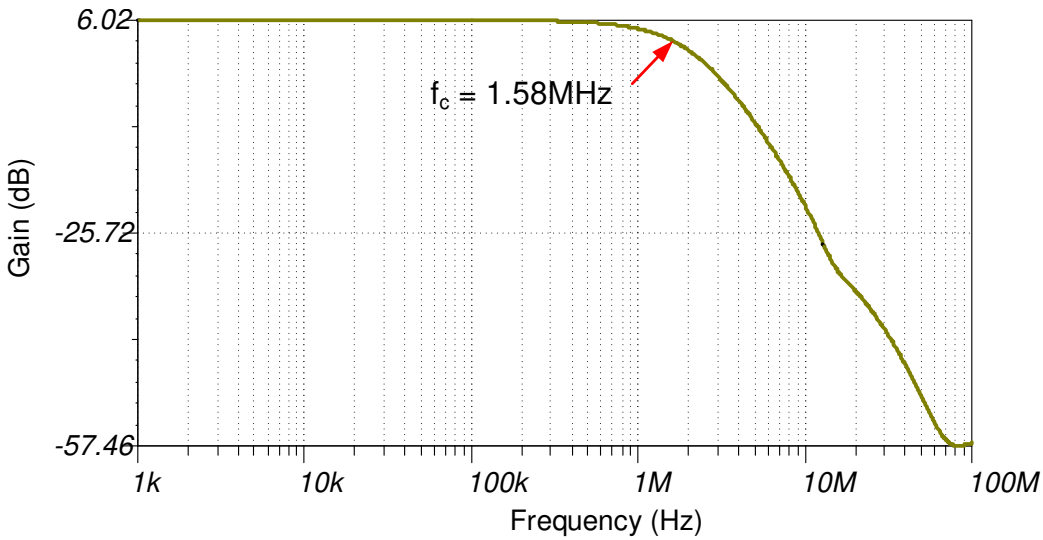
The following graph shows the DC transfer characteristics for this circuit (0-V to 5-V single-ended input, –5-V to +5-V fully-differential output). Note that the linear range is limited to about 0.1V from both supply rails (Vin linear range approximately 0.1V to 4.9V). The limitation is from the amplifier output swing limit. For improved linear swing the negative and positive supply on the amplifiers would need to be adjusted. See *Low-Power Sensor Measurements: 3.3-V, 1-ksps, 12-bit, Single-Ended, Dual-Supply Circuit* for an example on how to do this.



AC Transfer Characteristics

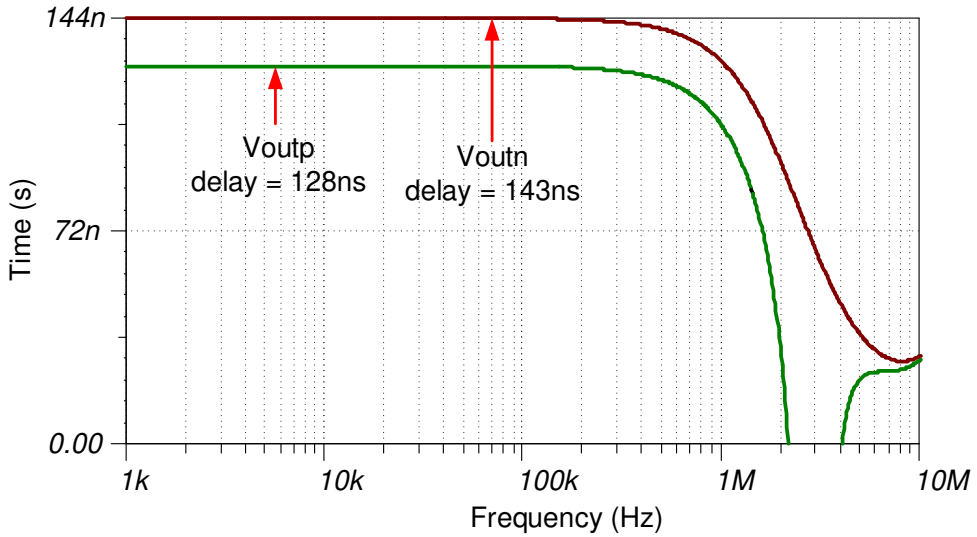
In this case the bandwidth limitation is primary set by the R_{filt}, C_{filt} values. The amplifier closed loop bandwidth can also impact the overall bandwidth. Note the bandwidth of U2 is half the bandwidth of U1 as its noise gain is two (BW_{U2} = GBW/G_n = 20MHz/2 = 10MHz).

$$f_c = \frac{1}{2\pi R \cdot C} = \frac{1}{2\pi(2 \cdot 47.5\Omega) \cdot 1.2nF} = 1.4MHz$$



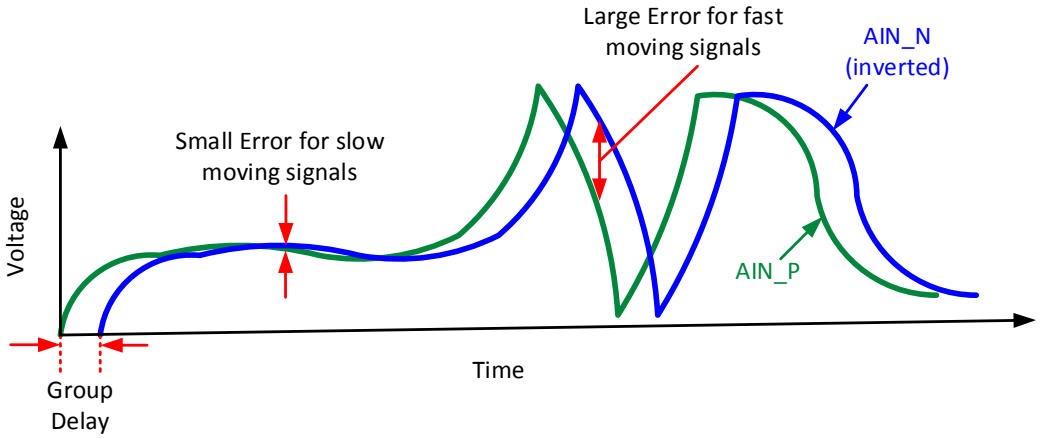
Group Delay (Frequency Domain)

Group delay is the time delay between the applied input signal and the output signal. All amplifiers and filters will have a group delay. Group delay is highlighted for this circuit because the inverting and non-inverting path both have different group delays. This can create distortion for higher frequency signals. See the group delay in time domain plot for additional detail.



Group Delay (Time Domain)

The following graph shows qualitatively how group delay can effect time domain signals. The errors in this plot are exaggerated to emphasize the effect of group delay. The green signal represents the output on AIN_P and the blue signal represents the inverted output on AIN_N. Ideally, the two signals should track, but the group delay shifts the blue signal to the right. Notice that when signals are moving slowly the error is relatively small and when they are moving rapidly the error is larger. Thus, low frequency signals will have good distortion, and higher frequency signals will have degraded distortion. SPICE does not simulate THD, so for quantitative values measurement is required. However, if the input signal period more than 1,000 times larger than the group delay between the channels than this effect can generally be neglected.



Noise Simulation

The following noise calculation considers the amplifier and resistor noise. Note that the noise from U1 is inverted by U2 and added at the differential output. Since this noise is directly correlated, it adds directly as opposed to root sum square addition usually used for noise sources. Also note that the output filter is approximated as first order but it is a more complex filter. The calculated noise compares well to the simulated noise (calculated = 30.5μV_{RMS}, simulated = 28.4μV_{RMS}).

$$e_{nU1} = e_{n320} + e_{n320} = 7\,nV/\sqrt{Hz} + 7\,nV/\sqrt{Hz} = 14\,nV/\sqrt{Hz}$$ Note these two sources are correlated

$$R_{eq} = \frac{R_f \cdot R_g}{R_f + R_g} = \frac{1k\Omega \cdot 1k\Omega}{1k\Omega + 1k\Omega} = 500\Omega$$

$$e_{nReq} = \sqrt{4K_n \cdot T_K \cdot R_{eq}} = \sqrt{4(1.38 \cdot 10^{-23}\,J/K) \cdot (298.15) \cdot (500\Omega)} = 2.87\,nV/\sqrt{Hz}$$

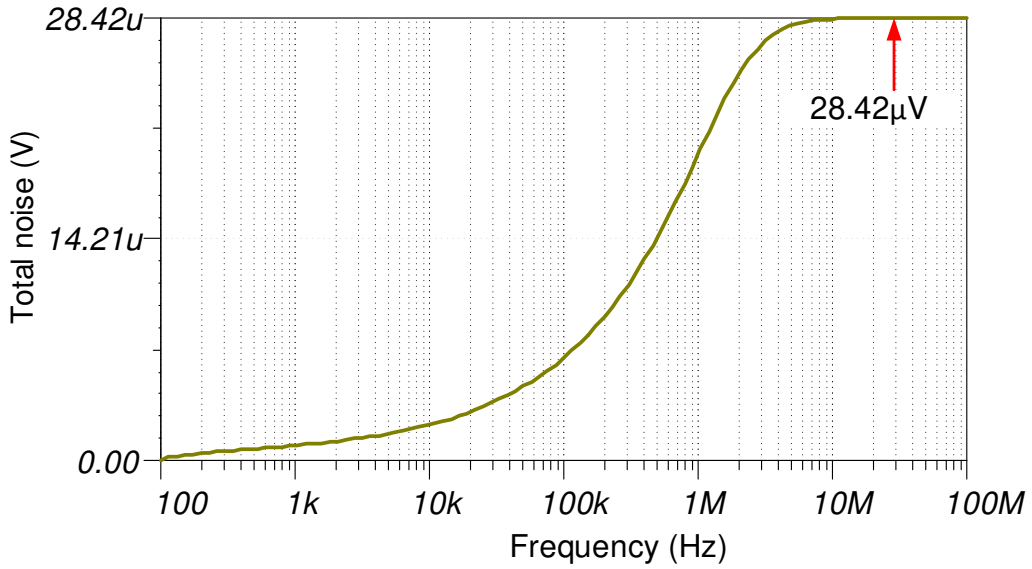
$$e_{nU2} = \sqrt{\left(e_{nReq} \cdot G_n\right)^2 + \left(e_{n320} \cdot G_n\right)^2} = \sqrt{\left(2.87\,nV/\sqrt{Hz} \cdot 2\right)^2 + \left(7\,nV/\sqrt{Hz} \cdot 2\right)^2} = 15.1nV/\sqrt{Hz}$$

$$e_{nT} = \sqrt{\left(e_{nU1}\right)^2 + \left(e_{nU2}\right)^2} = \sqrt{\left(14\,nV/\sqrt{Hz}\right)^2 + \left(15.1nV/\sqrt{Hz}\right)^2} = 20.6\,nV/\sqrt{Hz}$$

$$f_c = \frac{1}{2\pi R \cdot C} = \frac{1}{2\pi(2 \cdot 47.5\Omega) \cdot 1.2nF} = 1.4MHz$$

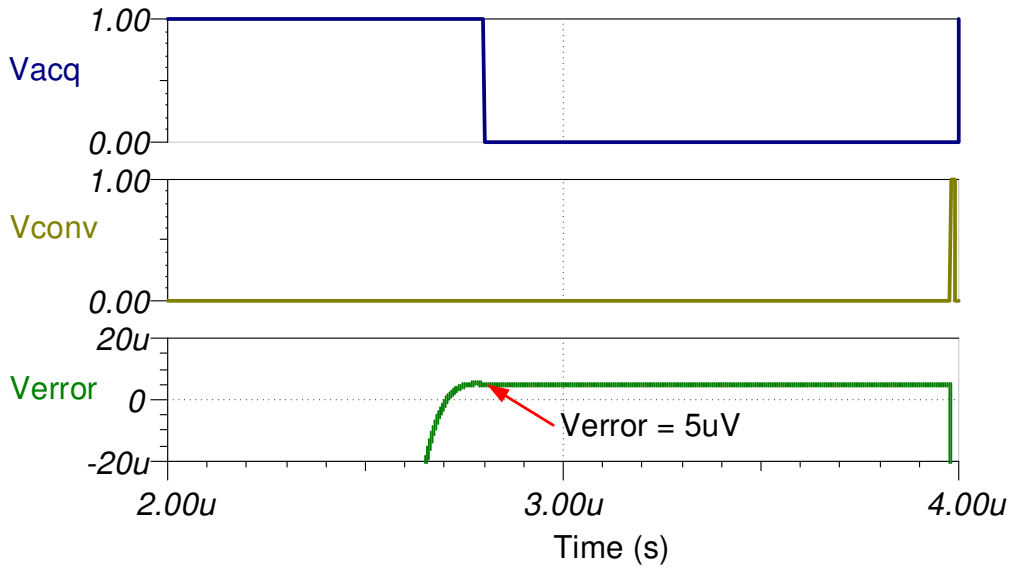
$$E_{nT} = e_{nT} \cdot \sqrt{1.57 \cdot f_c} = 20.6\,nV/\sqrt{Hz} \cdot \sqrt{1.57 \cdot 1.4MHz} = 30.5\mu V_{RMS}$$

The calculated noise compares well to the simulated noise (calculated = 30.5μV_{RMS}, simulated = 28.4μV_{RMS}). See *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a full scale DC input signal at 500kSPS. This type of simulation shows that the sample and hold kickback circuit is properly selected. See *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8912	18-bit resolution, 500-kSPS sample rate, integrated reference buffer, fully-differential input, Vref input range 2.5V to 5V.	18-Bit, 500kSPS, 1-Ch SAR ADC with Internal VREF Buffer, Internal LDO and Enhanced SPI Interface	Precision ADCs
OPA320	20-MHz bandwidth, Rail-to-Rail with zero crossover distortion, VosMax = 150µV, VosDriftMax = 5µV/C, en = 7 nV/√Hz	Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, CMOS operational amplifier	Precision op amps (Vos < 1mV)

Link to Key Files

Texas Instruments, source files for SBAA265, support software

Trademarks

All trademarks are the property of their respective owners.

Analog Engineer's Circuit

True Differential, 4 × 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit

Luis Chioye

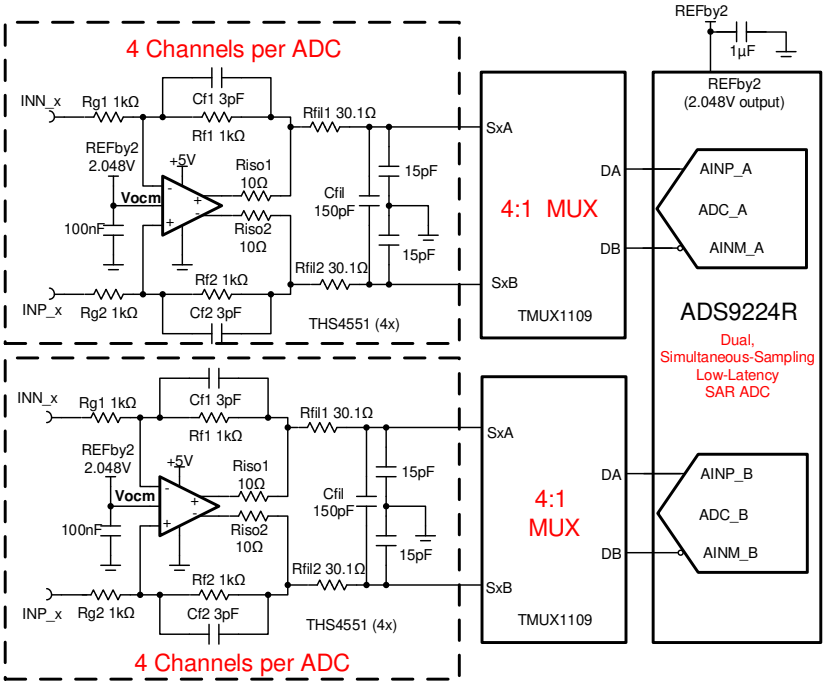
Input (THS4551 Inputs)	ADC Input (THS4551 Output)	Digital Output ADS7042
VinP = +0.23V, VinN = +3.866V, VinMin(Dif) = -3.636V	VoutP = +0.23V, VoutN = 3.866V, Vout(Dif) = -3.636V	$8E60_H$ -29088_{10}
VinP = +3.866V, VinN =0.23V, VinMax(Dif) = +3.636V	VoutP = 3.866V, VoutN = +0.23V, Vout(Dif) = +3.636V	$71A0_H$ $+29088_{10}$

Power Supplies

Vcc	Vee	Vref	Vocm
5	0V	4.096V	2.048V

Design Description

This dual simultaneous-sampling SAR ADC and 4 × 2 channel multiplexed analog front end data acquisition solution can measure differential voltage signals in the range of ±3.866V supporting ADC sampling rates up to 3-MSPS (or effective sampling rate of 750-kSPS per channel) with 16-B resolution. The circuit consists of a dual simultaneous sampling SAR ADC, with each SAR ADC connected to two 4:1 (2x) multiplexers, providing 4 differential input channels per ADC. Eight *Fully Differential Amplifiers* (FDAs) drive the multiplexed SAR ADC inputs. This circuit is applicable in the accurate measurement of dual simultaneous signals in applications such as *Optical Modules* and *Analog Input Modules.* It also can be used in motor drive applications such as *Servo Drive Control Module, Servo Drive Position Feedback,* and *Servo Drive Position Sensor.*



Specifications

Specification	Goal	Calculated	Simulated
Dual ADC Sampling Speed	3Msps	3Msps	3Msps
Sampling Rate per Channel (dual, simultaneous)	750kSPS (3MSPS / 4)	750kSPS (3-MSPS / 4)	750-kSPS (3MSPS / 4)
Transient ADC Input Settling	<< 1 LSB << 125µV	NA	20µV
Noise (at ADC Input)	$50\mu V_{rms}$	$55.9\mu V_{rms}$	$51.1\mu V_{rms}$

Design Notes

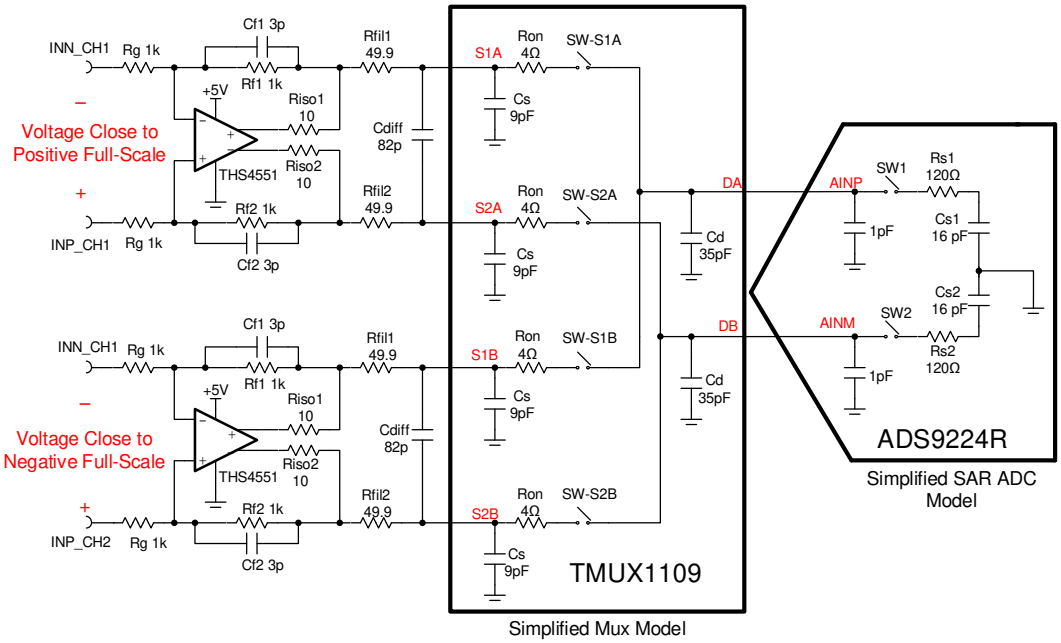
1. The ADS9224R was selected because of the dual simultaneous sampling and high throughput (3-MSPS) requirements.
2. The TMUX1109 4:1 (2x) multiplexer was selected to support 4-channel differential inputs for each ADC.
3. Find ADC full-scale range, resolution and common-mode range specifications. This is covered in the component selection.
4. Determine the linear range of the FDA (THS4551) based on common-mode and output swing specification. This is covered in the component selection section.
5. Select COG capacitors for all filter capacitors at the ADC input to minimize distortion.
6. Select the FDA gain resistors RF1,2 , RG1,2. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift and to minimize distortion.
7. *Introduction to SAR ADC Front-End Component Selection* covers the methods for selecting the charge bucket circuit Rfil1, Rfil1 and Cfil. These component values are dependent on the amplifier bandwidth, data converter sampling rare, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected.
8. The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling, and multiplexer charge injection and provides the common-mode level shifting to the voltage range of the SAR ADC.

Component Selection

1. Find ADC full-scale input range. In this circuit, ADS9224 internal V_REF= 2.5V
   $ADC_{Full-Scale\ Range} = (\pm 1.6384 V/V) \cdot V_{REF} = \pm 4.096 V$ from ADS9224R datasheet
2. Find required ADC common-mode voltage 2.
   $V_{CM} = \frac{+ADC_{Full-Scale\ Range}}{2} = +2.048 V$ from ADS9224R datasheet
   Use REFby2 Output pin of ADS9224R to connect to FDA $(THS4551)$ VCOM = 2.048V
3. Find FDA absolute output voltage range for linear operation:
   $0.23V < V_{out} < 4.77V$ from THS4551 output low/high specification for linear operation
4. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit:
   $V_{outMin} = \frac{V_{outDifMin}}{2} + V_{cm}$
   $V_{outMax} = \frac{V_{outDifMax}}{2} + V_{cm}$
   Rearrange the equations and solve for $V_{outDifMin}$ and $V_{outDifMax}$. Find maximum differential output voltage range based on worst case:
   $V_{outDifMax} = 2 \cdot V_{outMax} - 2 \cdot V_{cm} = 2 \cdot (4.096V) - 2 \cdot (2.048V) = 4.096V$
   $V_{outDifMin} = 2 \cdot V_{outMin} - 2 \cdot V_{cm} = 2 \cdot (0.23V) - 2 \cdot (2.048V) = -3.636V$
   Based on combined worst case, choose $V_{outDifMin}$ = -3.636V and $V_{outDifMax}$ = +3.636V
5. Set FDA gain to 1 V/V
   $Gain_{FDA} = \frac{R_f}{R_g} = \frac{1.00 k\Omega}{1.00 k\Omega} = 1 V/V$
6. Select the minimum charge kickback capacitor filter to optimize circuit for fastest settling.
   $C_{sh} = 16 pF$ internal sample-and-hold capacitor from ADS9224R datasheet
   Select a capacitor $10\times$ larger than $C_{fil} = 150 pF$
7. Optimize RC charge kickback filter resistors R_{fil1}, R_{fil2} and feedback capacitors C_{f1}, C_{f2} for both settling and stability using TINA simulations. This is covered in the transient settling optimization and stability simulation sections.

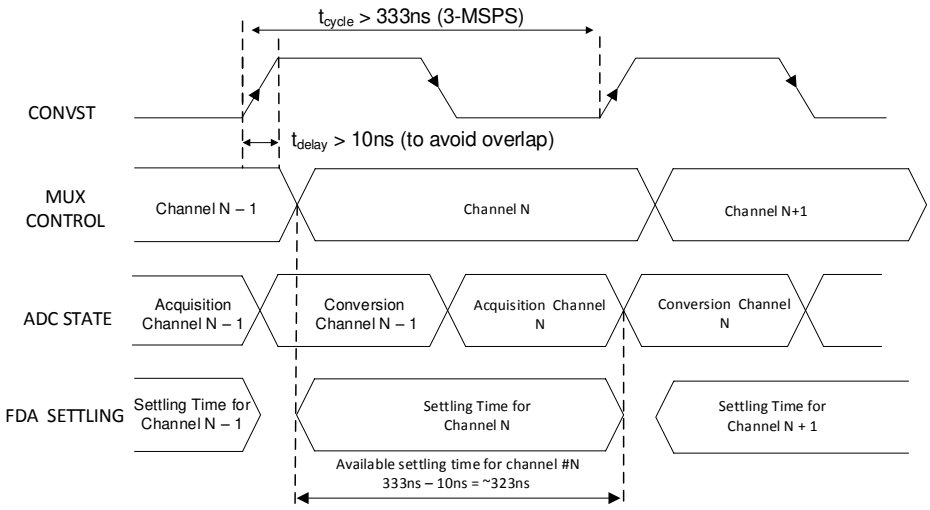
Transient Settling Optimization

TINA simulation is used to optimize the RC kickback filter for stability and transient settling. The transient simulation incorporates two adjacent channels of the multiplexer (TMUX1109). To simulate worst case transient settling during the multiplexer scanning sequence, the two adjacent channels are set to a voltage close to positive full-scale and negative full-scale respectively. The multiplexer drain capacitance and series resistance are modeled in the multiplexer simulation circuit. The sample and hold capacitor of the SAR ADC must settle within the 16-bit resolution of the SAR ADC during the acquisition period. A simplified schematic of the simulation circuit follows:



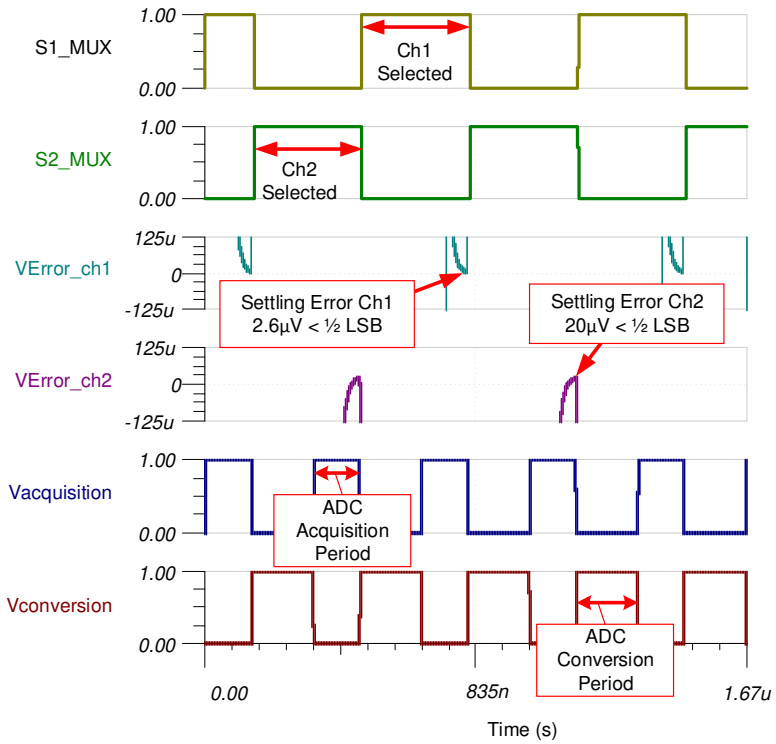
Multiplexer and ADC Control Timing

The following plot shows the ADC conversion control (CONVST) and multiplexer channel control timing. The ADS9224R supports a maximum sampling rate of 3Msps or a minimum cycle time of 333ns. To avoid switching channels prior to the rising edge of the CONVST signal, a small delay is implemented in the MUX channel control timing after the CONVST rising edge. Refer to TI design *16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design* for detailed theory in the subject.



Transient Settling Results

The following TINA transient simulation shows settling of the FDA, multiplexer, and SAR ADC sample and hold after a full-scale step change between adjacent MUX channels. This type of simulation shows that the sample and hold kickback circuit, and AFE amplifier circuit is properly selected. See *Introduction to SAR ADC Front-end Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

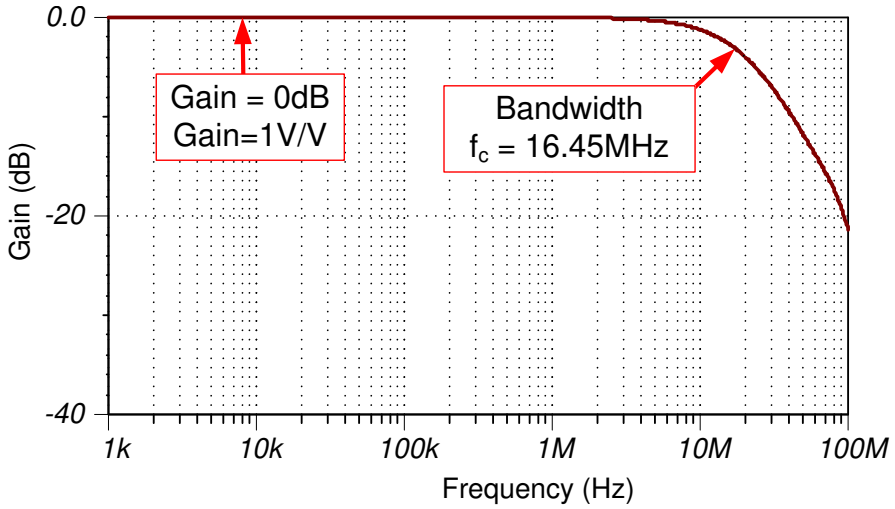


AC Transfer Characteristics

The circuit has a gain of 0-dB (1-V/V) and a simulated frequency bandwidth of 16.45-MHz. Notice that the calculated and simulated bandwidth compare well (calculated = 17.62MHz, simulated = 16.45MHz). See *Op Amp Bandwidth* for a general overview of bandwidth calculations and simulations.

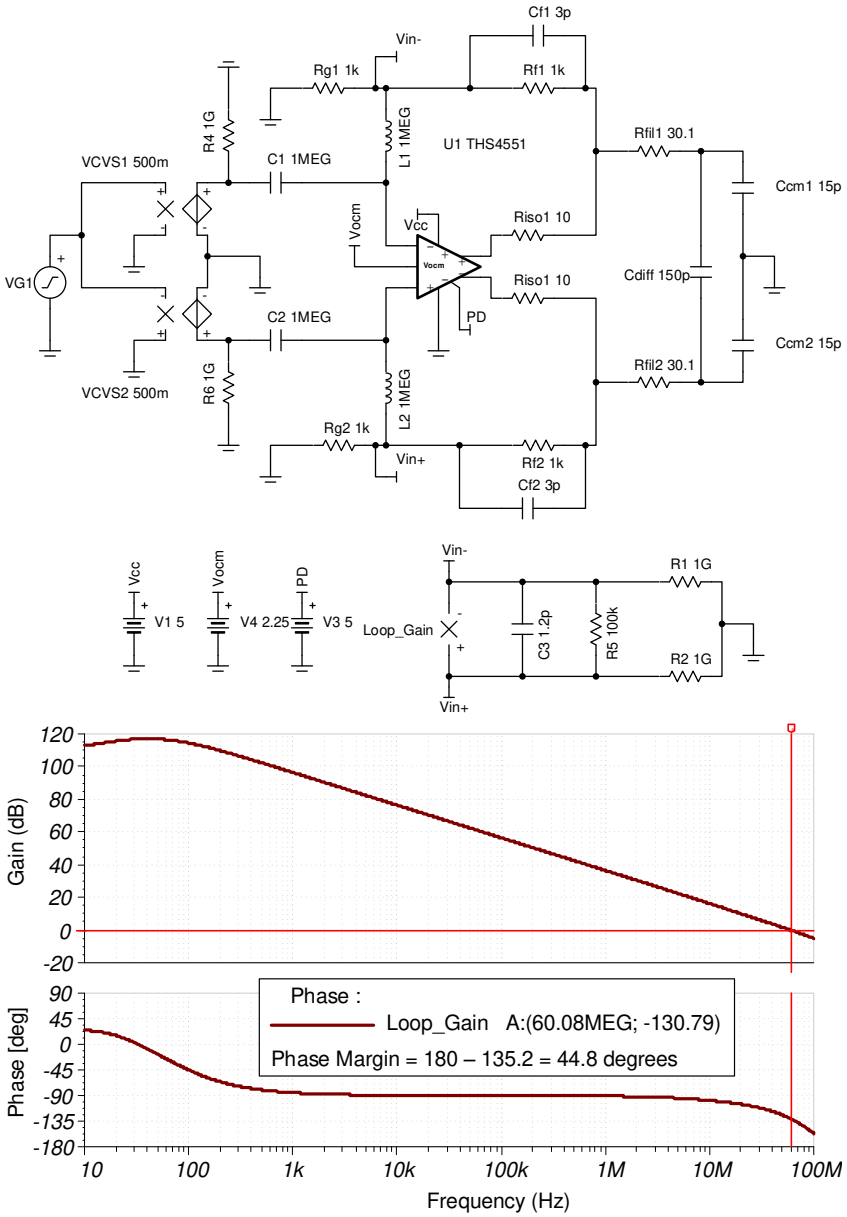
The system bandwidth is set by the output filter:

$$f_c = \frac{1}{2\pi (R_{fil1} + R_{fil2}) C_{diff}} = \frac{1}{2\pi \left(30.1\Omega + 30.1\Omega\right)\left(150pF\right)} = 17.62MHz$$



Stability Simulation Graph

The following circuit is used in TINA to measure loop gain and verify phase margin using AC analysis in TINA. Resistors RISO = 10Ω are used inside the feedback loop to increase phase margin. The circuit has good stability (approximately 45 degrees of phase margin). See *Op Amp Stability* for detailed theory on this subject.



Noise Simulation

Simplified noise calculation estimate:

The dominant pole in this data acquisition circuit is in the RC kickback filter:

$$f_c = \frac{1}{2\pi (R_{fil1} + R_{fil2}) C_{diff}} = \frac{1}{2\pi \left(30.1\Omega + 30.1\Omega\right)\left(150pF\right)} = 17.62MHz$$

Noise of THS4551 FDA referred to ADC input

Noise Gain: $NG = 1 + R_f / R_g = 1 + \frac{1k\Omega}{1k\Omega} = 2V/V$

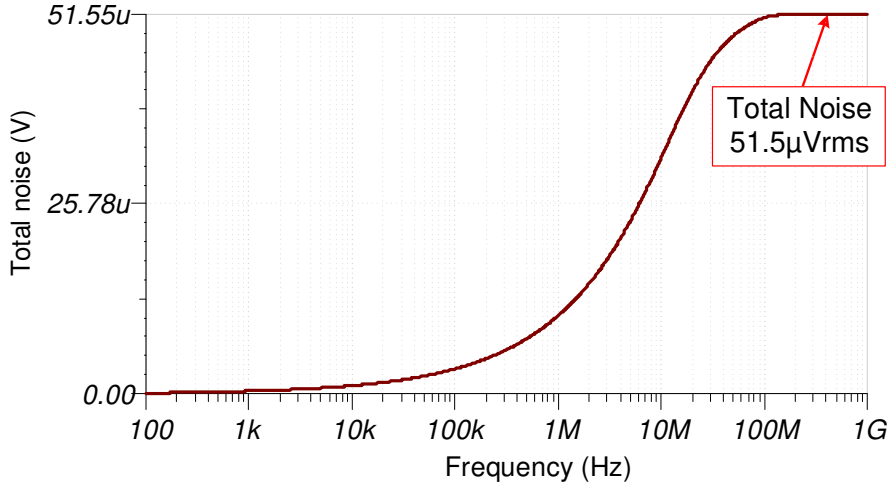
$$e_{noFDA} = \sqrt{\left(e_{nFDA} \cdot NG\right)^2 + 2\left(i_{nFDA} \cdot R_f\right)^2 + 2\left(4kTR_f \cdot NG\right)}$$

$$e_{noFDA} = \sqrt{\left(3.4nV/\sqrt{Hz} \cdot 2.00V/V\right)^2 + 2\left(0.5pA/\sqrt{Hz} \cdot 1k\Omega\right)^2 + 2\left(16.56 \cdot 10^{-18} \cdot 2.00V/V\right)}$$

$$e_{noFDA} = 10.629nV/\sqrt{Hz}$$

$$E_{nFDA} = e_{noFDA} \cdot \sqrt{K_n \cdot f_c} = \left(10.629nV/\sqrt{Hz}\right)\sqrt{1.57 \cdot 17.62MHz} = 55.90\mu Vrms$$

The following figure shows the TINA simulated total noise for the FDA circuit. See *Calculating the Total Noise for ADC systems* for detailed theory on this subject. Note that the calculated and simulated noise compare well (calculated = 55.9µV$_{rms}$, simulated = 51.5µV$_{rms}$).



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS9224R	16-bit resolution, SPI, 3-MSPS sample rate, fully-differential input, integrated 2.5-V reference, dual, simultaneous sampling, low-latency	16-bit, 3MSPS, dual-channel, simultaneous-sampling SAR ADC with internal reference and enhanced SPI	Analog-to-digital converters (ADCs)
THS4551	150MHz, 3.3nV ÷ √ Hz input voltage noise, fully-differential amplifier	Low Noise, Precision, 150MHz, Fully Differential Amplifier	Fully differential amplifiers

Link to Key Files

Texas Instruments, SBAC219 TINA files, software support

Trademarks

All trademarks are the property of their respective owners.

Revision History

Changes from Revision A (November 2018) to Revision B (August 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (October 2019) to Revision A (November 2019)	Page
• Downscale title. Updated the schematic in the *Transient Settling Optimization* section	1

Analog Engineer's Circuit

Circuit for Driving a Switched-Capacitor SAR ADC With a Buffered Instrumentation Amplifier

Art Kay

Input	ADC Input	Digital Output ADS8860
–10mV	Out = 0.2V	$0A3D_H$ or 2621_{10}
5mV	Out = 4.8V	$F5C3_H$ or 62915_{10}

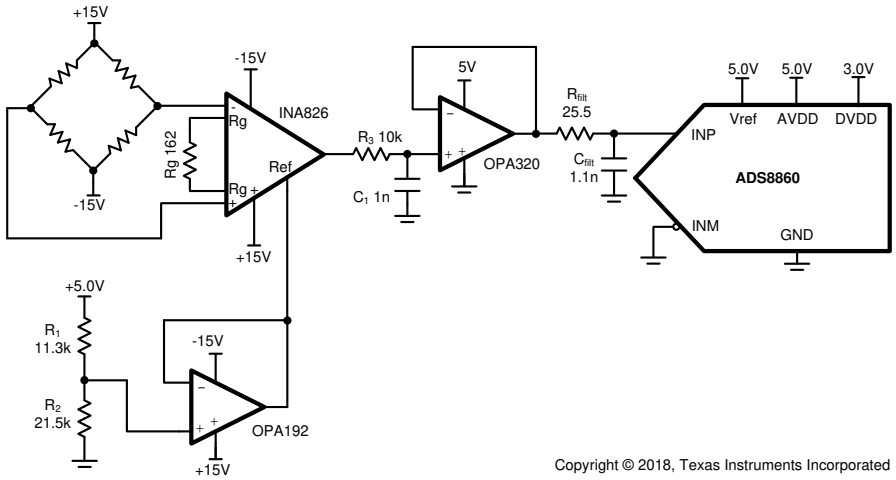
Power Supplies

AVDD	DVDD	V_{ref_INA}	V_{ref}	V_{cc}	V_{ee}
5.0V	3V	3.277V	5.0V	15V	–15V

Design Description

Instrumentation amplifiers are a common way of translating low-level sensor outputs to high-level signals to drive an ADC. Typically, instrumentation amplifiers are optimized for low noise, low offset, and low drift. Unfortunately, the bandwidth of many instrumentation amplifiers may not be sufficient to achieve good settling to ADC charge kickback at maximum sampling rates. This document shows how a wide-bandwidth buffer can be used with an instrumentation amplifier to achieve good settling at high sampling rates. Furthermore, many instrumentation amplifiers are optimized for high voltage supplies and it can be required to interface the high voltage output (that is, ±15V) to a lower voltage amplifier (for example, 5V). This design shows how a current-limiting resistor can protect the amplifier from electrical overstress in cases where the instrumentation amplifier is outside the input range of the op amp. A related cookbook circuit shows a simplified approach that does not include the wide-bandwidth buffer (*Driving a Switched-Capacitor SAR With an Instrumentation Amplifier* circuit design). The simplified approach has limited sampling rate as compared to the buffered design. Note that the following circuit shows a bridge sensor, but this method could be used for a wide range of different sensors.

This circuit implementation is applicable in applications such as *analog input modules*, *electrocardiograms (ECGs)*, *pulse oximeters*, *lab instrumentation*, and *control units for rail transport*.



Specifications

Specification	Calculated	Simulated
Sampling rate	1Msps	1Msps, settling to –44µV
Offset (ADC Input)	40µV × 306.7 = 12.27mV	16mV
Offset Drift	(0.4µV/°C) × 306.7 = 123µV/°C	N/A
Noise	978µV	586µV_{RMS}

Design Notes

1. The bandwidth of instrumentation amplifiers is typically too low to drive SAR data converters at high data rates (the INA826 bandwidth is 10.4kHz for a gain of 305V/V in this example). Wide bandwidth is needed because the SAR has a switched capacitor input that needs to be charged during each conversion cycle. The OPA320 buffer was added to allow the ADC to run at full data rate (ADS8860 1Msps).
2. Select the gain to achieve an input swing that matches the input range of the ADC. Use the instrumentation amplifier reference pin to shift the signal offset to match the input range. This is covered in the *component selection* section.
3. The INA826 gain is scaled so that the op amp input voltage levels are inside the normal operating range of the amplifier. However, during power up or when a sensor is disconnected the output can drive to either power supply rail (±15V). The resistor R_3 is used to limit the current . This is covered in the *Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp* section of this document.
4. The buffer amplifier following the voltage divider is required for driving the reference input of most instrumentation amplifiers. Choose precision resistors and a precision low offset amplifier as the buffer. Refer to *Selecting the right op amp* for more details on this subject.
5. Check the common mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
6. Select COG capacitors for C_1, and C_{filt} to minimize distortion.
7. Use 0.1% 20ppm/°C film resistors or better for the gain set resistor R_g. The error and drift of this resistor directly translates into gain error and gain drift.
8. The *Precision labs series: Analog-to-digital converters (ADCs)* training video series methods for selecting the charge bucket circuit R_{filt} and C_{filt}. Refer to the *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

1. Find the gain set resistor for the instrumentation amplifier to set the output swing to 0.2V to 4.8V.

$$Gain = \frac{V_{out\_max} - V_{out\_min}}{V_{in\_max} - V_{in\_min}} = \frac{4.9V - 0.2V}{5mV - (-10mV)} = 306.7$$

$$Gain = 1 + \frac{49.4k\Omega}{R_g}$$

$$R_g = \frac{49.4k\Omega}{Gain - 1.0} = \frac{49.4k\Omega}{(306.7) - 1.0} = 151.6\Omega \text{ or } 162\Omega \text{ for standard } 0.1\% \text{ resistor}$$

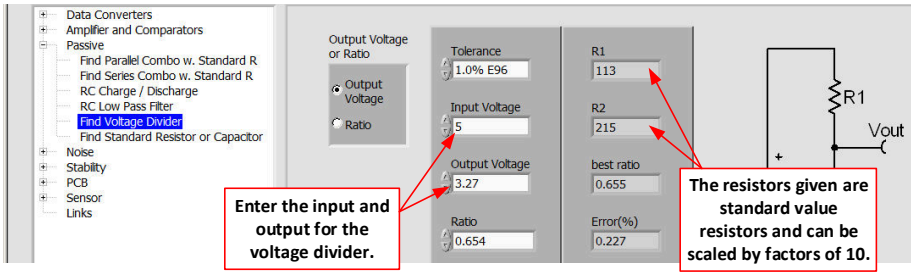
2. Find the INA826 reference voltage (Vref) to shift the output swing to the proper voltage level.

$$V_{out} = Gain \cdot V_{in} + V_{ref\_INA}$$

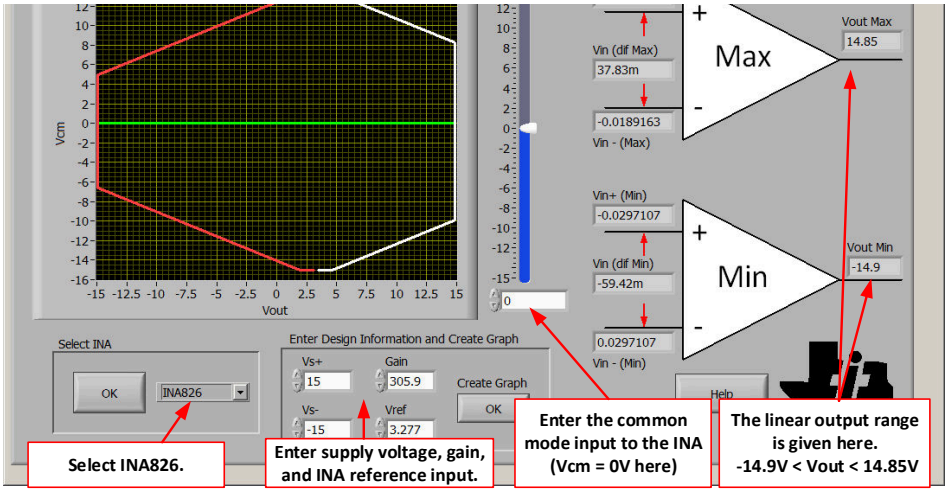
$$V_{ref\_INA} = V_{out} - Gain \cdot V_{in} = 4.8V - \left(1 + \frac{49.4k\Omega}{162\Omega}\right) \cdot (5mV) = 3.27V$$

3. Select standard value resistors to set the INA826 reference voltage (V_{ref_INA} = 3.27V). Use the *Analog Engineer's Calculator* ("Passive\Find Voltage Divider" section) to find standard values for the voltage divider.

$$V_{ref\_INA} = \frac{R_2}{R_1 + R_2} \cdot V_{in\_div} = \frac{21.5k\Omega}{11.3k\Omega + 21.5k\Omega} \cdot (5V) = 3.277V$$

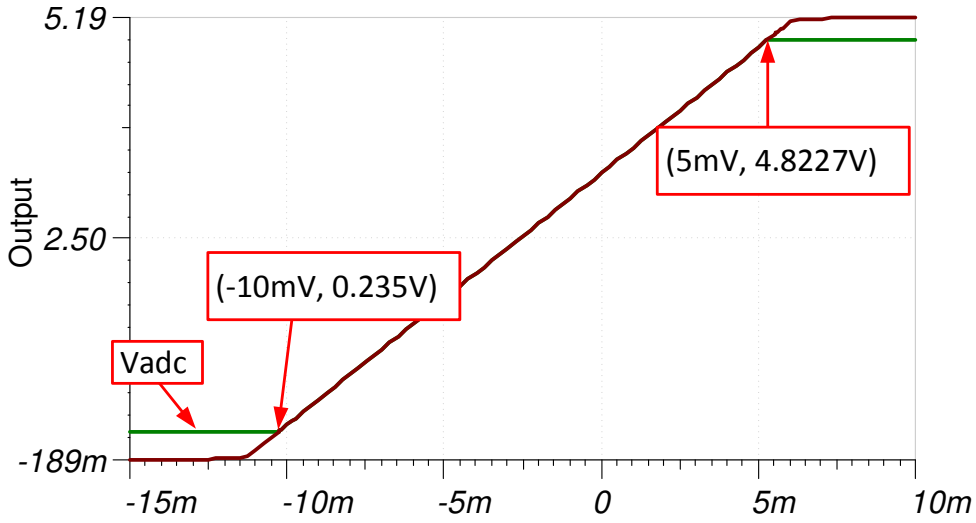


4. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common mode range.



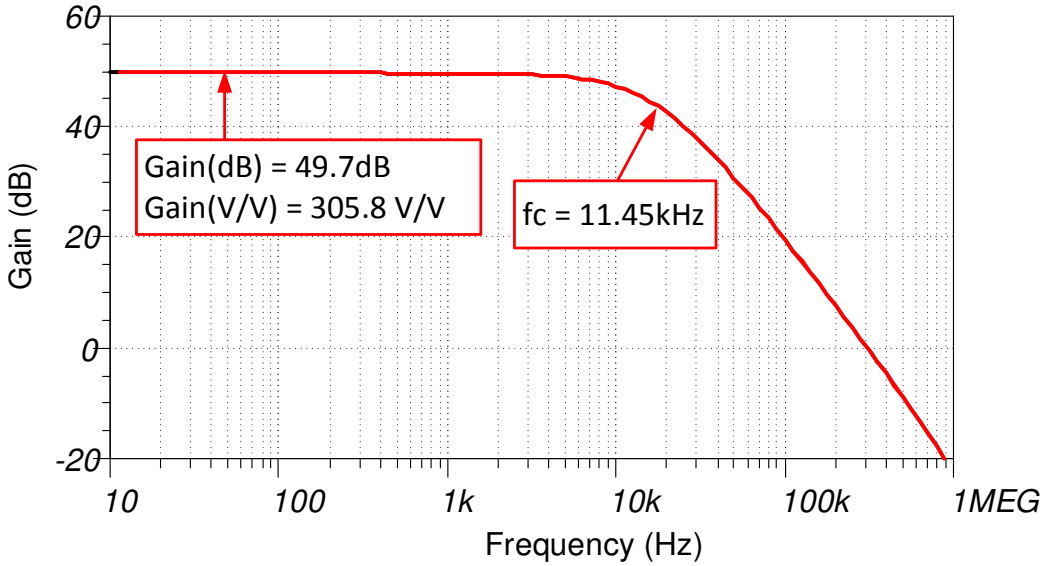
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –5mV to +15mV. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. In cases where the INA826 output exceeds the op amp input range, the ESD diodes turn on and limit the input. The resistor R3 protects the amplifier from damage by limiting the input current (see the *Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp* section). The op amp output is inside the absolute maximum rating of the ADS8860 (–0.3V < V_{IN} < REF +0.3V).



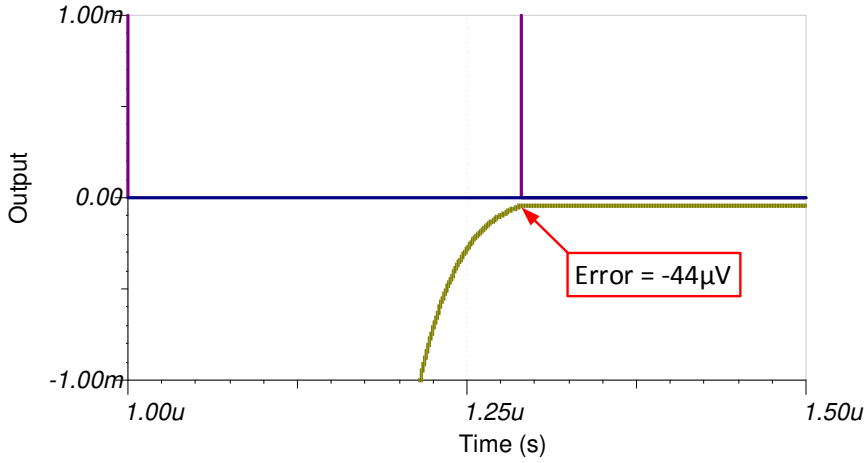
AC Transfer Characteristics

The bandwidth is simulated to be 11.45 kHz in this configuration. In this bandwidth it is not possible to drive the SAR converter at full speed. See the *TI Precision Labs* video series *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The OPA320 buffer (20MHz) is used because it is capable of responding to the rapid transients from the ADC8860 charge kickback. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



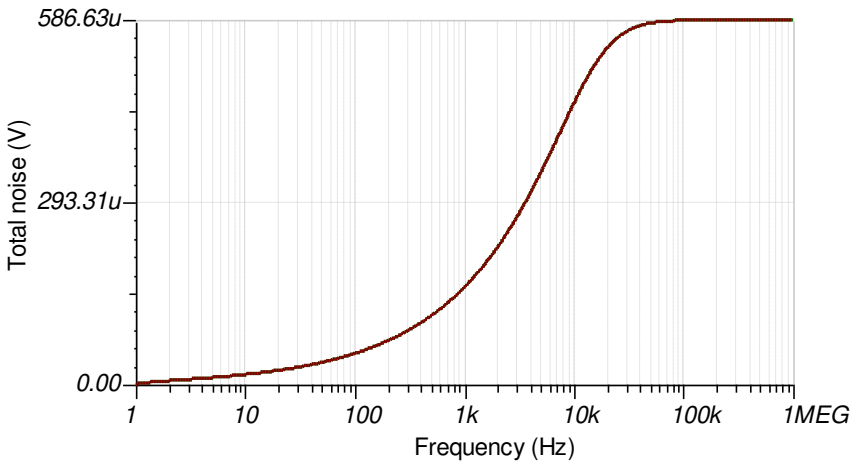
Noise Simulation

Use a simplified noise calculation for a rough estimate. We neglect the noise from the OPA192 as the instrumentation amplifier is in high gain so its noise is dominant.

$$E_n = Gain \cdot \sqrt{e_{NI}{}^2 + \left(\frac{e_{NO}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = (305.8) \cdot \sqrt{\left(18nV/\sqrt{Hz}\right)^2 + \left(\frac{110nV/\sqrt{Hz}}{305.8}\right)^2} \cdot \sqrt{1.57 \cdot (11.45kHz)} = 738\mu V/\sqrt{Hz}$$

Note that the calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating the Total Noise for ADC Systems* for data converter noise.

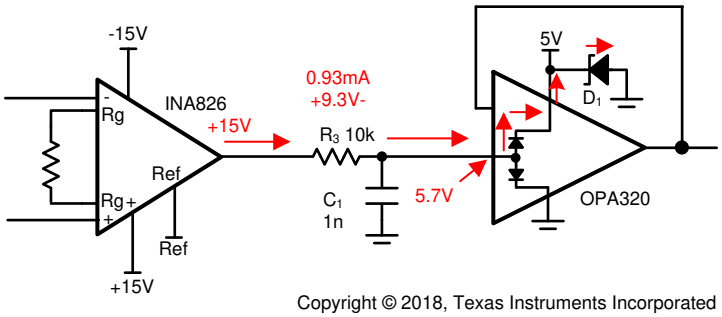


Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp

The filter between the INA826 and OPA320 serves two purposes. It protects the OPA320 from overvoltage, and acts as a noise or anti-aliasing filter. Scale the INA826 gain so that under normal circumstances, the output is inside the range of the OPA320 (that is, 0V to 5V). Thus, normally the overvoltage signals applied to the input of the OPA320 is not seen. However, during power up or in cases where the sensor is disconnected, the INA826 output can be at either power supply rail (that is, ±15V). In overvoltage cases, the resistor (R3) limits current into the OPA320 for protection. The internal ESD diodes on the OPA320 turns on during overvoltage events and direct the overvoltage signal to the positive or negative supply. In the following example, the overvoltage signal is directed to the positive supply and the transient voltage suppressor (D_1, SMAJ5.0A) turns on to sink the current. Note that the resistor is scaled to limit the current to the OPA320 absolute maximum input current (10mA). See *TI Precision Labs - Op Amps: Electrical Overstress (EOS)* for detailed theory on this subject.

$$R_3 > \frac{V_{INA} - V_{OpaSupply} - 0.7V}{I_{ABS\_MAX\_OPA}} = \frac{15V - 5.0V - 0.7V}{10mA} = 9.3k\Omega \text{ choose } 10\text{k}\Omega \text{ for margin.}$$

$$C_1 = \frac{1}{2 \cdot \pi \cdot R_3 \cdot f_c} = \frac{1}{2 \cdot \pi \cdot (10k\Omega) \cdot (15kHz)} = 1.06nF \text{ or } 1\text{nF standard value}$$



Optional Input Filter

The following figure shows a commonly used instrumentation amplifier input filter. The differential noise is filtered with C_{dif}, and the common mode noise is filtered with C_{cm1} and C_{cm2}. Note that it is recommended that $C_{dif} \geq 10C_{cm}$. This prevents conversion of common mode noise to differential noise due to component tolerances. The following filter was designed for a differential cutoff frequency of 15kHz.

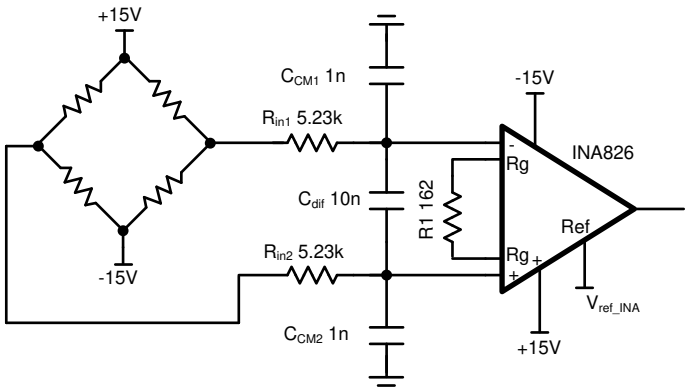
Let $C_{dif} = 1nF$ and $f_{dif} = 15kHz$

$$R_{in} < \frac{1}{4 \cdot \pi \cdot f_{dif} \cdot C_{dif}} = \frac{1}{4 \cdot \pi \cdot (15kHz) \cdot (1nF)} = 5.305k\Omega \text{ or } 5.23k\Omega \text{ for 1\% standard value}$$

$$C_{cm} = \frac{1}{10} \cdot C_{dif} = 100pF$$

$$f_{cm} = \frac{1}{2 \cdot \pi \cdot R_{in} \cdot C_{cm}} = \frac{1}{2 \cdot \pi \cdot (5.23k\Omega) \cdot (100pF)} = 304kHz$$

$$f_{dif} = \frac{1}{4 \cdot \pi \cdot R_{in} \cdot \left(C_{dif} + \frac{1}{2} C_{cm} \right)} = \frac{1}{4 \cdot \pi \cdot (5.23k\Omega) \cdot \left(1nF + \frac{1}{2} \cdot 100pF \right)} = 14.5kHz$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8860	16-bit resolution, SPI, 1-Msps sample rate, single-ended input, Vref input range 2.5V to 5.0V.	16-bit, 1MSPS, 1-channel SAR ADC with single-ended input, SPI and daisy chain	Precision ADCs
OPA192	8-kHz bandwidth, Rail-to-Rail output, 450-nA supply current, unity gain stable	High-Voltage, Rail-to-Rail Input/ Output, 5μV, 0.2μV/˚C, Precision Operational Amplifier	Precision op amps (Vos<1mV)
INA826	Bandwidth 1MHz (G=1), low noise 18nV/rtHz, low offset ±40μV, low offset drift ±0.4μV/°C, low gain drift 0.1ppm/°C. (typical values)	Precision, 200-μA Supply Current, 36-V Supply Instrumentation Amplifier	Instrumentation amplifiers

Link to Key Files

Texas Instruments, source files for SBAC184, software support

Trademarks

All trademarks are the property of their respective owners.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (February 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to Data Converters. Added link to circuit cookbook landing page	1

Analog Engineer's Circuit

Circuit for Driving a Switched-Capacitor SAR ADC With an Instrumentation Amplifier

Art Kay and Bryan McKay

Input	ADC Input	Digital Output ADS8860
–5mV	Out = 0.2V	$0A3D_H$ or 2621_{10}
15mV	Out = 4.8V	$F5C3_H$ or 62915_{10}

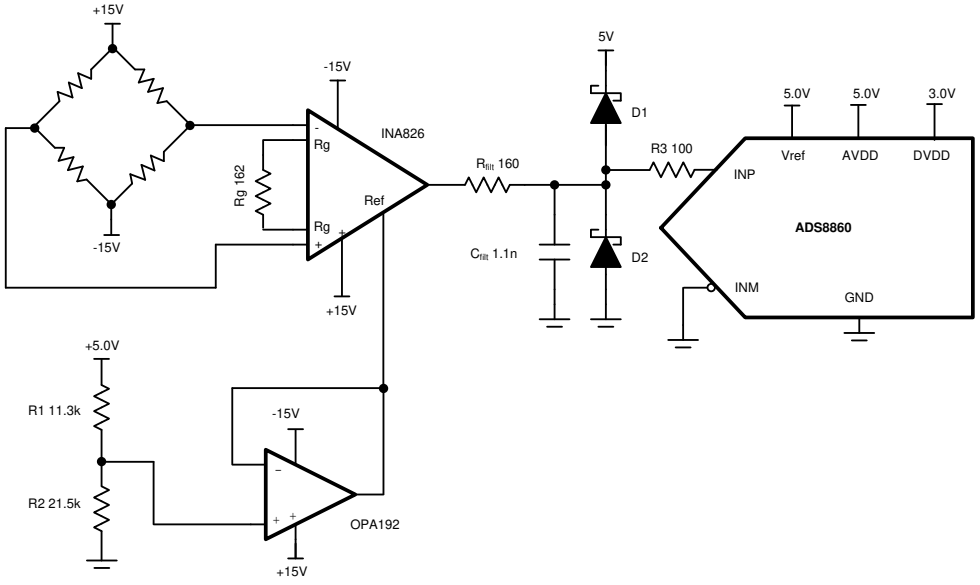
Table 1-1. Power Supplies

AVDD	DVDD	V_{ref_INA}	V_{ref}	V_{cc}	V_{ee}
5.0V	3.0V	3.277V	5.0V	+15V	–15V

Design Description

Instrumentation amplifiers are a common way of translating low level sensor outputs to high level signals to drive an ADC. Typically, instrumentation amplifiers are optimized for low noise, low offset, and low drift. Unfortunately, the bandwidth of many instrumentation amplifiers may not be sufficient to achieve good settling to ADC charge kickback at maximum sampling rates. This document shows how sampling rate can be adjusted to achieve good settling. Furthermore, many instrumentation amplifiers are optimized for high-voltage supplies and it may be required to interface the high-voltage output (that is, ±15V) to a lower voltage ADC (for example, 5V). This design shows how to use Schottky diodes and a series resistor to protect the ADC input from an overvoltage condition. Note that the following circuit shows a bridge sensor, but this method could be used for a wide range of different sensors. A modified version of this circuit, *Driving a Switched-Capacitor SAR With a Buffered Instrumentation Amplifier* shows how a wide bandwidth buffer can be used to achieve higher sampling rate.

This circuit implementation is applicable to all *Bridge Transducers in PLC's* and *Analog Input Modules* that require precision signal-processing and data-conversion.



Specifications

Specification	Calculated	Simulated
Sampling rate	200ksps	200ksps, settling to –6µV
Offset (ADC Input)	40µV × 306.7 = 12.27mV	16mV
Offset Drift	(0.4µV/°C) × 306.7 = 123µV/°C	NA
Noise	978µV	874µV

Design Notes

1. Select the gain to achieve an input swing that matches the input range of the ADC. Use the instrumentation amplifier reference pin to shift the signal offset to match the input range. This is covered in the component selection section.
2. The input Schottky diode configuration is used to prevent driving the input voltage outside of the absolute maximum specifications. The BAT54S Schottky is a good option for design as this device integrates both diodes into one package and the diodes are low leakage and have a low forward voltage. This is covered in the *component selection* section.
3. The buffer amplifier following the voltage divider is required for driving the reference input of most instrumentation amplifiers. Choose precision resistors and a precision low-offset amplifier as the buffer. Refer to *Selecting the right op amp* for more details on this subject.
4. Check the common-mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
5. Select C0G capacitors for C_{CM1}, C_{CM2}, C_{DIF}, and C_{filt} to minimize distortion.
6. Use 0.1% 20ppm/°C film resistors or better for the gain set resistor R_g. The error and drift of this resistor directly translates into gain error and gain drift.
7. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. Although this method was designed for op amps, it can be modified for instrumentation amplifiers. Refer to *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

1. Find the gain set resistor for the instrumentation amplifier to set the output swing to 0.2V to 4.8V.

$$\text{Gain} = \frac{V_{out\_max} - V_{out\_min}}{V_{in\_max} - V_{in\_min}} = \frac{4.9\text{V} - 0.2\text{V}}{5\text{mV} - (-10\text{mV})} = 306.7$$

$$\text{Gain} = 1 + \frac{49.4\text{k}\Omega}{R_g}$$

$$R_g = \frac{49.4\text{k}\Omega}{\text{Gain} - 1.0} = \frac{49.4\text{k}\Omega}{(306.7) - 1.0} = 151.6\Omega \text{ or } 162\Omega \text{ for standard 0.1\% resistor}$$

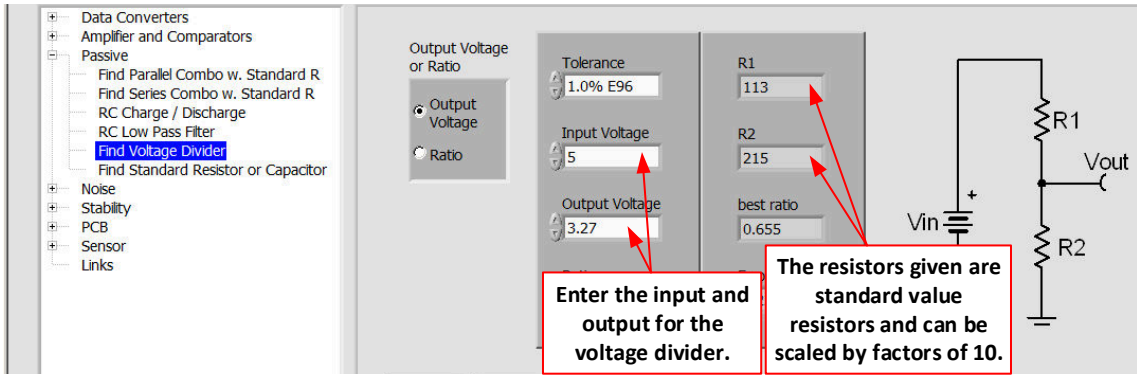
2. Find the INA826 reference voltage (V_{ref}) to shift the output swing to the proper voltage level.

$$V_{out} = \text{Gain} \cdot V_{in} + V_{ref\_INA}$$

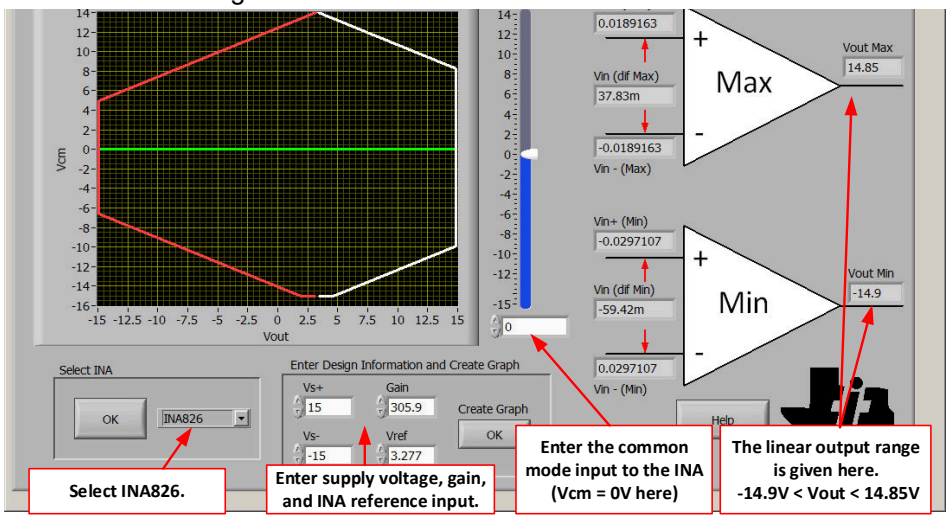
$$V_{ref\_INA} = V_{out} - \text{Gain} \cdot V_{in} = 4.8\text{V} - \left(1 + \frac{49.4\text{k}\Omega}{162\Omega}\right) \cdot (5\text{mV}) = 3.27\text{V}$$

3. Select standard value resistors to set the INA826 reference voltage (V_{ref} = 3.27V). *Use Analog Engineer's Calculator* ("Passive\Find Voltage Divider" section) to find standard values for the voltage divider.

$$V_{ref\_INA} = \frac{R_2}{R_1 + R_2} \cdot V_{in\_div} = \frac{21.5\text{k}\Omega}{11.3\text{k}\Omega + 21.5\text{k}\Omega} \cdot (5\text{V}) = 3.277\text{V}$$

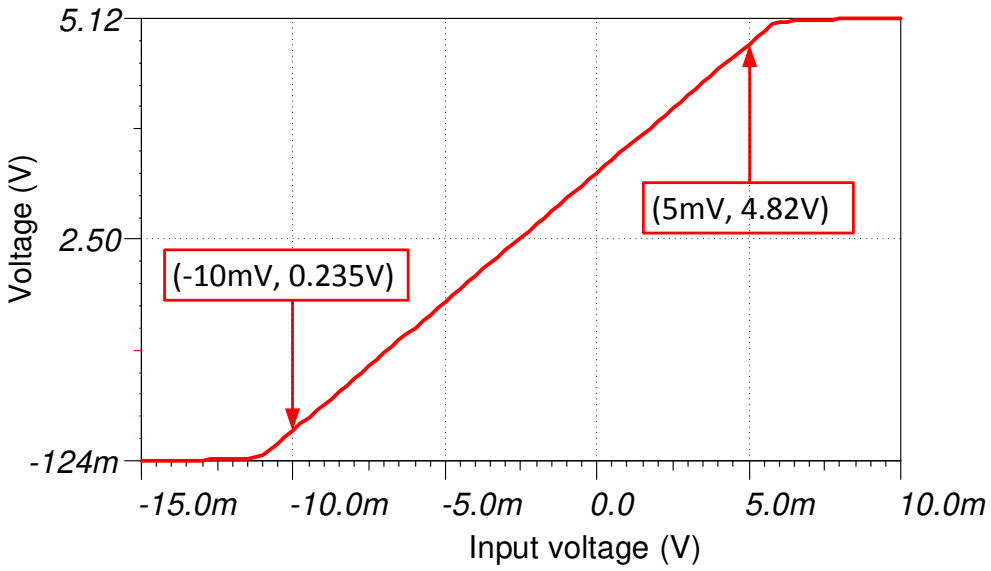


4. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common-mode range.



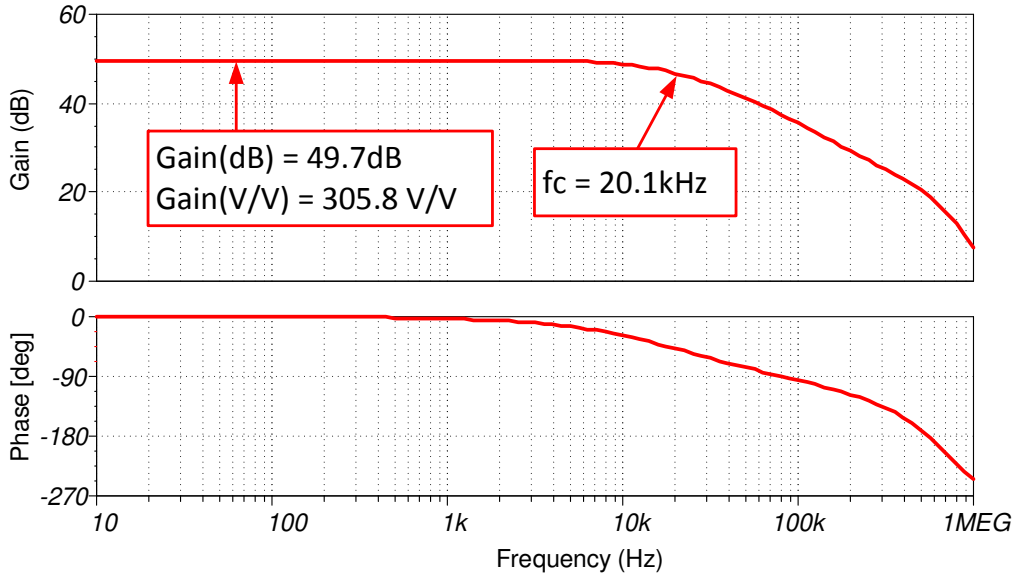
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –5mV to +15mV. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. Note that the output range is intentionally limited to –0.12V to 5.12V using Schottky diodes to protect the ADS8860. Note that Schottky diodes are used because the low forward voltage drop (typically less than 0.3V) keeps the output limit very near the ADC supply voltages. The absolute maximum rating for the ADS8860 is –0.3V < Vin < REF +0.3V.



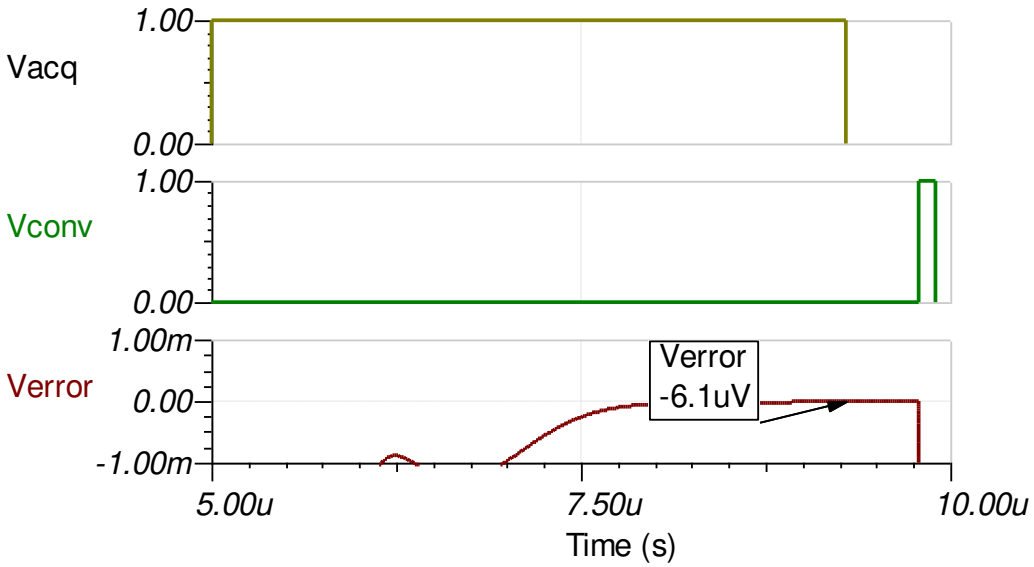
AC Transfer Characteristics

The bandwidth is simulated to be 20.1kHz, and the gain is 49.7dB which is a linear gain of 305.8. See the video series on *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a +15mV dc input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject



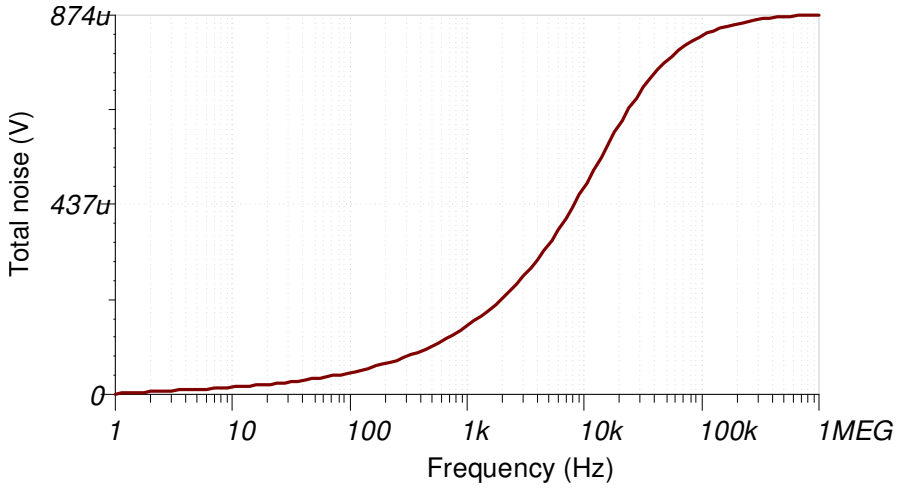
Noise Simulation

The following simplified noise calculation is provided for a rough estimate. We neglect noise from the OPA192 as the instrumentation amplifier is in high gain, so its noise is dominant.

$$E_n = Gain \cdot \sqrt{e_{NI}^2 + \left(\frac{e_{NO}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = (305.8) \cdot \sqrt{(18nV/\sqrt{Hz})^2 + \left(\frac{110nV/\sqrt{Hz}}{305.8}\right)^2} \cdot \sqrt{1.57 \cdot (20.1kHz)} = 978\mu V/\sqrt{Hz}$$

Note that calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating the Total Noise for ADC Systems* for data converter noise.



Optional Input Filter

The following figure shows a commonly used instrumentation amplifier input filter. The differential noise is filtered with C_{dif}, and the common-mode noise is filtered with C_{cm1} and C_{cm2}. Note that it is recommended that $C_{dif} \geq 10C_{cm}$. This prevents conversion of common-mode noise to differential noise due to component tolerances. The following filter was designed for a differential cutoff frequency of 15kHz.

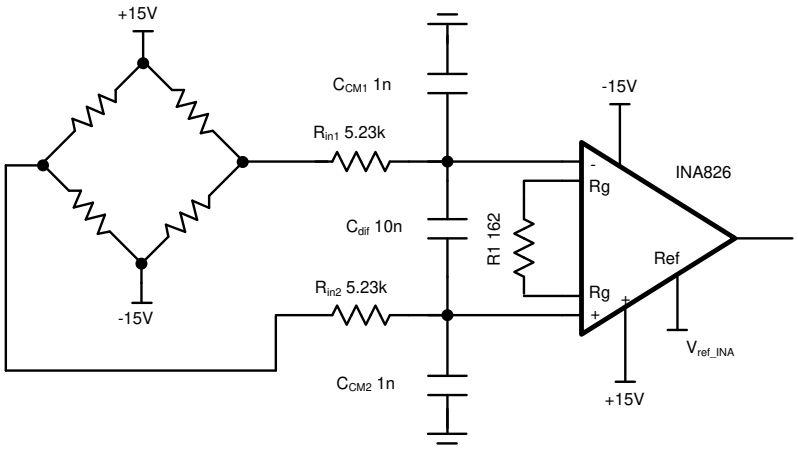
Let $C_{dif} = 1nF$ and $f_{dif} = 15kHz$

$$R_{in} < \frac{1}{4 \cdot \pi \cdot f_{dif} \cdot C_{dif}} = \frac{1}{4 \cdot \pi \cdot (15kHz) \cdot (1nF)} = 5.305k\Omega \text{ or } 5.23k\Omega \text{ for 1\% standard value}$$

$$C_{cm} = \frac{1}{10} \cdot C_{dif} = 100pF$$

$$f_{cm} = \frac{1}{2 \cdot \pi \cdot R_{in} \cdot C_{cm}} = \frac{1}{2 \cdot \pi \cdot (5.23k\Omega) \cdot (100pF)} = 304kHz$$

$$f_{dif} = \frac{1}{4 \cdot \pi \cdot R_{in} \cdot \left(C_{dif} + \frac{1}{2}C_{cm}\right)} = \frac{1}{4 \cdot \pi \cdot (5.23k\Omega) \cdot \left(1nF + \frac{1}{2} \cdot 100pF\right)} = 14.5kHz$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8860	16-bit resolution, SPI, 1Msps sample rate, single-ended input, Vref input range 2.5V to 5.0V.	16-bit, 1MSPS, 1-channel SAR ADC with single-ended input, SPI and daisy chain	Precision ADCs
OPA192	Bandwidth 10MHz, Rail-to-Rail input and output, low noise 5.5nV/rtHz, low offset ±5µV, low offset drift ±0.2µV/°C. (Typical values)	High-Voltage, Rail-to-Rail Input/ Output, 5µV, 0.2µV/˚C, Precision Operational Amplifier	Precision op amps (Vos<1mV)
INA826	Bandwidth 1MHz (G = 1), low noise 18nV/rtHz, low offset ±40µV, low offset drift ±0.4µV/°C, low gain drift 0.1ppm/°C. (Typical values)	Precision, 200-µA Supply Current, 36-V Supply Instrumentation Amplifier	Instrumentation amplifiers

Link to Key Files

Texas Instruments, Source Files for SBAA277, support software

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024) **Page**

- Updated the format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision * (December 2017) to Revision A (March 2019) **Page**

- Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page... 1

Trademarks

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Analog Engineer's Circuit

Circuit for driving an ADC with an instrumentation amplifier in high gain

Dale Li, Art Kay

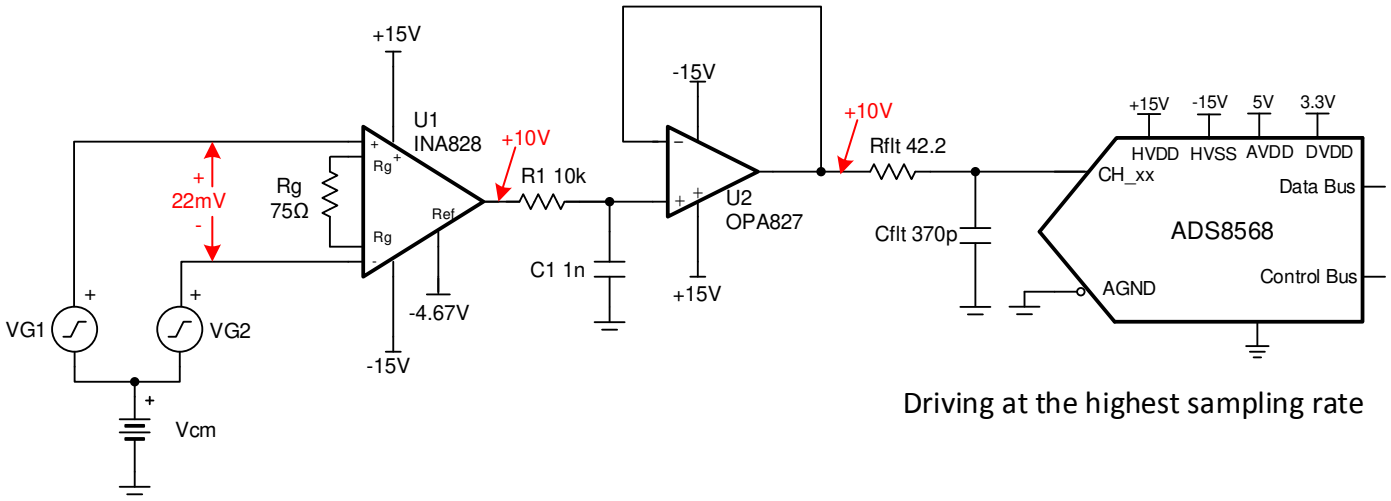
Input	ADC Input	Digital Output ADS8568
VinDiffMin = –8mV	CH_x = –10V	8000H
VinDiffMax = +22mV	CH_x = +10V	7FFFH

Power Supplies

AVDD		Vee	Vdd
5.0V	3.3V	+15V	–15V

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy but these instrument amplifiers are not able to drive a precision ADC to settle the signal properly during the acquisition time of ADC. This design shows an example of how to set the gain and offset shift to amplify a low level asymmetric input signal. Also, the high gain limits the INA828 instrumentation amplifier bandwidth, so an OPA827 op amp is used as a buffer so that the ADS8568 full sampling rate can be achieved. A related cookbook circuit shows a simplified approach that does not include the wide bandwidth buffer (*Driving High Voltage SAR ADC with an Instrumentation Amplifier*), this simplified approach has limited sampling rate as compared to the buffered design in this document. Also *Driving High Voltage SAR ADC with a Buffered Instrumentation Amplifier*, analyzes this design in unity gain. This circuit implementation is applicable to all *Bridge Transducers in PLC's* and *Analog Input Modules* that require precision signal-processing and data-conversion.



Driving at the highest sampling rate

Specifications

Specification	Goal	Calculated	Simulated
Transient Settling Error	>0.5 LSB (152µV)	NA	0.36µV
Noise		1.1mV	1.14mV
System Offset Error		33.6mV	NA
System Offset Drift		334µV/°C	NA
System Gain Error		0.53%	NA
System Gain Drift		54.2ppm/°C	NA

Design Notes

1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at a higher data rate. This is especially true when the instrumentation amplifier is in high gain. so a wide bandwidth driver is needed because the SAR ADC with switched-capacitor input structure has an input capacitor that needs to be fully charged during each acquisition time. The OPA827 buffer is added to allow the ADC to run at full sampling rate (ADS8568 510kSPS for parallel interface).
2. Check the common-mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
3. Select COG capacitors for C_1 and C_{filt} to minimize distortion.
4. The gain set resistor, R_g, are 0.1% 20ppm/°C film resistors or better for low gain error and low gain drift.
5. The *TI Precision Labs* video series covers the method for selecting the driver amplifier and the charge bucket circuit R_{filt} and C_{filt}. See *Introduction of SAR ADC Front-End Component Selection* for details.
6. Set the cutoff of the filter between the op amp and instrumentation amplifier for anti aliasing and to minimize noise. See *Aliasing and Anti-aliasing Filters* for more details on aliasing and anti-aliasing filters.
7. Because of the high instrumentation amplifier gain, the DC errors (offset, gain, and drift) are significant. Calibration is a good approach to minimizing these errors. See *Understanding and Calibrating the Offset and Gain for ADC Systems* for more details on calibration.

Component Selection

1. Find the gain based on differential input signal and the ADS8568 full-scale input range.

$$G = \frac{V_{out} - V_{out}}{V_{in} - V_{in}} = \frac{10V - (-10V)}{22mV - (-8mV)} = 666.7$$

$$R_g = \frac{50k\Omega}{G - 1} = \frac{50k\Omega}{666.7} = 75.1\Omega$$

$$R_g = 75.1\Omega \text{ standard value}$$

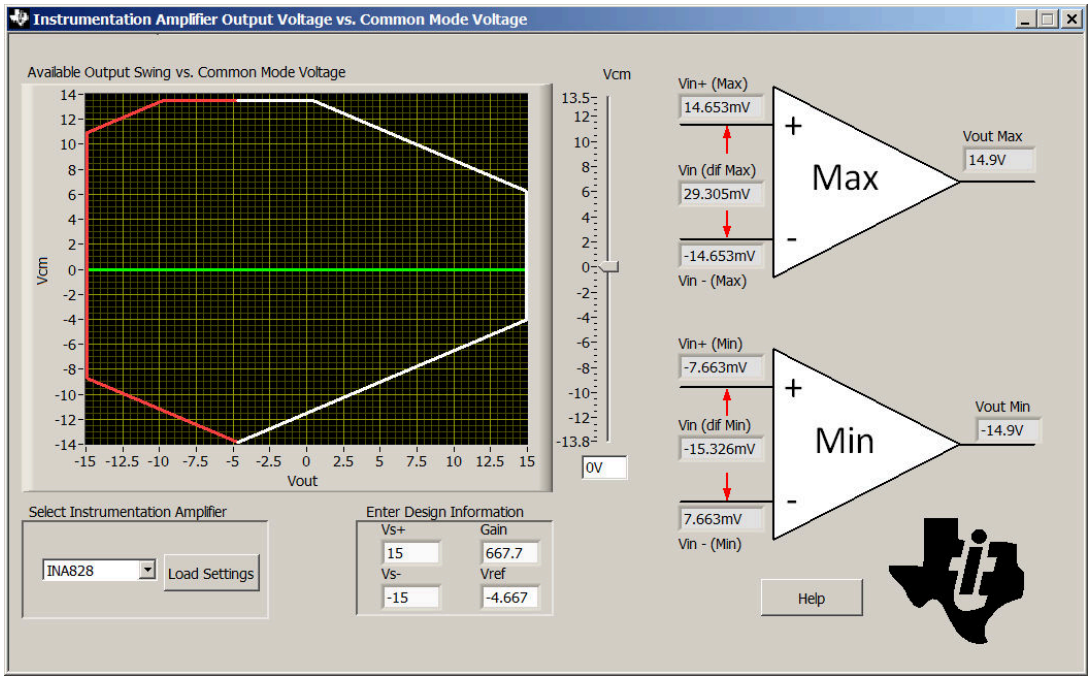
$$G = 1 + \frac{50k\Omega}{R_g} = 667.7$$

2. The input signal in this design is ±10-V high voltage signal, so the gain of INA828 are set to 1 and no gain resistor (R_g) is needed.

$$V_{out} = G \cdot V_{in} + V_{ref}$$

$$V_{ref} = V_{out} - G \cdot V_{in} = 10V - 667.7 \cdot 22mV = -4.667V$$

3. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common-mode range. The common-mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common-mode input.

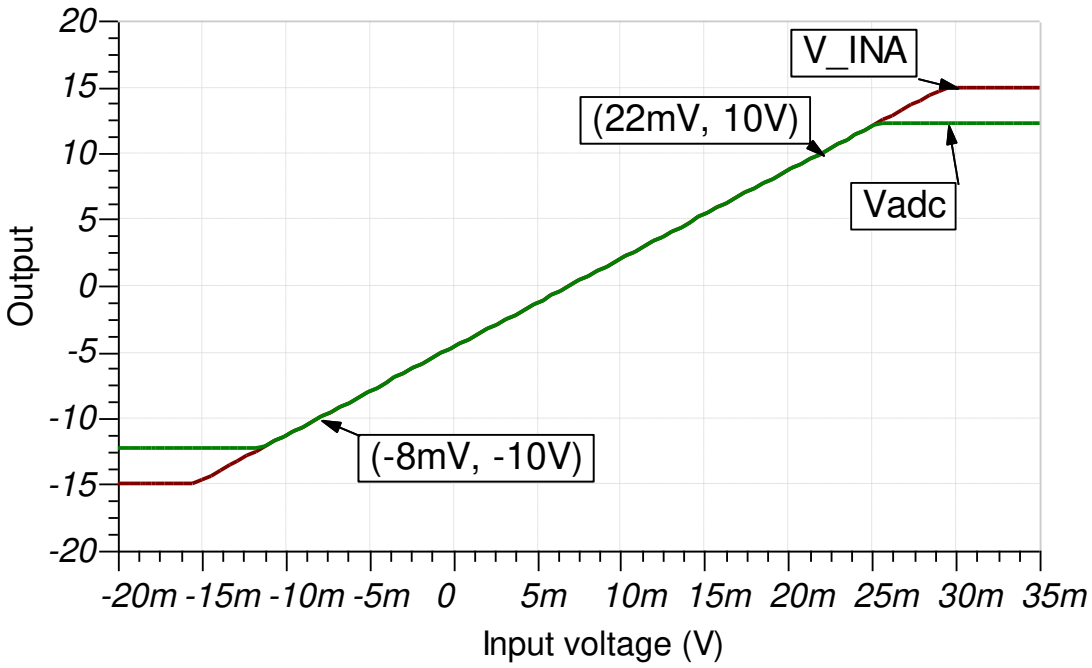


4. Find the value for C_{filt}, and R_{filt} using TINA-TI SPICE and the methods described in *Introduction of SAR ADC Front-End Component Selection* videos. The value of R_{filt} and C_{filt} shown in this document works for these circuits; however, when using different amplifiers new values are needed that are found using TINA-TI SPICE.
5. Select the RC filter between the INA828 and OPA827 based on your system requirements (f_{cRC} = 15.9kHz in this example).

$$f_{cRC} = \frac{1}{2\pi \cdot R_1 \cdot C_1} = \frac{1}{2\pi \cdot (10k\Omega) \cdot (1pF)} = 15.9kHz$$

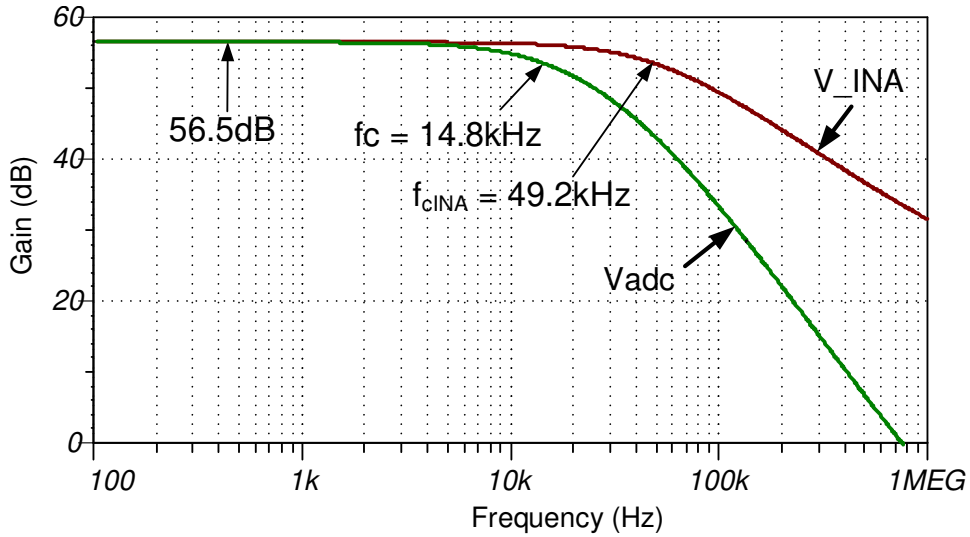
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –10V to +10V. See *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the Instrumentation Amplifier.



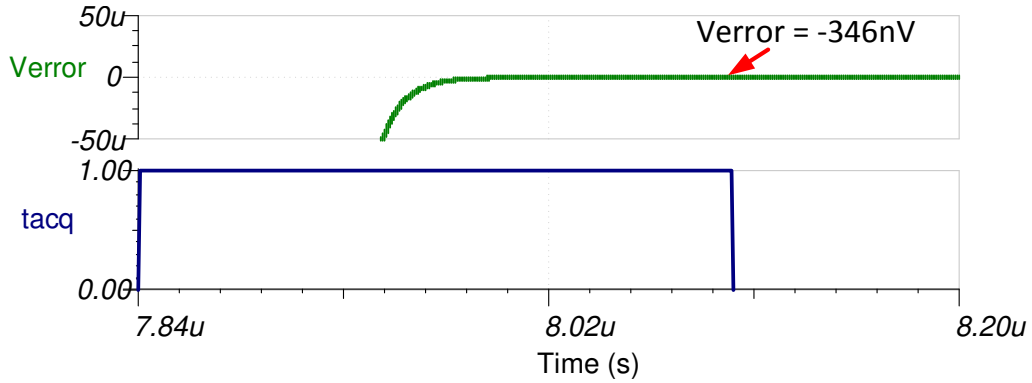
AC Transfer Characteristics

The bandwidth for this design is simulated to be 14.8kHz and the gain is 56.4dB (667.7V/V). The bandwidth limit is set by a combination RC filter (f_{cRC} = 15.9kHz) and the instrumentation amplifier (f_{cINA}=49.2kHz).



Transient ADC Input Settling Simulation (510kSPS)

The OPA827 buffer (22-MHz GBW) is used because it is capable of responding to the rapid transients from the charge kickback of the ADS8568. The op-amp buffer allows the system to achieve the ADS8568 maximum sampling rate of 510kSPS. The following simulation shows settling to a full-scale DC input signal with the INA828 and OPA827 buffer, and ADS8568. This type of simulation shows that the sample and hold kickback circuit is properly selected to meet desired ½ of a LSB (152µV). See *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



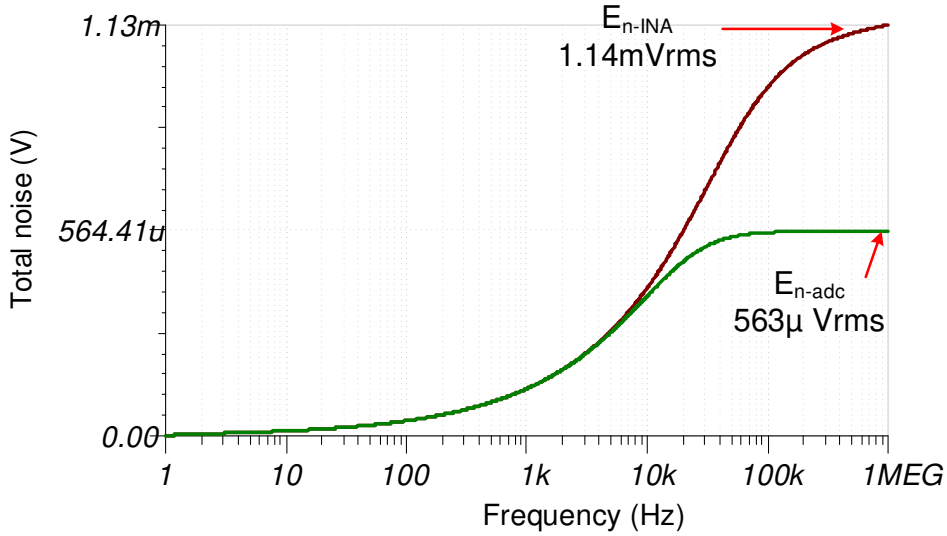
Noise Simulation

The section walks through a simplified noise calculation for a rough estimate. We neglect the noise from the OPA827 as the noise of the INA828 is dominant also neglect resistor noise in this calculation as it is attenuated for frequencies greater than 15.92kHz.

$$E_n = Gain \cdot \sqrt{e_{NI}^2 + \left(\frac{e_{NO}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = 667.7 \cdot \sqrt{\left(7nV/\sqrt{Hz}\right)^2 + \left(\frac{90nV/\sqrt{Hz}}{667.7}\right)^2} \cdot \sqrt{1.57 \cdot 14.8kHz} = 595\mu Vrms$$

Note that calculated and simulated match well (simulated = 563μV_{RMS}, calculated = 595μV_{RMS}). See *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations and *Calculating Total Noise for ADC Systems* for data converter noise.



Gain Error and Offset Estimates

The following offset and offset drift calculations are dominated by the instrumentation amplifier since it is in high gain. Gain error calculations include the gain error of the ADC and instrumentation amplifier. For offset and gain error, the maximum room temperature value is used. See *Statistics Behind Error Analysis* for details on system gain and offset error.

System Offset Calculation:

$V_{osi} = 50\mu V,\ V_{oso} = 250\mu V$ max at room temp

$G = 667.7V/V$

$$V_{osRTI} = V_{osi} + \frac{V_{oso}}{G} = 50\mu V + \frac{250\mu V}{667.7} = 50.4\mu V$$

$$V_{osRTO} = G \cdot V_{osRTI} = 667.7 \cdot 50.4\mu V = 33.6mV$$

$V_{os(System)} \approx 33.6mV$ total system offset is dominated by INA828 offset

System Offset Drift Calculation:

$V_{osDrift(INA828RTI)} = 0.5\mu V/^{o}C$

$V_{osDrift(INA828RTO)} = G \cdot V_{osDriftINA828RTI} = 667.7 \cdot 0.5\mu V/°C = 334\mu V/°C$

$V_{osDrift(System)} \approx 334\mu V/°C$ the INA drift dominates because of the high gain.

System Gain Error Calculation:

$GE_{ina} = \pm 0.15\%,$ max room temp INA828

$GE_{Rg} = \pm 0.1\%,$ Rg Tolerance

$GE_{ADS8568} = \pm 0.5\%,$ max room temp ADS8568

$$GE_{total} = \sqrt{(GE_{ina})^2 + (GE_{Rg})^2 + (GE_{ADS8568})^2} = \sqrt{(0.15\%)^2 + (0.1\%)^2 + (0.5\%)^2} = 0.53\%$$

System Gain Drift Calculation:

$$\frac{\Delta GE_{INA}}{\Delta T} \approx 50ppm/°C$$

$$\frac{\Delta GE_{Rg}}{\Delta T} \approx 20ppm/°C$$

$$\frac{\Delta GE_{ADC8568}}{\Delta T} \approx 6ppm/°C$$

$$\frac{\Delta GE_{System}}{\Delta T} \approx \sqrt{(50ppm/°C)^2 + (20ppm/°C)^2 + (6ppm/°C)^2} = 54.2ppm/°C$$

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8568	16-bit resolution, SPI, 500kSPS sample rate, single-ended input, simultaneous sampling, internal reference, programmable range up to ±12V.	16-bit, 8-channel, simultaneous-sampling, bipolar-input, SAR analog-to-digital converter (ADC)	Analog-to-digital converters (ADCs)
INA828	Bandwidth 1MHz (G=1), low noise 18nV/√ Hz, low offset ±40µV, low offset drift ±0.4µV/°C, low gain drift 0.1ppm/°C (Typical values)	50-µV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier	Instrumentation amplifiers
OPA827	Gain bandwidth 22MHz, low noise 4nV/√ Hz, low offset ±75µV, low offset drift ±0.1µV/°C (Typical values)	Low-noise, high-precision, JFET-input operational amplifier	Operational amplifiers (op amps)

Link to Key Files

Texas Instruments, SBAC215 source files, software support

Trademarks

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Analog Engineer's Circuit

Low-input bias-current front end SAR ADC circuit

Mike Stout

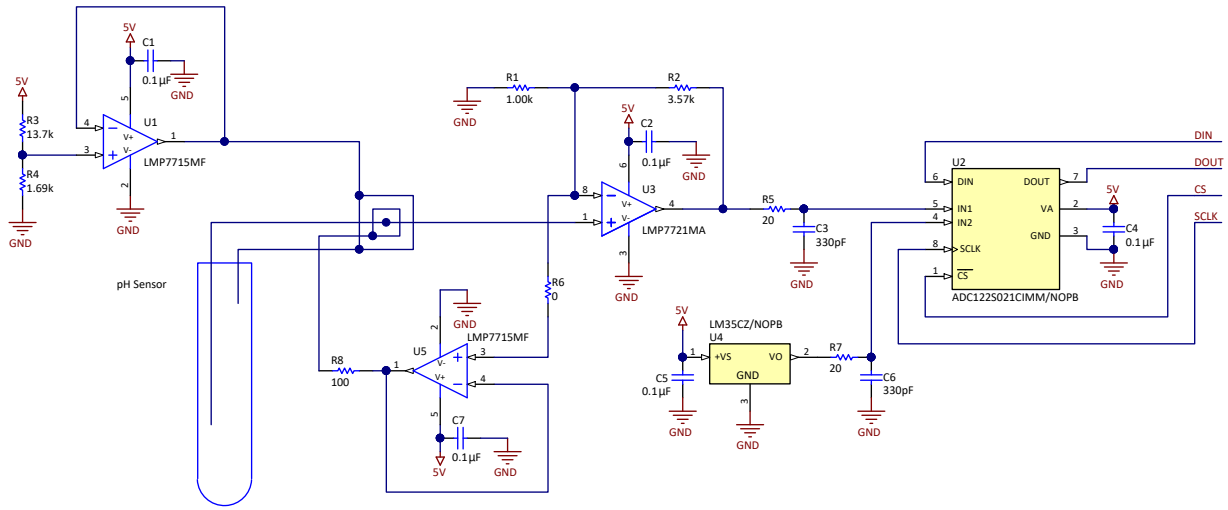
Input	ADC Input	Digital Output ADC122S021
VinMin = 0.03V	IN1 = 0.14	115 = 0x073
VinMax = 1.07V	IN1 = 4.88	3998 = 0xF9E
VinMin = 0V	IN2 = 0V	0 = 0x000
VinMax = 1V	IN2 = 1V	819 = 0x333

Power Supplies	
V+, VA	**V–**
5V	0V

Design Description

This design shows a low Ibias amplifier being used to drive a SAR ADC. A sensor with high output impedance requires an amplifier with a low input bias current to minimize errors. Examples of applications where this type of sensor can be used include *gas detectors*, *blood gas analyzers*, and *air quality detectors*. In this design, a pH probe is used for the sensor. The output impedance of a pH probe can be from 10MΩ to 1000MΩ. If a pH probe is used that has an output impedance of 10MΩ with an op amp that has 3nA of input bias current, then the error is due to the input bias current of the op amp is 30mV. Using the input signal amplitude and gain described in the *component selection* section, this 30mV equates to an error of about 2.9%. If an op amp with an input bias current of 3fA is used, the error is decreased to 30nV.

The output of the pH sensor does not quickly change, so a lower speed ADC can be used. The value from the pH sensor changes as the temperature changes so a two channel ADC was selected so that one channel can be used to monitor the temperature. The ADC122S021 used in this design is a 2-channel, 12-bit, ADC that can sample up to 200ksps.



Specifications

Specification	Calculated	Simulated	Measured
Ibias	20fA	118fA	20fA

Design Notes

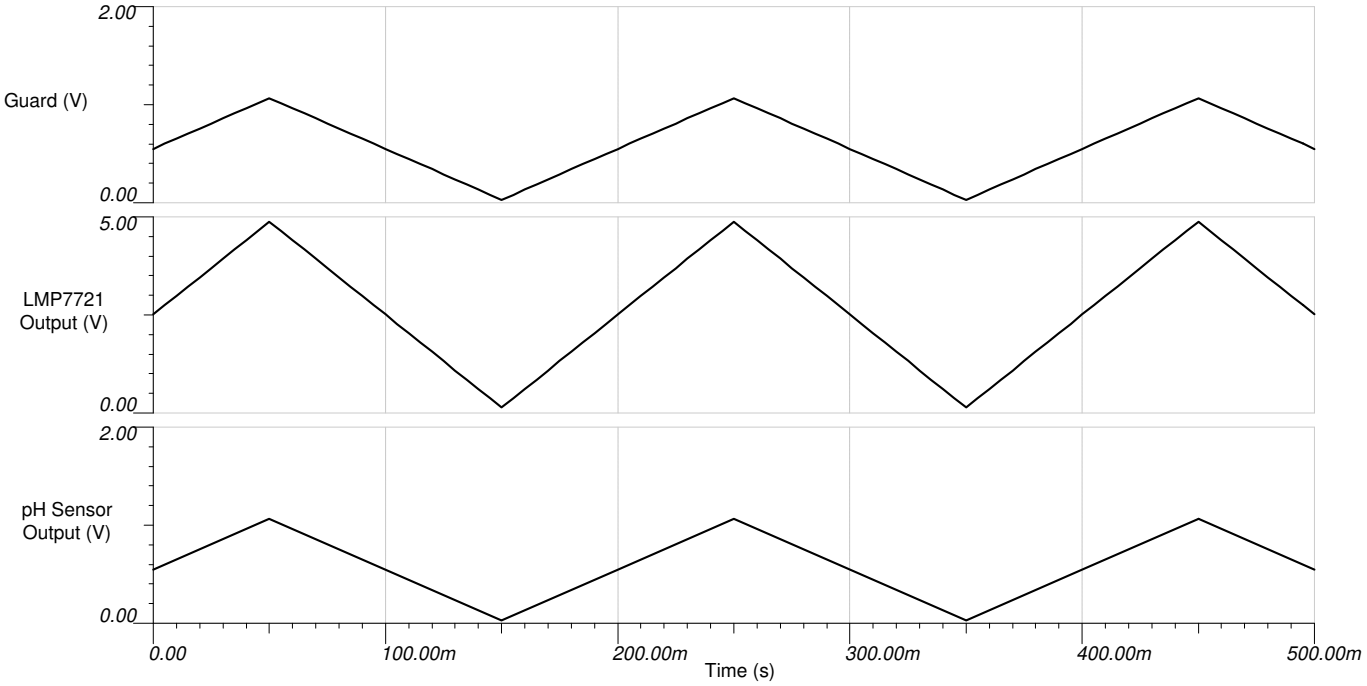
1. Use COG (NPO) capacitors for C3 and C6.
2. Each IC needs to have a bypass capacitor of 0.1µF.
3. PCB layout is very important. See the *LMP7721 Multi-Function Evaluation Board Users' Guide*.
4. The PCB must be clean. See the *LMP7721 Multi-Function Evaluation Board Users' Guide*.
5. For more information on low leakage design, see *Design femtoampere circuits with low leakage*.

Component Selection

1. The output voltage of a pH sensor changes as the temperature changes. At 0°C, the output voltage outputs 54.2mV/pH, at 25°C, the output voltage outputs 59.16mV/pH, and at 100°C, the output voltage outputs 74.04mV/pH. This means that the maximum swing of the pH sensor around the bias point of the pH sensor is ±518.3mV at 100°C. The maximum output of the LMP7721 needs to be limited to ±2.4V to allow for headroom. That sets the gain of the LMP7721 at:
   2.4V / 0.5183V = 4.6V/V
   Setting resistors R2 = 3.57kΩ and R1 = 1kΩ, sets this gain.
2. Since the input of the LMP7721 must be from 0V to 5V, the pH sensor needs to be biased above ground. Resistors R3 = 13.7kΩ and R4 = 1.69kΩ in a voltage divider configuration sets the input of U1 to:
   5V · 1.69kΩ / (1.69kΩ + 13.7kΩ) = 549mV
   U1 has a gain of 1V/V so the bias of the pH sensor is also at 549mV. Since the pH sensor can swing –518.3mV below the bias point, this keeps the input of the LMP7721 above ground. The output of the LMP7721 is centered at:
   0.549V · 4.6V/V = 2.52V
   and can swing ±2.4V above and below the center point.
3. U5 is used to set the voltage of the guard ring and is set with a gain of 1V/V and the input is the signal on the –IN pin of the LMP7721.
4. The output of the LMP7721 is connected to one of the inputs of the ADC122S021 SAR ADC. The sampling capacitor of the ADC is 33pF and the external capacitor placed next to the pin of the ADC must be 10 times larger, or 330pF. A small resistor of 20Ω is added in series to isolate the capacitor from the LMP7721.
5. Because the output of the pH sensor changes as the temperature changes the LM35, a temperature sensor, is connected to channel 2 of the ADC122S021. A 330pF capacitor along with a 20Ω series resistor is used on the output of the temperature sensor.

DC Transfer Characteristics

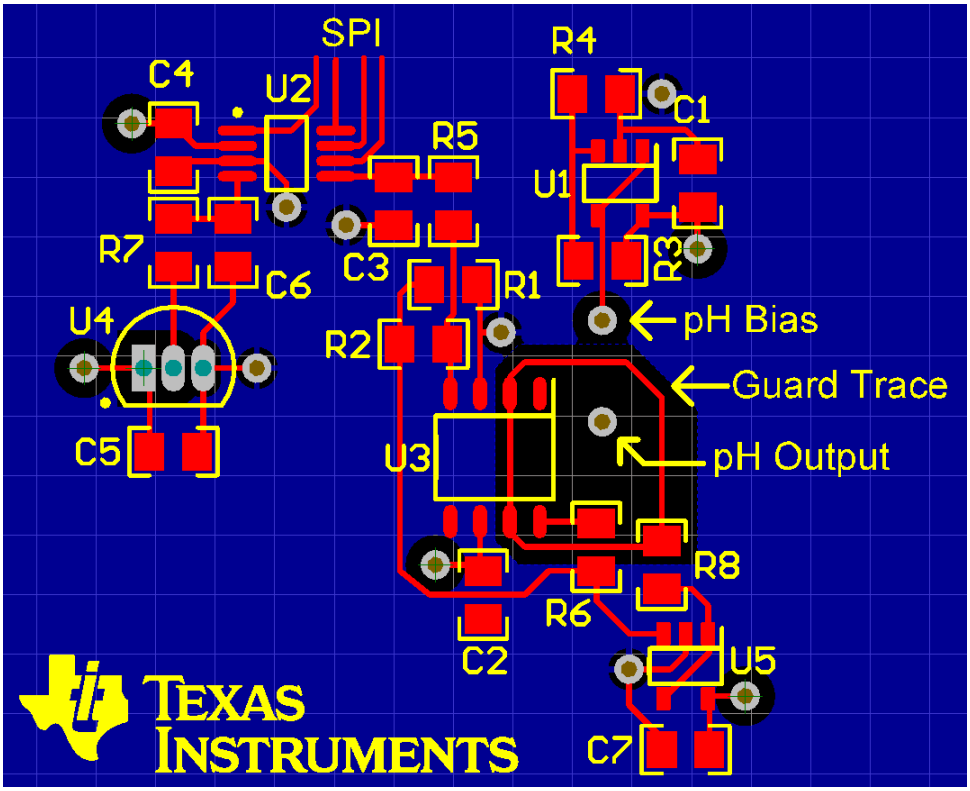
The following graph shows the pH sensor input to the LMP7721, the Guard voltage, and the LMP7721 output. This data is for 100°C, when the pH sensor output has the largest possible output swing.



Layout

The PCB layout is very important for a low Ibias circuit. Current leakage occurs between two traces when there a voltage potential between the traces. This is the reason for the guard trace. The guard trace is set to a voltage close to the input voltage to minimize the leakage between the input of the LMP7721 and the outside world. The LMP7721 includes two unused pins (pins 2 and 7) that can be used to simplify the layout of a guard trace.

The following image shows a sample layout. The output of the pH sensor and the +IN input of the LMP7721 are separated from the rest of the circuit by the guard trace, which is close to the input voltage. This minimizes the leakage on the input of the LMP7721. The bias of the pH sensor is located outside of the guard. Leakage between the bias point and the rest of the circuit is not important. Solder mask must not cover the area inside the guard trace. If there is a ground plane on the bottom side of the board or other internal planes, then the planes need to have a *keep out* area underneath the guard area.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADC122S021	12 bit, SPI, 2 channel, 50ksps to 200ksps, single ended input	www.ti.com/product/adc122s021	www.ti.com/adcs
LMP7721	Ultra-low input bias current of 3fA, with a specified limit of ±20fA at 25°C, offset voltage ±26µV, GBW 17MHz	www.ti.com/product/lmp7721	www.ti.com/opamps
LMP7715	Input offset voltage ±150µV, input bias current 100fA, input voltage noise 5.8nV/√Hz, gain bandwidth product 17MHz	www.ti.com/product/lmp7715	www.ti.com/opamps
LM35	Calibrated directly in degrees Celsius, Linear + 10mV/°C scale factor, 0.5°C verified accuracy (at 25°C), rated for full –55°C to 150°C range	www.ti.com/product/lm35	www.ti.com/temperature

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024) **Page**

- Updated the format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision * (February 2018) to Revision A (March 2019) **Page**

- Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page... 1

Analog Engineer's Circuit

High-Side Current Shunt Monitor Circuit to 3-V Single-Ended ADC

Art Kay

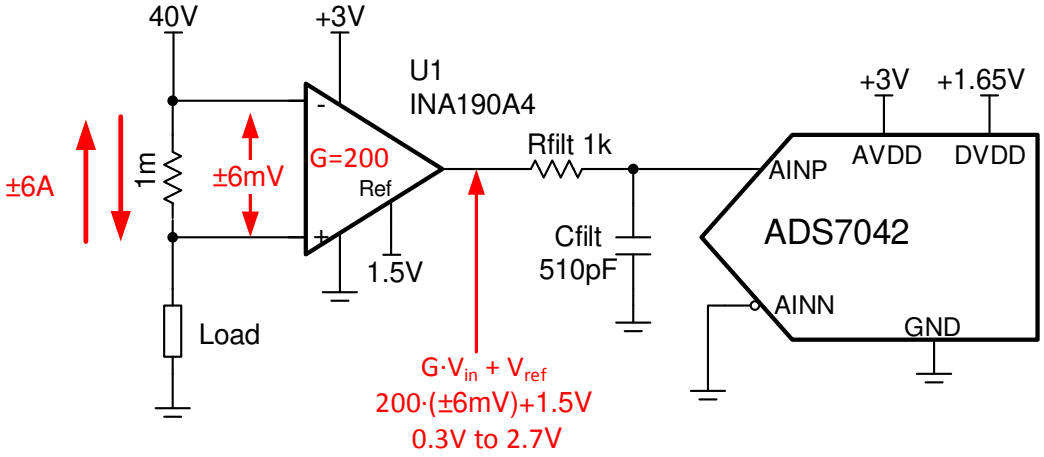
Input	ADC Input	Digital Output ADS7042
–6A	0.3V	$19A_H$, 410_d
+6A	2.7V	$E66_H$, 3686_d

Power Supplies

AVDD / V_{REF}	DVDD	Vsup
3.0V	1.65V	40V

Design Description

Current shunt monitors are amplifiers that are optimized to read small shunt voltages over very wide common mode ranges. This example application uses the INA190A4 to translate a ±6-A current into a 0-V to 3-V range for the ADC. Note that this is a high sided current measurement with a 40V common mode range. Detailed theory on current sensing is covered in *Using current sense amplifiers to solve today's current sensing design challenges*. Compared to other current shunt devices the INA190 has very low offset voltage, bias current, and drift. This excellent DC performance allows smaller for smaller input voltage ranges without compromising accuracy as the offset is small compared to the input signal. The use of small shunt resistors is an advantage as the power dissipated in the shunt is smaller for smaller resistors for a given current level. The ADS7042 is a 12-bit 1MSPS SAR ADC with a 3V analog input range. The design shown in this document can be modified for other data converters and input ranges. This design can be used a wide range of applications where current needs to be monitored such as notebook computers, cell phones, and battery management.



Specifications

Specification	Goal	Calculated	Simulated
Transient Settling	< 0.5LSB = 366µV	NA	0.94µV
Noise	NA	3.5mVrms	3.16mV
Bandwidth	NA	33kHz	35kHz

Design Notes

1. The tolerance in the shunt resistor, R_{SENSE}, will translate into a gain error. Choose the tolerance according to your error budget. Note that the maximum specified gain error for the INA190A4 is 0.3% and a common tolerance 1-m resistor is 0.5% to 1.0%.
2. Selection of the shunt resistor is covered in the component selection section. The objective is to minimize power dissipation while maintaining good accuracy.
3. Use a C0G capacitor for C_{FILT} to minimize distortion.
4. The example design is for a bidirectional current source (for example, ±6A). A similar approach can be followed for an unidirectional current source (for example, 0A to 12A). The main difference is that the reference input pin would connect to ground as opposed to 1/2 V_{REF}.

Component Selection

1. Choose Rsense Resistor and find Gain for the current sense amplifier (bidirectional current)

$$R_{sh} < \frac{P_{max}}{(I_{max})^2} = \frac{50mW}{(6A)^2} = 1.38m\Omega$$

$$Choose\ Rsh\ =\ 1m\Omega$$

$$\pm V_{out(\text{range})} = \pm\frac{V_{REF}}{2} = \pm\frac{3V}{2} = \pm 1.5V$$

$$G_{INA} = \frac{\pm V_{out(\text{range})}}{I_{load(\max)} \cdot R_{sh}} = \frac{\pm 1.5V}{6A \cdot 1m\Omega} = 250V/V$$

Select INA190A4, $G\ =\ 200V/V$, Common Mode Range : $-0.2\ V\ to\ 40\ V$

2. Calculate the current sense amplifier output range

$$V_{INA\_outmax} = G_{INA} \cdot \left(I_{load(\max)} \cdot R_{sh}\right) + \frac{V_{REF}}{2} = 200V/V \cdot (6A \cdot 1m\Omega) + \frac{3V}{2} = 2.7V$$

$$V_{INA\_outmin} = G_{INA} \cdot \left(I_{load(\min)} \cdot R_{sh}\right) + \frac{V_{REF}}{2} = 200V/V \cdot (-6A \cdot 1m\Omega) + \frac{5V}{2} = 0.3V$$

3. Find the INA190 output swing from the data sheet.

   Swing to Positive Rail = 3V - 40mV = 2.96V

   Swing to Negative Rail = 1mV

   The output is scaled for 0.3V to 2.7V, so this design has significant margin.

   If desired, a larger shunt resistor could be used to expand the usable range.

4. Offset Error impact on system error.

   OutputOffsetINA = $V_{os} \cdot Gain = 15\mu V \cdot 200 = 3mV$

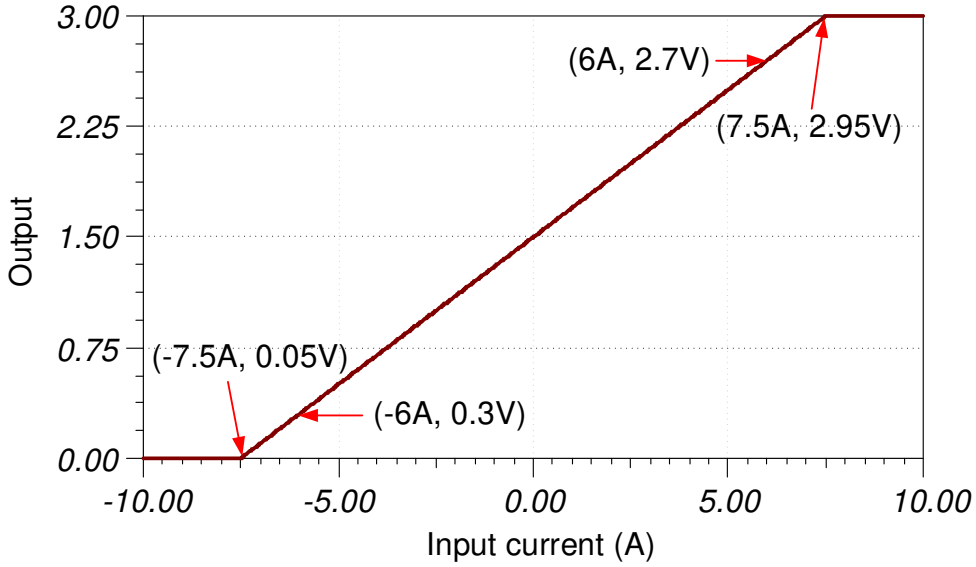
   OfsetADS7042 = $3LSB \cdot 366\,\mu V/LSB = 1.1mV$

$$TotalOffsetRSS = \sqrt{(3mV)^2 + (1.1mV)^2} = 3.2mV$$

$$Error(\%FSR) = \frac{3.2mV}{3V} \cdot 100 = 0.11\%\ \text{of FSR}$$

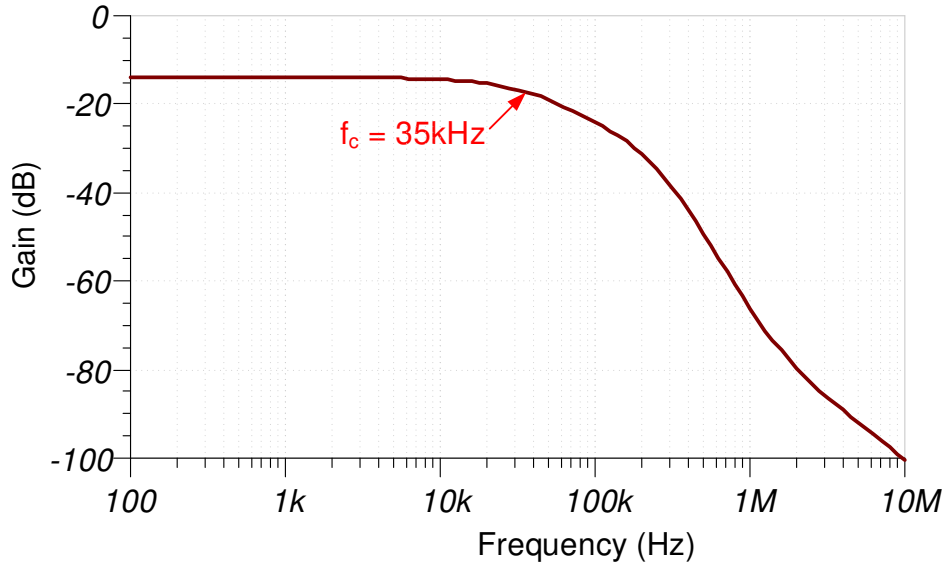
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –7.5A to +7.5A. The required linear range is ±6A, so this circuit meets the requirement with design margin.



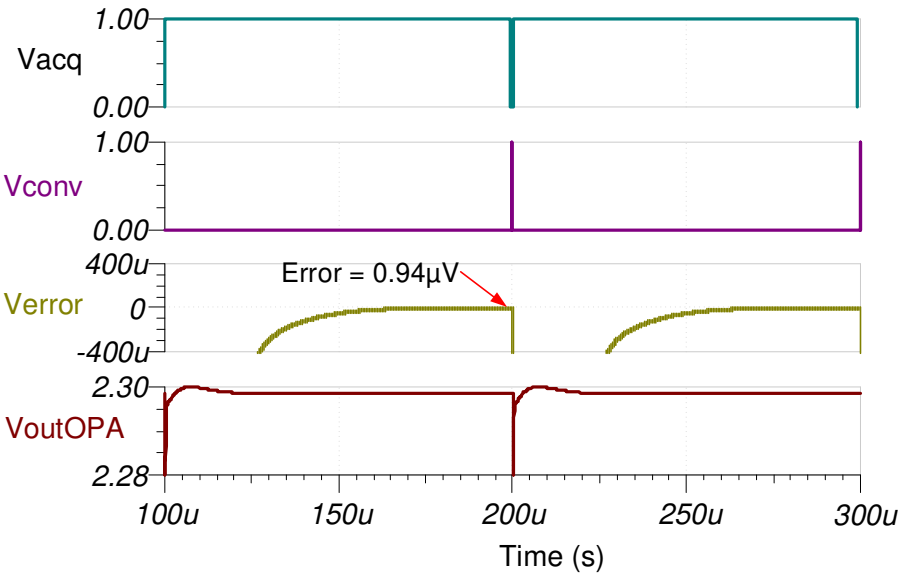
AC Transfer Characteristics

The data sheet specified bandwidth of 33kHz for the INA190A4 closely matches the simulated 35kHz bandwidth. The input ADC filter is designed to minimize charge kickback and does not limit the bandwidth ($f_{c(ADC\ filter)}$ = 312kHz). See *TI Precision Labs - Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The transient ADC simulation is performed for a near full scale input (VinADC = 2.3V), for a 100-kHz sampling rate. Note that the sampling rate needed to be adjusted as the INA190 does not have sufficient bandwidth to respond to the transient charge kickback from the ADC at full sampling rate. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



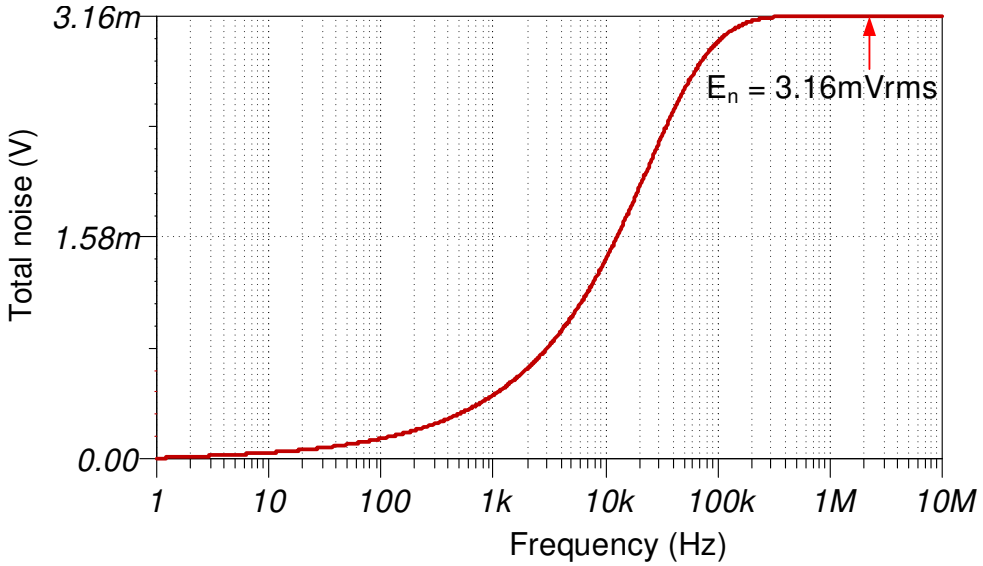
Noise Simulation

The noise hand calculation follows. This calculation assumes that the filter is a first order but inspection of the bandwidth simulation shows a more complex response.

$$E_n = G_n \cdot e_n \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = 200 \cdot 75\,nV/\sqrt{Hz} \cdot \sqrt{1.57 \cdot 35kHz} = 3.5mVrms$$

Note that the calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating the Total Noise for ADC Systems* for data converter noise.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS7042	12-bit resolution, SPI, 1MSPS sample rate, single-ended input, AVDD/ Vref input range 1.6V to 3.6V.	12-Bit 1MSPS Ultra-Low-Power Ultra-Small-Size SAR ADC With SPI Interface	Analog-to-digital converters (ADCs)
INA190	Low Supply voltage (1.7V to 5.5V), Wide Common-Mode (-0.2V to 40V), Low Offset Voltage (Vos < 15µV Max), Low Bias Current (500pA typ).	40-V, Bidirectional, Ultraprecise Current Sense Amplifier with Picoamp IB and ENABLE	Analog current-sense amplifiers

Link to Key Files

Texas Instruments, TINA source files, software support

Trademarks

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Analog Engineer's Circuit

Two-Wire PT100 RTD Measurement Circuit With Low-Side Reference

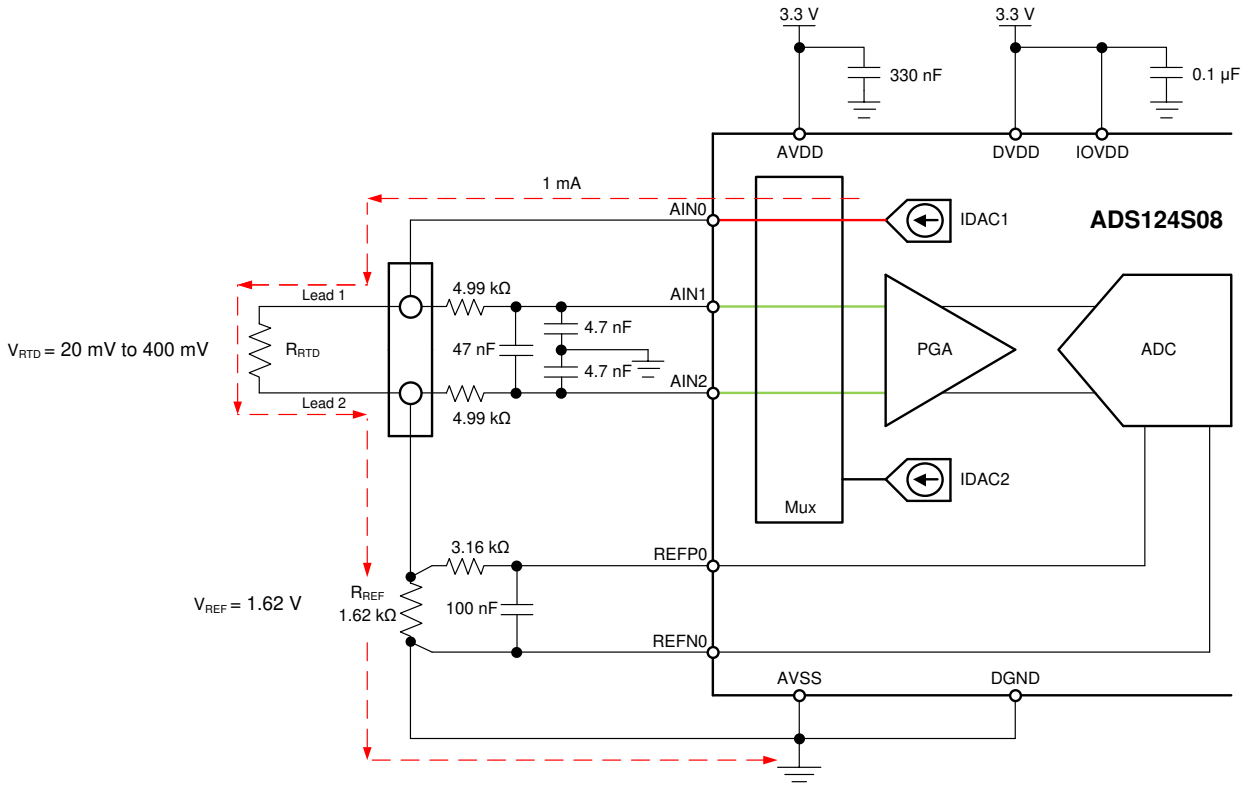
Joseph Wu

Power Supplies

AVDD	AVSS, DGND	DVDD, IOVDD
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a two-wire RTD using the ADS124S08. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6-*

and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.
7. This design shows connections to three input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The two-wire RTD measurement is the least accurate of RTD measurements because the lead resistance error cannot be removed. For measurements with more accurate RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01°C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations.

$$V_{AIN1} = I_{IDAC1} \times (R_{RTD} + R_{REF}) = 1mA \times (400\Omega + 1620\Omega) = 2.02V \quad (1)$$

$$V_{AIN2} = I_{IDAC1} \times R_{REF} = 1mA \times 1620\Omega = 1.62V \quad (2)$$

$$V_{INMAX} = 1mA \times 400\Omega = 400mV \quad (3)$$

3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel,*

4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference data sheet shows, the absolute input voltage must satisfy the following:

$$AVSS + 0.1V + [|V_{INMAX} \times (Gain - 1) \div 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX} \times (Gain - 1) \div 2] \quad (4)$$

$$0V + 0.15V + [|V_{INMAX} \times (Gain - 1) \div 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX} \times (Gain - 1) \div 2] \quad (5)$$

$$0.75 < V_{AIN1}, V_{AIN2} < 2.55V \quad (6)$$

Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02V and 1.62V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

$$AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V \quad (7)$$

$$0V < V_{AIN0} < 2.7V \quad (8)$$

With the previous result, the output compliance of the IDAC is satisfied.

4. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 times higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 times higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50Hz and 60Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

$$f_{IN\_DIFF} = \frac{1}{[2 \times \pi \times C_{IN\_DIFF}(R_{RTD} + 2 \times R_{IN})]} \quad (9)$$

$$f_{IN\_CM} = \frac{1}{[2 \times \pi \times C_{IN\_CM}(R_{RTD} + R_{IN} + R_{REF})]} \quad (10)$$

For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5kHz.

The bandwidth for the reference input filtering is approximated in the following equation.

$$f_{REF} = \frac{1}{[2 \times \pi \times C_{REF}(R_{RTD} + R_{IN\_REF})]} \quad (11)$$

For the reference input filtering, R_{IN_REF} = 3.16kΩ and C_{REF} = 100nF. This sets the reference filter bandwidth to 330Hz. Because REFN0 is set to ground, the common-mode filtering is removed. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

For an in-depth analysis of component selection for input filtering, see the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$Output\ Code\ = 2^{23} \times Gain \times \left(\frac{V_{RTD}}{V_{REF}}\right) = 2^{23} \times Gain \times (I_{IDAC1} \times R_{RTD}) \div (I_{IDAC1} \times R_{REF}) = 2^{23} \times Gain \times (R_{RTD} \div R_{REF}) \quad (12)$$

$$R_{RTD} = R_{REF} \times \left[\frac{Output\ Code}{\left(Gain \times 2^{23}\right)}\right] \quad (13)$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Two-Wire PT100 RTD Measurement Circuit With Low-Side Reference Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	12h	Positive reference buffer enabled, negative reference buffer disabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{DRDY}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;// RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
05// Write to 6 registers
12// Select AINP = AIN1 and AINN = AIN2
0A// PGA enabled, Gain = 4
14// Continuous conversion mode, low-latency filter, 20-SPS data rate
12// Positive reference buffer enabled, negative reference buffer disabled
  // REFP0 and REFN0 reference selected, internal reference always on
07// IDAC magnitude set to 1 mA
F0;// IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low; // For verification, read back configuration registers
Send 22// RREG starting at 02h address
05// Read from 6 registers
00 00 00 00 00 00;// Send 6 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	24-bit, 4-kSPS, 12-ch delta-sigma ADC with PGA and voltage reference for sensor measurement	Precision ADCs
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	16-bit, 4-kSPS, 12-ch delta-sigma ADC with PGA and voltage reference for sensor measurement	

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module, overview
- Texas Instruments, *ADS1x4S08 Evaluation Module*, user's guide
- Texas Instruments, ADS1x4S08 Firmware, example code
- Texas Instruments, *A Basic Guide to RTD Measurements*, application note
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*, application note

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2020) to Revision B (September 2024)	Page
• Updated the format for tables, figures, equations, and cross-references throughout the document	1

Changes from Revision * (December 2018) to Revision A (March 2020)	Page
• Changed schematic to remove filtering from REFN0	1
• Changed bandwidth calculation for reference input filter	1
• Changed Register Settings Table to disable negative reference buffer	1
• Changed Pseudo Code Example to disable negative reference buffer	1

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Analog Engineer's Circuit

Three-Wire PT100 RTD Measurement Circuit With High-Side Reference and Two IDAC Current Sources

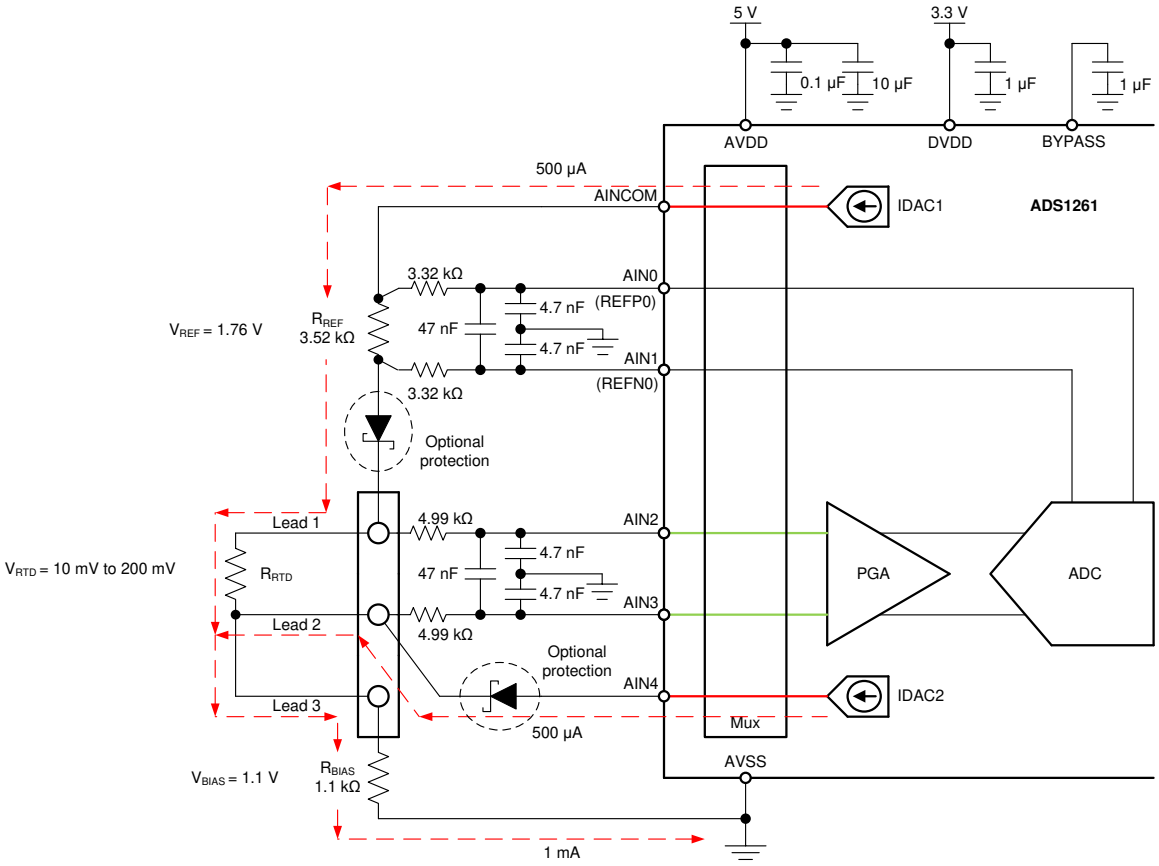
Joseph Wu and Chris Hall

Power Supplies

AVDD	AVSS, DGND	DVDD
5V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD using the ADS1261. This design uses a ratiometric measurement with a high-side reference using two matched excitation current sources for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab and field instrumentation,* and *factory automation and control.* For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements.*



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. Place 0.1-µF and 10-µF capacitors between AVDD and AVSS (ground). Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from BYPASS to the ground plane. See the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet for details on power-supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 10-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices.*
7. This design shows connections to six input pins of the ADC multiplexer. Use the remaining analog inputs for other measurements, such as bridge measurements with AC excitation.
8. Because of lead-resistance cancellation, the three-wire measurement offers more accuracy than comparable *two-wire RTD measurements.* Using a high-side reference for this design significantly reduces the error from IDAC current mismatch seen in *three-wire RTD measurements using a low-side reference.* For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements.*

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Use two matched IDAC current sources to cancel the lead-resistance error.

   Two matched IDAC current sources are used for lead-resistance cancellation. Assuming the resistances of lead 1 and lead 2 are the same, and the currents of IDAC1 and IDAC2 are the same, then the lead-resistance error is canceled. Cancellation can be shown through the measured voltages at AIN2 and AIN3.

   IDAC1 drives current into the reference resistor R_{REF} and the RTD through lead 1. IDAC2 drives current into lead 2. First, assume that the input protection shown in the circuit has no voltage drop. The voltages at AIN2 and AIN3 are calculated with the following equations.

   $$V_{AIN2} = I_{IDAC1} \times (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})$$

   $$V_{AIN3} = I_{IDAC2} \times R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})$$

   The measurement of the ADC is the difference between AIN2 and AIN3, which is the subtraction of the previous equations.

   $$V_{AIN2} - V_{AIN3} = [I_{IDAC1} \times (R_{LEAD1} + R_{RTD} + R_{BIAS}) + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})] - [I_{IDAC2} \times R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \times (R_{LEAD3} + R_{BIAS})]$$

   Then, the R_{LEAD3} and R_{BIAS} terms drop out.

   $$V_{AIN2} - V_{AIN3} = I_{IDAC1} \times (R_{LEAD1} + R_{RTD}) - I_{IDAC2} \times R_{LEAD2}$$

If R_{LEAD1} and R_{LEAD2} are equal and I_{IDAC1} and I_{IDAC2} are equal (to become I_{IDAC}), then the lead resistance errors cancel to leave the following equation:

$$V_{AIN2} – V_{AIN3} = I_{IDAC} × R_{RTD}$$

3. Determine values for the IDAC excitation currents and reference resistor.

   The excitation current source in this design is selected to be 500µA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire wound elements. With 500µA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.005°C.

   After selecting the IDAC current magnitude, set R_{REF} = 3.52kΩ. Using a 500µA excitation current sets the reference at 1.76V and the maximum RTD voltage is 200mV. With these values, the PGA gain can be set to eight so that the maximum RTD voltage is near, but not exceeding, the positive full scale range without exceeding.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP and REFN pins (AIN0 and AIN1) are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Note that for a high-side reference, the current flowing through the reference resistor and the RTD are the same. For a *three-wire RTD measurement with a low-side reference*, the IDAC current mismatch is a large contributor to the error. In this design, the mismatch only leads to a smaller error in the lead-resistor cancellation, rather than a larger gain error in the RTD measurement.

4. Set R_{BIAS} and verify that the design is within the range of operation of the ADC.

   Once the reference resistance, IDAC current magnitudes, and ADC gain are set, select the R_{BIAS} resistance to set the bias voltage of the input measurement. Normally, R_{BIAS} is selected to set the input to the mid-supply voltage. However, there is a large total sum of the voltage drop across the reference resistor, the RTD resistance, the bias resistor, and any optional input protection used in the circuit. It is important that the R_{BIAS} input offset is high enough to keep the RTD measurement voltage in the PGA input range, but not too high so that the excitation current output pin is within the compliance voltage of the IDAC.

   Setting R_{BIAS} of 1.1kΩ meets this requirement. Using the maximum RTD resistance of 400Ω, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

   $$V_{AIN2} = (I_{IDAC1} × R_{RTD}) + [(I_{IDAC1} + I_{IDAC2}) × R_{BIAS}] = 1.3V$$

   $$V_{AIN3} = (I_{IDAC1} + I_{IDAC2}) × R_{BIAS} = 1mA × 1.1kΩ = 1.1V$$

   $$V_{INMAX} = 500µA × 400Ω = 200mV$$

   First, verify that the voltage at AIN2 and AIN3 are within the input range of the PGA given that the gain is 8 and that AVDD is 5V and AVSS is 0V. As shown in the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet, the absolute input voltage must satisfy the following:

   $$AVSS + 0.3V + [|V_{INMAX}| × (Gain – 1) ÷ 2] < V_{AIN2}, V_{AIN3} < V_{AVDD} – 0.3V – [|V_{INMAX}| × (Gain – 1) ÷ 2]$$

   $$0.3V + [|0.2V| × (8 – 1) ÷ 2] < V_{AIN2}, V_{AIN3} < 5V– 0.3V – [|0.2V| × (8 – 1) ÷ 2]$$

   $$1V < V_{AIN2}, V_{AIN3} < 4V$$

   Because the maximum and minimum input voltage seen at AIN2 and AIN2 (1.1V and 1.3V) are between 1V and 4V, the inputs are in the PGA operating range.

Second, verify that the IDAC output pin voltages are within the compliance voltage. The IDAC current output voltage is highest and most limited by output compliance when the RTD voltage is at a maximum as the following equation shows. As before, we can ignore the low voltage contribution of the lead resistance.

$V_{IDAC1} = V_{BIAS} + V_{RTD} + V_D + V_{REF}$

$V_{IDAC1} = 1V + 0.2V + 0.3V + 1.76V = 3.26V$

The maximum RTD voltage is 200mV and a drop of 300mV is assumed for an input protection Schottky diode (V_D).

The IDAC current compliance range is listed in the *Electrical Characteristics* table under the *Current Sources* section of the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet. The IDAC current compliance range is given by the following equation.

$AVSS < V_{IDAC1} < AVDD – 1.1V$

In this example design, AVDD is 5V and reduces the following:

$0V < V_{IDAC1} < 3.9V$

With the previous equation, the output compliance of the IDAC1 pin is satisfied. Because the IDAC2 pin is always at a lower voltage than IDAC1 voltage, both current sources are in the compliance range.

The schematic is shown with two optional input protection diodes. These low V_F diodes provide input fault protection for the IDAC current sources, and may be replaced with series resistances. If series resistance is used, then the added diode voltage of 0.3V is replaced with the voltage from I_{IDAC} across the new series resistance for equations verifying the IDAC output pin compliance voltage.

Third, verify that the reference voltage is within the reference voltage input range for the ADC. For the ADS1261, the differential reference input voltage range is shown in the *Recommended Operating Conditions* of the *ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors* data sheet as the following equation.

$0.9V < V_{REFP} – V_{REFN} < AVDD – AVSS$

$0.9V < 1.76V < 5V$

Also verify the absolute negative reference input voltage and verify the absolute positive reference input voltage with the following equations. Calculations show that the reference voltages are within the input range of the ADC reference.

$AVSS – 0.05V < V_{REFN} = V_{BIAS} + V_{RTD} + V_D < V_{REFP} – 0.9V$

$–0.05V < 1.5V < 4.1V$

$V_{REFN} < V_{REFP} = V_{BIAS} + V_{RTD} + V_D + V_{REF} < AVDD + 0.05V$

$1.5V < 3.26V < 5.05V$

5. Select values for the differential and common-mode input filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS1261. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

$$f_{IN\_DIFF} = 1 \div [2 \times \pi \times C_{IN\_DIFF} (R_{RTD} + 2 \times R_{IN})]$$

$$f_{IN\_CM} = 1 \div [2 \times \pi \times C_{IN\_CM} (R_{RTD} + R_{IN} + R_{BIAS})]$$

For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.4kHz.

Similarly, the bandwidth for the reference input filtering is approximated in the following equations.

$$f_{REF\_DIFF} = 1 \div [2 \times \pi \times C_{REF\_DIFF} \times (R_{REF} + 2 \times R_{IN\_REF})]$$

$$f_{REF\_CM} = 1 / \{2 \times \pi \times C_{REF\_CM} \times [R_{IN\_REF} + (½ \times R_{REF}) + R_{RTD} + R_{BIAS}]\}$$

For the reference input filtering, R_{IN_REF} = 3.32kΩ, C_{REF_DIFF} = 47nF, and C_{REF_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.3kHz. Matching the ADC input and reference input filtering is not always possible in a design. However, keeping the bandwidths close may reduce noise in the measurement.

For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$\text{Output Code} = 2^{23} \times \text{Gain} \times (V_{RTD} \div V_{REF}) = 2^{23} \times \text{Gain} \times (I_{IDAC1} \times R_{RTD}) \div (I_{IDAC1} \times R_{REF}) = 2^{23} \times \text{Gain} \times (R_{RTD} \div R_{REF})$$

$$R_{RTD} = R_{REF} \times [\text{Output Code} \div (\text{Gain} \times 2^{23})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a 3-Wire RTD Measurement with High-Side Reference and Two IDAC Current Sources Using the ADS1261

Register Address	Register Name	Setting	Description
02h	MODE0	24h	20SPS, FIR digital filter
03h	MODE1	01h	Normal mode, Continuous conversion, 50 µs delay between conversions
04h	MODE2	00h	GPIOs disabled
05h	MODE3	00h	No power-down, no STATUS or CRC byte, timeout disabled
06h	REF	1Ah	Internal reference enabled, REFP = AIN0, REFN = AIN1
0Dh	IMUX	4Ah	IDAC2 = AIN4, IDAC1 = AINCOM
0Eh	IMAG	44h	IMAG2 = IMAG1 = 500µA
0Fh	RESERVED	00h	Reserved
10h	PGA	03h	PGA enabled, Gain = 8
11h	INPMUX	34h	Select AIN_P = AIN2 and AIN_N = AIN3
12h	INPBIAS	00h	VBIAS voltages and burnout current sources disabled

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS1261 in continuous conversion mode. The dedicated $\overline{DRDY}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS1261 example code is available from the ADS1261 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;//RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
04// Write to 5 registers
24// 20SPS, FIR digital filter
01// Normal mode, Continuous conversion, 50µs delay between conversions
00// GPIOs disabled
00// No power-down, no STATUS or CRC byte, timeout disabled
1A;// Internal reference enabled, REFP = AIN0, REFN = AIN1
Set CS high;
Set CS low;// Configure the device, IDACs
Send 4D// WREG starting at 0Dh address
05// Write to 6 registers
4A// IMUX2 = AIN4, IMUX1 = AINCOM
44// IMAG2 = IMAG1 = 500µA
00// RESERVED
03// PGA enabled, Gain = 8
34// Select AINP = AIN2 and AINN = AIN3
00;// VBIAS voltages and burn-out current sources disabled
Set CS high;
Set CS low;// For verification, read back configuration registers
Send 22// RREG starting at 02h address
10// Read from 17 registers
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00;// Send 17 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS1261	24-bit 40kSPS 10-ch delta-sigma ADC with PGA, Vref, 2 × IDACs, and AC excitation for factory automation	24-bit, 40-kSPS, 10-ch delta-sigma ADC with PGA, VREF, IDACs & AC excitation for factory automation	Precision ADCs

Additional Resources

- Texas Instruments, ADS1261 Evaluation Module, product overview
- Texas Instruments, *ADS1261 and ADS1235 Evaluation Module*, user's guide
- Texas Instruments, *24-bit, 40-kSPS, 10-ch delta-sigma ADC with PGA, VREF, IDACs & AC excitation for factory automation*, product overview
- Texas Instruments, *A Basic Guide to RTD Measurements*, application note
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*, application note

Trademarks

Analog Engineer's Circuit

Four-Wire PT100 RTD Measurement Circuit With Low-Side Reference

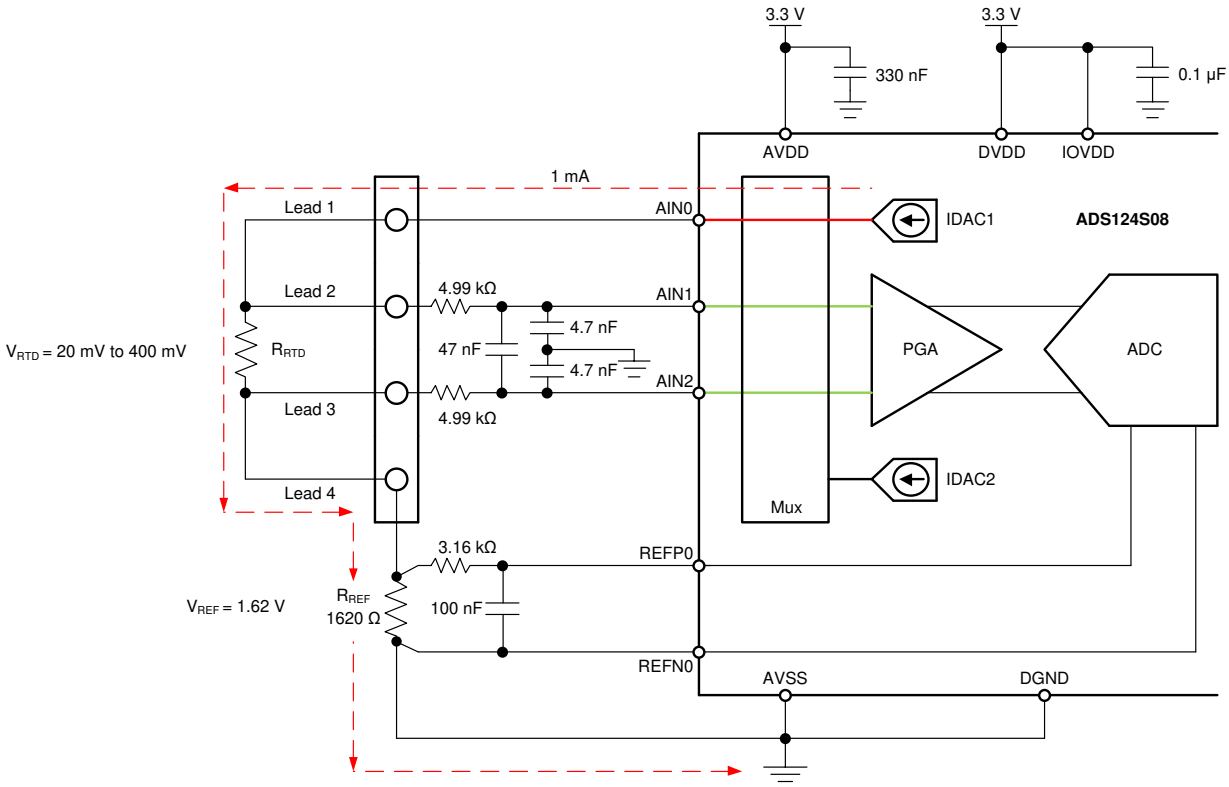
Joseph Wu

Power Supplies

AVDD	AVSS, DGND	DVDD, IOVDD
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a four-wire RTD using the ADS124S08. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. The four-wire RTD measurement is the most accurate of the RTD wiring configurations because the lead-resistance is not a factor in the measurement. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.
7. This design shows connections to three input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The design for the four-wire RTD measurement is identical to the two-wire RTD measurement but requires four terminal connections and eliminates the lead-resistance error. For measurements with different RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   In this design, the IDAC current source drives the RTD through lead 1. The current exits the RTD through lead 4 and is shunted by R_{REF} to create a ratiometric measurement. The measurement is made between lead 2 and lead 3 by the ADC, making a Kelvin connection to remove the lead resistance error. With this four-terminal sensing, the 4-wire RTD measurement is the most accurate of the RTD wiring configurations.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01°C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

Using the maximum RTD resistance, the ADC input voltages are calculated in the following:

$V_{AIN1} = I_{IDAC1} \times (R_{RTD} + R_{REF}) = 1mA \times (400\Omega + 1620\Omega) = 2.02V$

$V_{AIN2} = I_{IDAC1} \times R_{REF} = 1mA \times 1620\Omega = 1.62V$

$V_{INMAX} = 1mA \times 400\Omega = 400mV$

3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet shows, the absolute input voltage must satisfy the following:

   $AVSS + 0.15V + [|V_{INMAX}| \times (Gain - 1) \div 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) \div 2]$

   $0V + 0.15V + [|V_{INMAX}| \times (Gain - 1) \div 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) \div 2]$

   $0.75 < V_{AIN1}, V_{AIN2} < 2.55V$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02V and 1.62V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

   $0V < V_{AIN0} < 2.7V$

   With the above result, the output compliance of the IDAC is satisfied.

4. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $f_{IN\_DIFF} = 1 \div [2 \times \pi \times C_{IN\_DIFF} (R_{RTD} + 2 \times R_{IN})]$

   $f_{IN\_CM} = 1 \div [2 \times \pi \times C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$

For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5kHz.

The bandwidth for the reference input filtering is approximated in the following equation.

$$f_{REF} = 1 \div [2 \times \pi \times C_{REF} \times (R_{REF} + R_{IN\_REF})]$$

For the reference input filtering, R_{IN_REF} = 3.16kΩ and C_{REF_DIFF} = 100nF. This sets the reference filter bandwidth to 330Hz. Because REFN0 is set to ground, the common-mode filtering is removed. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

For an in-depth analysis of component selection for input filtering, see the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$\text{Output Code} = 2^{23} \times \text{Gain} \times (V_{RTD} / V_{REF}) = 2^{23} \times \text{Gain} \times (I_{IDAC1} \times R_{RTD}) \div (I_{IDAC1} \times R_{REF}) = 2^{23} \times \text{Gain} \times (R_{RTD} \div R_{REF})$$

$$R_{RTD} = R_{REF} \times [\text{Output Code} \div (\text{Gain} \times 2^{23})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or look-up table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Four-Wire PT100 RTD Measurement Circuit with Low-Side Reference Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	12h	Positive reference buffer enabled, negative reference buffer disabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{DRDY}$ pin indicates availability of new conversion data. Pseudo code is shown

without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;// RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
05// Write to 6 registers
12// Select AINP = AIN1 and AINN = AIN2
0A// PGA enabled, Gain = 4
14// Continuous conversion mode, low-latency filter, 20-SPS data rate
12// Positive reference buffer enabled, negative reference buffer disabled
  // REFP0 and REFN0 reference selected, internal reference always on
07// IDAC magnitude set to 1 mA
F0;// IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low; // For verification, read back configuration registers
Send 22// RREG starting at 02h address
05// Read from 6 registers
00 00 00 00 00 00;// Send 6 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	24-bit, 4kSPS, 12-ch delta-sigma ADC with PGA and voltage reference for sensor measurement	Precision ADCs
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	16-bit, 4kSPS, 12-ch delta-sigma ADC with PGA and voltage reference for sensor measurement	

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Resources

- Texas Instruments, *ADS124S08 Evaluation Module*, support
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*, user's guide
- Texas Instruments, *ADS1x4S08 Firmware Example Code*, support
- Texas Instruments, *A Basic Guide to RTD Measurements Application Report*, application note
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices Application Report*, application note

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2020) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (December 2018) to Revision A (March 2020)	Page
• Changed schematic to remove filtering from REFN0	1
• Changed bandwidth calculation for reference input filter	1
• Changed Register Settings Table to disable negative reference buffer	1
• Changed Pseudo Code Example to disable negative reference buffer	1

Trademarks

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Analog Engineer's Circuit

Two-channel, K-type thermocouple measurement circuit with internal temperature sensor CJC

Joseph Wu

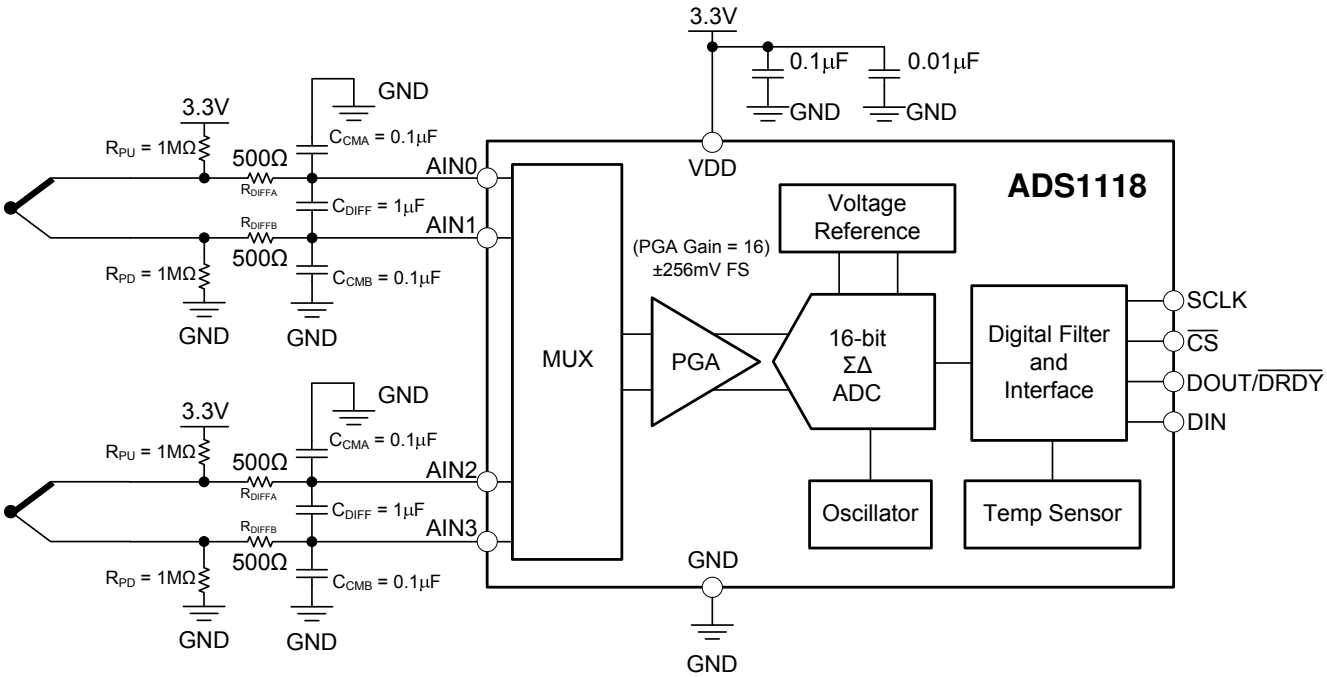
Input Measurement	ADC Input Voltage	ADC Digital Output
T = –270°C	AINP – AINN = –6.5mV	$FCC0_H$ or -832_{10}
T = 1370°C	AINP – AINN = 55mV	$1B80_H$ or 7040_{10}

Power Supplies

VDD	GND
3.3V	0V

Design Description

This cookbook design describes a temperature measurement circuit with two thermocouples using the ADS1118. Thermocouple voltage measurements are made with the ADS1118 internal voltage reference, while cold-junction compensation (CJC) measurements are made with the onboard temperature sensor. Two channels of the ADC are used for two K-type thermocouples with a temperature measurement range from –270°C to 1370°C. Included in this design are ADC register settings to configure the device and pseudo code is provided to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab and field instrumentation,* and *factory automation and control.* For more information about using precision ADCs with thermocouples, see *A Basic Guide to Thermocouple Measurements.*



Design Notes

1. Use supply decoupling capacitors for the supply. VDD must be decoupled with at least a 0.1-µF capacitor to GND. See *ADS1118 Ultrasmall, Low-Power, SPI™-Compatible, 16-Bit Analog-to-Digital Converter with Internal Reference and Temperature Sensor* for details on power supply recommendations.
2. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Because of size, this may not always be practical and X7R capacitors are the next best alternative.
3. Cold-junction compensation is required for accurate measurement of the thermocouple temperature.
4. The K-type thermocouple is chosen as it has a large input range and thermocouple voltage. Other thermocouples have different sensitivities and error tolerances. For measurements with other thermocouples and a guide to use them, see *A Basic Guide to Thermocouple Measurements.*
5. Conversion tables and polynomial equations used to determine thermocouple temperature from the thermoelectric voltage is found at the NIST website. Additionally, use the Analog Engineer's Calculator to determine some thermocouple conversions.

Component Selection

1. Identify the range of operation for the thermocouple.

   The K-type thermocouple has a range of approximately −6.5mV to +55mV if the temperature measurement range is from −270°C to 1370°C. This range is used to maximize the resolution of the measurement, considering the full-scale range of the ADC.
2. Determine gain and input range of the ADC.

   In the ADS1118, the programmable gain amplifier (PGA) is implemented through scaled capacitive sampling, not as a true amplifier. With this PGA, the input range extends to the full supply range, but has less amplification and lower input impedance. In this device, the maximum amplification gives a full scale range of ±0.256V. This is much larger than the range of −6.5mV to +55mV for the thermocouple. While it is not possible to over-range the PGA, the measurement uses a limited portion of the full scale range. Comparing the thermocouple range to the full-range, the percent of the usable ADC range can be calculated:

   % of usable ADC range = [55mV–(–6.5mV)]/[0.256mV–(–0.256mV)] • 100% = 12.0%

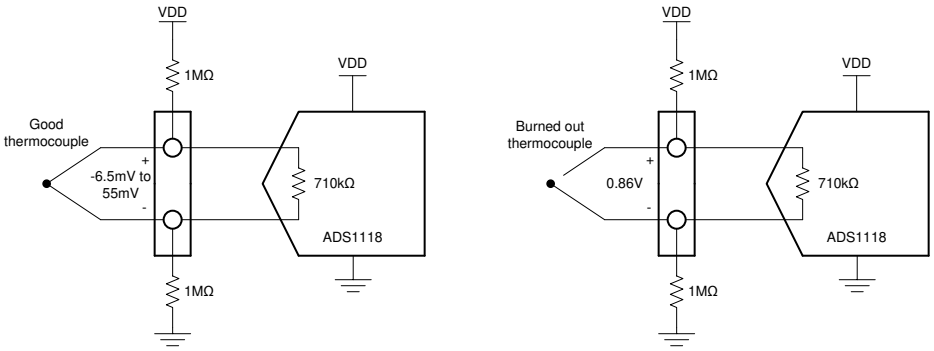
   Number of ADC codes in measurement range = $0.12 \times 2^{16} = 7864$

   With a range of −270°C to 1370°C for the thermocouple, 7864 codes are used to represent a temperature range of 1640°C. This equates to approximately 0.21°C per ADC code which is enough for most thermocouple applications.

   In other precision ADCs, the PGA is implemented similar to an instrumentation amplifier. If using a different ADC, calculate the maximum gain allowed without over-ranging the PGA based on the maximum thermocouple output voltage. Then, verify that the thermocouple biasing is near mid-supply so that the input signal is in the common-mode input range of the PGA.
3. Set up the resistor biasing to establish the input DC level and burnout detection.

   Equal biasing resistors are tied from either end of the thermocouple and to GND and VDD. In normal operation, the resistors set the DC biasing point of the thermocouple to near mid-supply. If the thermocouple burns out and becomes an open circuit, the resistors pull apart the thermocouple leads to either supply. These resistors are set high (often 500kΩ to 10MΩ) to reduce the bias current going through the thermocouple. Resistor bias current reacting with the thermocouple lead resistance cause measurement error. However, the resistors must also be low enough to provide sufficient bias current to overcome any input current from the resistor.

   In this design, biasing resistors are chosen to be 1MΩ. This value sets the resistor biasing current to a low 1.65µA. However, in the case of a burned out thermocouple, 1MΩ provides enough current to separate the ADC inputs against the 710kΩ equivalent input impedance of the ADS1118.



In the case of the good thermocouple, the thermocouple voltage has a range of –6.5mV to 55mV. The remaining 3.3V of the VDD supply is dropped equally between the biasing resistors. With 1-MΩ bias resistors, the thermocouple voltage has a DC operating point near mid-supply at 1.65V.

In the case of a burned out thermocouple, the open circuit creates a voltage divider with the two 1MΩ around the 710-kΩ equivalent input impedance. The ADC input voltage with a burned out thermocouple may be calculated as:

ADC input voltage = 3.3V × [710kΩ ÷ (1MΩ + 710kΩ + 1MΩ)] = 0.85V

If the thermocouple burns out, the ADC input voltage is 0.86V, which is much larger that the positive full-scale reading of the ADC. The ADC reports a reading of 7FFFh to indicate a burnout condition.

4. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   If there is input filtering, the input current reacts with any series filter resistance to create an error. For the ADS1118, the input current is modeled as an equivalent differential input impedance. As previously mentioned, the equivalent differential input impedance is typically 710kΩ. For this reason, the input series resistance is kept low or the added voltage appears as a gain error.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors are reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 8SPS. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations:

   $f_{IN\_DIFF} = 1 \div [2 \times \pi \times C_{DIFF} \times (2 \times R_{DIFF})]$

   $f_{IN\_CM} = 1 \div (2 \times \pi \times C_{CM} \times R_{DIFF})$

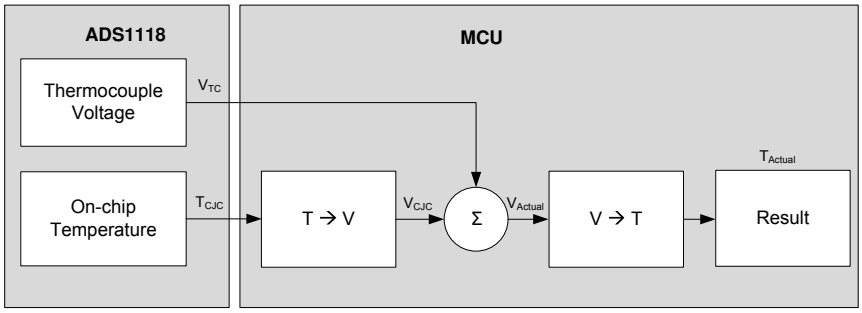
   For the ADC input filtering, R_{IN} = 500Ω, C_{IN_DIFF} = 1µF, and C_{IN_CM} = 0.1µF. This sets the differential filter bandwidth to 160Hz and the common-mode filter bandwidth to 3.2kHz.

5. Use cold-junction compensation to calculate the actual thermocouple voltage based on the cold-junction temperature.

   To get a precise measurement from a thermocouple, cold-junction compensation must be performed to get an accurate temperature measurement. An accurate measurement of the cold-junction where the thermocouple leads are tied is required. You cannot simply add the temperature of the cold-junction to the temperature computed from the thermocouple voltage. To accurately determine the thermocouple temperature, the proper method is to:

a. Convert the cold-junction temperature (T_{CJ}) to a voltage (V_{CJ})
b. Add the cold-junction voltage to the measured thermocouple voltage ($V_{CJ} + V_{TC}$)
c. Convert the summed cold-junction voltage and thermocouple voltage to the thermocouple temperature (T_{TC})

The following flow diagram shows the conversion method to determine the actual temperature of the thermocouple based on the ADC measurements.



Conversion tables and polynomial equations used to determine thermocouple temperature from the thermoelectric voltage are found at the NIST website.

Because the ADS1118 has an accurate internal temperature sensor, use a measurement. The internal temperature sensor has a typical accuracy of 0.2°C for a range of 0°C to 70°C. This accuracy is preferred for the cold-junction measurement. However, the device requires a good thermal contact to the connection for the thermocouple cold-junction. Any error in the cold-junction measurement yields an error in the resulting temperature measurement.

For more information about thermocouples and the cold-junction compensation measurement, see *A Basic Guide to Thermocouple Measurements*.

Measurement Conversion

Conversions for the thermocouple voltage are relatively straight forward based on the full-scale range setting of the ADC. In this design, the smallest full-scale range is used (±0.256V).

Measurement 1 (Thermocouple 1):

$$\text{Output Code 1} = [2^{15} \times (V_{AIN0} - V_{AIN1}) \div (0.256V)]$$

$$\text{Thermocouple 1 Voltage} = V_{AIN0} - V_{AIN1} = [(\text{Output Code 1}) \times 0.256V \div 2^{15}]$$

Measurement 2 (Thermocouple 2):

$$\text{Output Code 2} = [2^{15} \times (V_{AIN2} - V_{AIN3}) \div (0.256V)]$$

$$\text{Thermocouple 2 Voltage} = V_{AIN2} - V_{AIN3} = [(\text{Output Code 2}) \times 0.256V \div 2^{15}]$$

Conversions for the internal temperature sensor require some data manipulation. Temperature data from the ADC are represented as a 14-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C and negative numbers are represented in binary twos complement format.

Measurement 3 (Internal Temperature Sensor):

$$\text{Output Code 3} = [(\text{Temperature}) \div (0.03125°C)]$$

$$\text{Temperature} = [(\text{Output Code 3}) \times (0.03125°C)]$$

Output Code 3 is the first 14 bits of the two byte output data from the ADC. For more information about the ADS1118 and the internal temperature sensor see *ADS1118 Ultrasmall, Low-Power, SPI™-Compatible, 16-Bit Analog-to-Digital Converter with Internal Reference and Temperature Sensor*.

Register Settings

Measurement 1 (Thermocouple 1 Voltage): Configure Register (8D0Bh)

Bit	Field	Setting	Description
15	SS	1	Start a single conversion
14:12	MUX[2:0]	000	AINP is AIN0 and AINN is AIN1 for thermocouple 1
11:9	PGA[2:0]	110	FSR is ±0.256V
8	MODE	1	Power-down and single-shot mode
7:5	DR[2:0]	000	8SPS
4	TS_MODE	0	ADC mode
3	PULL_UP_EN	1	Pullup resistor enabled on DOUT/ $\overline{\text{DRDY}}$ pin
2:1	NOP[1:0]	01	Valid data, update the Config register
0	Reserved	1	Always write 1h

Measurement 2 (Thermocouple 2 Voltage): Configure Register (BD0Bh)

Bit	Field	Setting	Description
15	SS	1	Start a single conversion
14:12	MUX[2:0]	011	AINP is AIN2 and AINN is AIN3 for thermocouple 2
11:9	PGA[2:0]	110	FSR is ±0.256V
8	MODE	1	Power-down and single-shot mode
7:5	DR[2:0]	000	8SPS
4	TS_MODE	0	ADC mode
3	PULL_UP_EN	1	Pullup resistor enabled on DOUT/ $\overline{\text{DRDY}}$ pin
2:1	NOP[1:0]	01	Valid data, update the Config register
0	Reserved	1	Always write 1h

Measurement 3 (Internal Temperature Sensor): Configure Register (8D1Bh)

Bit	Field	Setting	Description
15	SS	1	Start a single conversion
14:12	MUX[2:0]	011	AINP is AIN2 and AINN is AIN3 (ignored by TS_MODE)
11:9	PGA[2:0]	110	FSR is ±0.256V (ignored by TS_MODE)
8	MODE	1	Power-down and single-shot mode
7:5	DR[2:0]	000	8SPS
4	TS_MODE	1	Temperature sensor mode (bypasses MUX[2:0])
3	PULL_UP_EN	1	Pullup resistor enabled on DOUT/ $\overline{\text{DRDY}}$ pin
2:1	NOP[1:0]	01	Valid data, update the Config register
0	Reserved	1	Always write 1h

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS1118 in single-shot conversion mode.

Data read back and device configuration are done with 32-bit transmission cycle with Configure register read back. The ADS1118 is configured to measure the thermocouple voltages with a full-scale range of ±256mV and a data rate of 8SPS. The device cycles from reading the voltage of thermocouple 1, the voltage of thermocouple

2, and then the ADS1118 internal temperature sensor. After taking all three readings, cold-junction compensation is used to convert the thermocouple voltages to the thermocouple temperatures.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Set CS low; // Start conversions
Send 8D0B8D0B;  //Start conversion for thermocouple 1
// Use 32-bit data transmission cycle with Config register readback
// The first iteration of the loop has no data readback
Set CS high;
Loop
{
Wait 69ms // Wait for typical data period +10% for internal oscillator variation
Set CS low;
Send BD0BBD0B; // Read data for thermocouple 1, start conversion for thermocouple 2,
Set CS high;
Wait 69ms;
Set CS low;
Send 8D1B8D1B; // Read data for thermocouple 2, start conversion for temperature sensor,
Set CS high;
Wait 69ms;
Set CS low;
Send 8D0B8D0B // Read data temperature sensor, Start conversion for thermocouple 1
Set CS high;
// Cold-junction compensation to determine thermocouple temperature
Convert thermocouple 1 ADC data to voltage;
Convert thermocouple 2 ADC data to voltage;
Convert temperature sensor data to temperature;
Convert temperature sensor data to thermoelectric voltage; // By lookup table or calculation
Add thermocouple 1 voltage to temperature thermoelectric voltage;
Convert resulting voltage for thermocouple 1 to temperature; // By lookup table or calculation
Add thermocouple 2 voltage to temperature thermoelectric voltage;
Convert resulting voltage for thermocouple 2 to temperature; // By lookup table or calculation
}
```

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS1118	Ultrasmall, low-power, SPI™-compatible, 16-bit analog-to-digital converter with internal reference and temperature sensor	16-bit, 860-SPS, 4-channel, delta-sigma ADC with PGA, oscillator, VREF, temp sensor and SPI	Precision ADCs (1)

(1) For cold-junction compensation, check that the device has a internal temperature sensor with specified limits. Alternately, an external temperature sensor may be used with an ADC channel for the cold-junction measurement.

Additional Resources

- Texas Instruments, ADS1118 Evaluation Module, product overview
- Texas Instruments, *ADS1118EVM User Guide and Software Tutorial*, user's guide
- Texas Instruments, *A Basic Guide to Thermocouple Measurements*, application note
- Texas Instruments, Analog Engineer's Calculator, tool overview
- Texas Instruments, Simple thermocouple measurement reference design, less than 1°C accuracy, product overview

Trademarks

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Analog Engineer's Circuit

±12V Voltage Sensing Circuit With an Isolated Amplifier and Pseudo-Differential Input SAR ADC

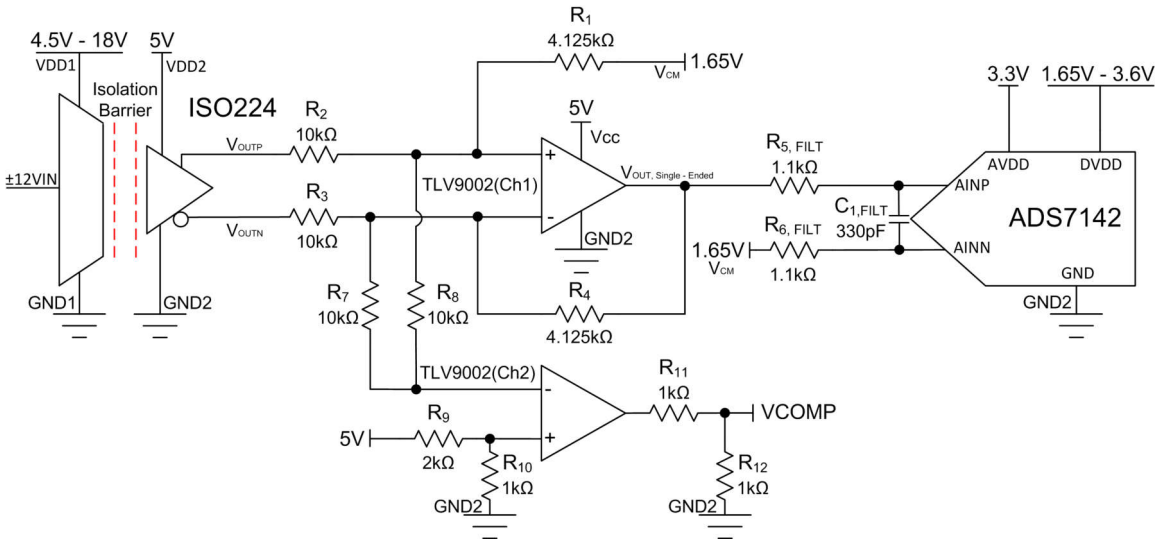
Data Converters *Alex Smith*

ISO224 Input Voltage	ISO224 Output (V_{OUTP} – V_{OUTN})	ADS7142 Input (Pseudo-Differential)	ADS7142 Digital Output
12V	4V	3.3V	FFF_H
–12V	–4V	0V	000_H

Power Supplies and Reference Voltages			
VDD1	**VDD2 and Vcc**	**AVDD**	**GND**
4.5V - 18V	5V	3.3V	0V

Design Description

This circuit performs a ±12V isolated voltage sensing measurement using the ISO224 isolated amplifier, TLV9002 operational amplifier, and the ADS7142 SAR ADC. The ISO224 can measure single-ended signals of ±12V with a fixed gain of ⅓V/V and produces a ±4V isolated differential output voltage with an output common-mode voltage of VDD2 / 2. Channel 1 of the TLV9002 conditions the output of the ISO224 to fit the input range of the ADS7142, while channel 2 monitors the ISO224 fail-safe output. The ADS7142 is a dual-channel ADC with a full-scale input and reference voltage of AVDD which can range from 1.65V to 3.6V. For this cookbook circuit, the ADS7142 dual-channel input is used in a pseudo-differential configuration which allows for both positive and negative signals to be measured by the ISO224. This circuit is applicable to many high voltage industrial applications, such as *Train Control and Management Systems*, *Analog Input Modules*, and *Inverter and Motor Control*. The equations and explanation of component selection in this design can be customized based on system specifications and requirements.



Specifications

Specification	Calculated	Simulated
Transient ADC input settling at 140kSPS	403µV	88µV
Conditioned signal range	0V–3.3V	0V–3.3V
Noise (at the input)	262µV_{RMS}	526µV_{RMS}
Closed-loop bandwidth	175kHz	145kHz

Design Notes

1. The ISO224 was selected due to the wide input range, flexible power configuration, and high accuracy.
2. The ADS7142 was selected due to very low power, high level of integration, flexible power configurations, and small size.
3. The TLV9002 operational amplifier was selected for the cost optimization, configuration options, and small size.
4. Select low impedance, low noise sources for AVDD, V_{CM}, and the pseudo-differential input to AINN which sets the common-mode voltage of the ADC.
5. Find the ADC full-scale range and common-mode specifications. This is discussed in component selection.
6. Select a COG capacitor for C_{FILT} to minimize distortion.
7. For best performance, consider using a 0.1% 20ppm/°C film resistor for $R_{FILT1,2}$ or better to minimize distortion.
8. *Understanding and Calibrating the Offset and Gain for ADC Systems* discusses methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors.
9. The *TI Precision Labs - ADCs* training video series discusses methods for selecting the charge bucket circuit R_{FILT} and C_{FILT}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. See *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select an isolated amplifier based on the input voltage range and determine the output common-mode voltage and output voltage range:

   The ISO224 power supplies can be 4.5V to 18V for the high-side power supply, and 4.5V to 5.5V for the low-side power supply. The ISO224 has a ±12V single-ended input range with a fixed gain of ⅓V/V, yielding a ±4V differential output at a common-mode voltage of VDD2 / 2, 2.5V for this example:

   $$\frac{\pm 12V_{\text{IN, Single}-\text{Ended}}}{3} = \pm 4V_{\text{OUT, Differential}} \text{ at } 2.5V\left(\frac{V_{DD2}}{2}\right) \text{common}-\text{mode}$$

2. Select an ADC with small size and low power:

   The ADS7142 is a small sized, low power, dual channel ADC that can be used in a pseudo-differential configuration. The maximum input range is set by the reference voltage and is equal to AVDD, 3.3V for this example:

   $$\text{ADC}_{\text{Full}-\text{Scale Range}} = V_{REF} = \text{AVDD} = 3.3V$$

   Find the required ADC common-mode voltage for pseudo-differential measurements:

   $$V_{CM} = \frac{V_{REF}}{2} = 1.65V$$

3. Select an operational amplifier that can convert the ±4V differential, 2.5V common-mode output of the ISO224 to the 3.3V pseudo-differential, 1.65V common-mode input of the ADS7142. Additionally, selecting an operational amplifier with a second channel that can monitor the fail-safe output feature of the ISO224 is preferred.

The TLV9002 is a 2 channel, rail-to-rail input and output amplifier optimized for cost sensitive and small size applications.

Channel 1 is used to convert the ±4V differential, 2.5V common-mode output of the ISO224 to a 3.3V peak pseudo-differential output with a common-mode voltage of 1.65V. When R1 = R4 and R2 = R3, the transfer function is set by the following equation:

$$V_{OUT} = V_{OUTP}\left(\frac{R_4}{R_3}\right) + V_{OUTN}\left(\frac{R_1}{R_2}\right) + V_{CM}$$

The signal must be converted from ±4V to 3.3V, this means that the signal must be reduced by a factor of 3.3V / ±4V = 3.3V / 8V. Substituting V_{CM} with the previously calculated value of 1.65V and setting R2 and R3 to 10kΩ yields the following equations:

$$3.3V = 4V\left(\frac{R_4}{10k\Omega}\right) + 1.65V \qquad 0V = -4V\left(\frac{R_1}{10k\Omega}\right) + 1.65V$$

Solving for R1 and R4 yields values of 4.125kΩ.

Additional information on this topic can be seen in the *Interfacing a Differential-Output (Isolated) Amplifier to a Single-Ended Input ADC* application brief.

Channel 2 of the TLV9002 is used to monitor the fail-safe output feature of the ISO224. The ISO224 fail-safe output feature becomes active whenever the high-side power supply (VDD1) is missing independent of the input signal on the V_{IN} pin. The TLV9002 channel 2 output (VCOMP) is fed to a GPIO port on the system controller and goes high whenever the fail-safe output feature is active. For additional details, see the *Fail-Safe Output Feature* application note.

4. Select R_{1FILT}, R_{2FILT}, and C_{FILT} for settling of the input signal and sample rate of 140kSPS:

   Refine the R_{FILT} and C_{FILT} Values is a TI Precision Labs video showing the methodology for selecting R_{FILT} and C_{FILT}. The final value of 1.1kΩ and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

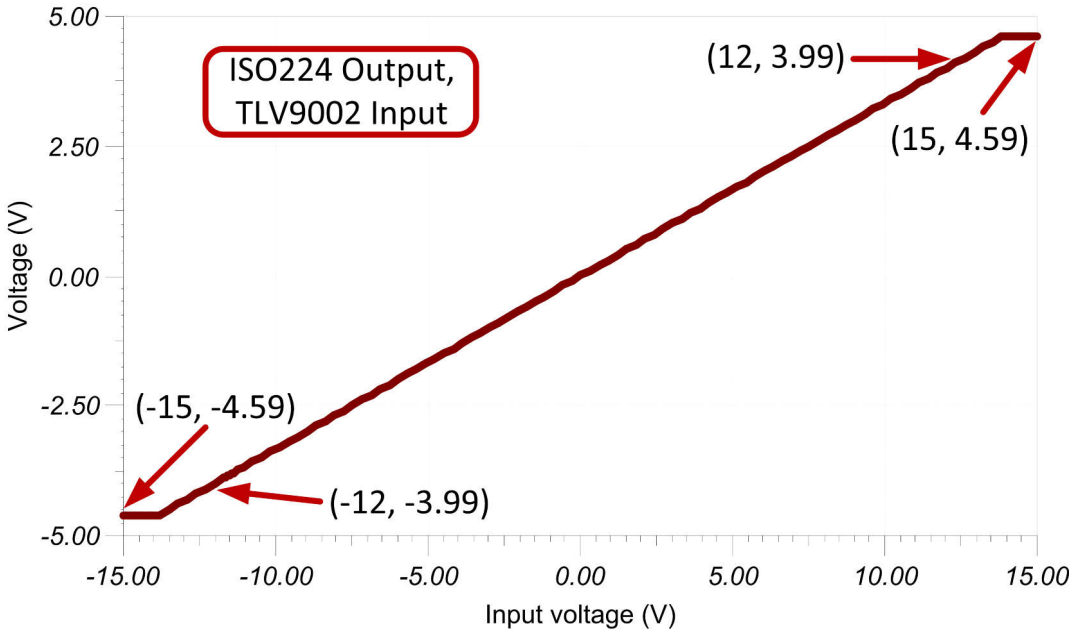
DC Transfer Characteristics

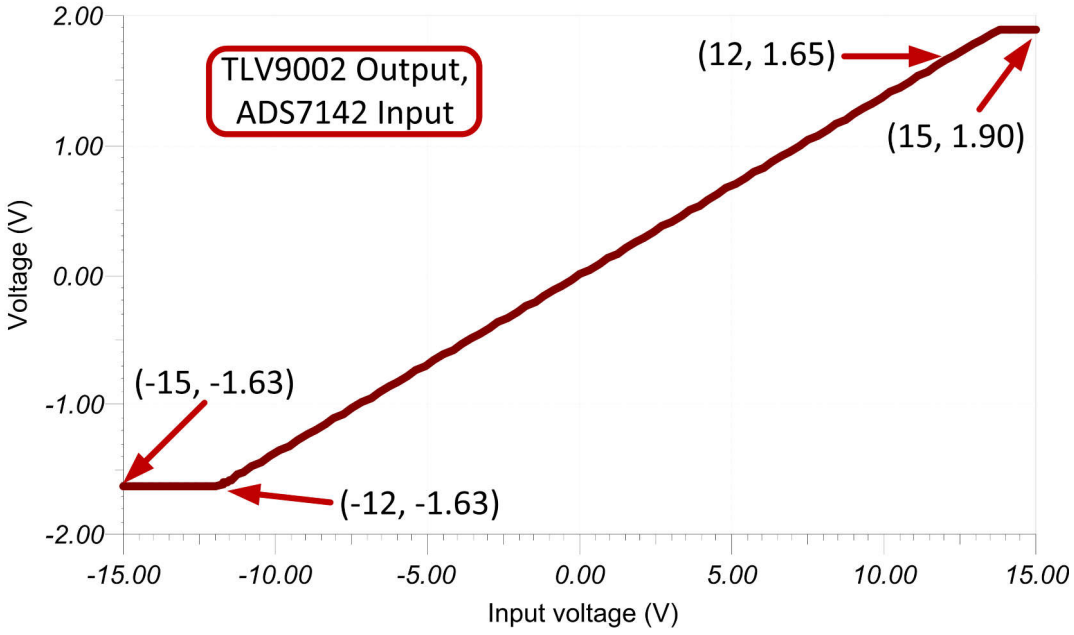
The following graphs show the simulated inputs of the TLV9002 and the ADS7142 from a ±15V input signal to the ISO224. The ISO224 has a linear output of ±VIN / 3 and the input to the TLV9002 can be seen in the first graph. The second graph shows that the TLV9002 further reduces the gain by VIN / 2.43 and shifts the common mode to 1.65V. This results in the full-range ±12V input signal using the 0V – 3.3V full-scale range (FSR) of the ADC with AVDD = VREF = 3.3V.

The following transfer function shows that the gain of the ISO224 and TLV9002 is 1/7.28V/V.

$$\text{Gain}_{\text{ISO224}} \times \text{Gain}_{\text{TLV9002}} \times V_{\text{IN}} = V_{\text{OUT}}$$

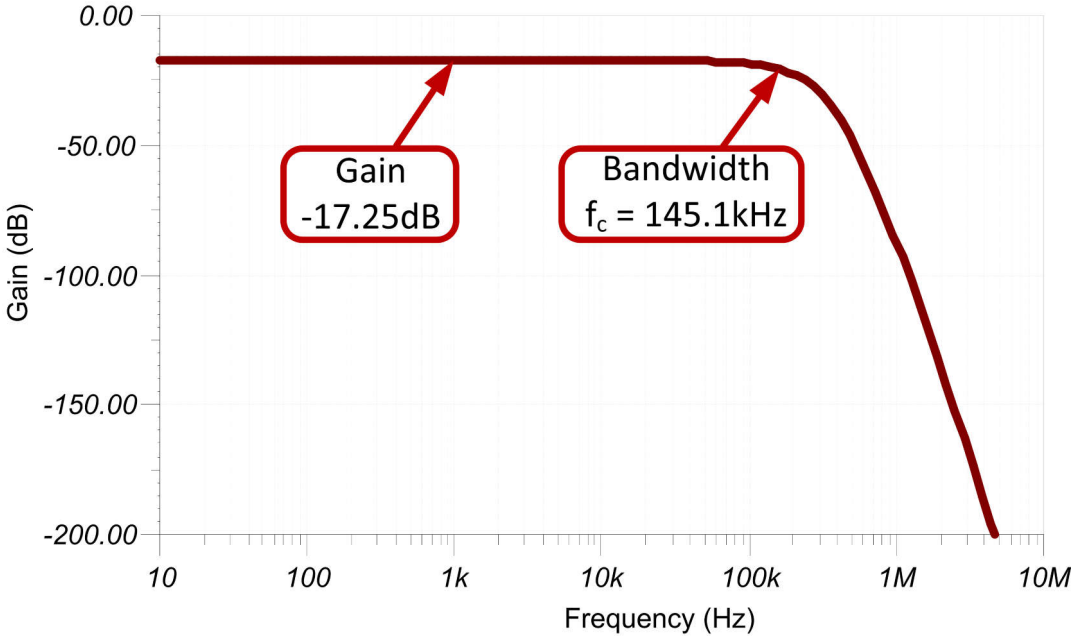
$$\frac{1}{3} \times \frac{1}{2.43} \times 12\text{V} = \frac{1}{7.28} \times 12\text{V} = 1.65\text{V}$$





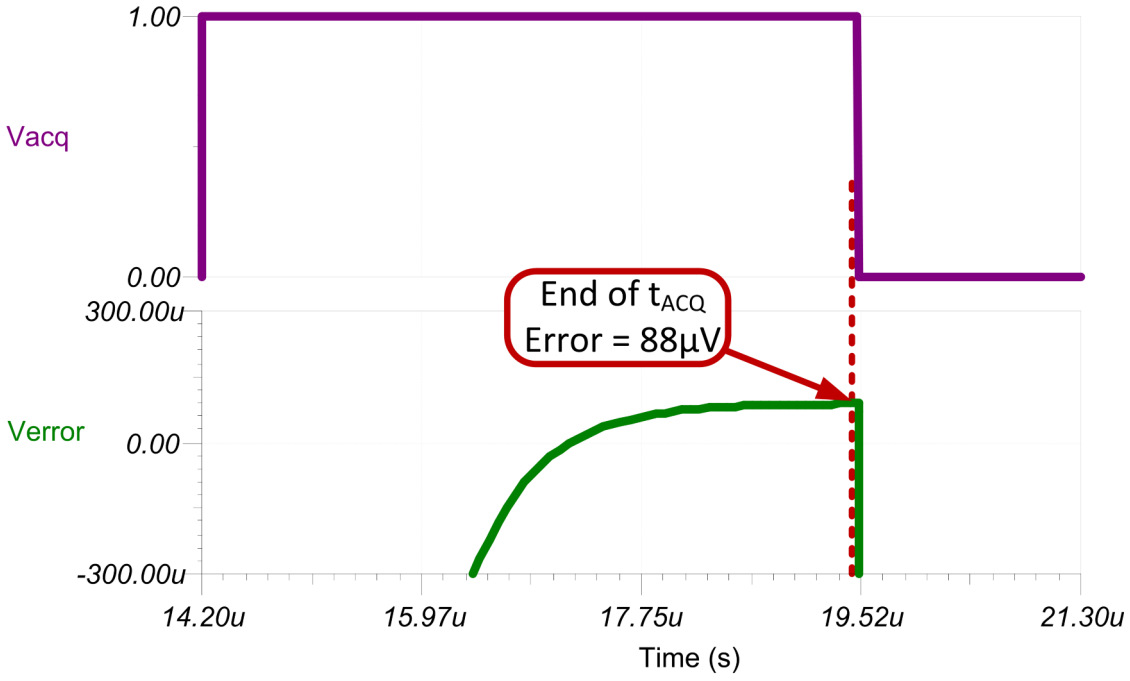
AC Transfer Characteristics

The simulated bandwidth of the signal chain is approximately 145kHz and the gain is –17.25dB, which is a linear gain of approximately 0.137V/V (attenuation ratio 1/7.28V/V). This matches the expected gain of the system.



Transient ADC Input Settling Simulation

The following simulation shows the transient settling results with an acquisition time of 5.3µs. The 88µV of noise is well within the 0.5 × LSB limit of 403µV. See *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.



Noise Simulation

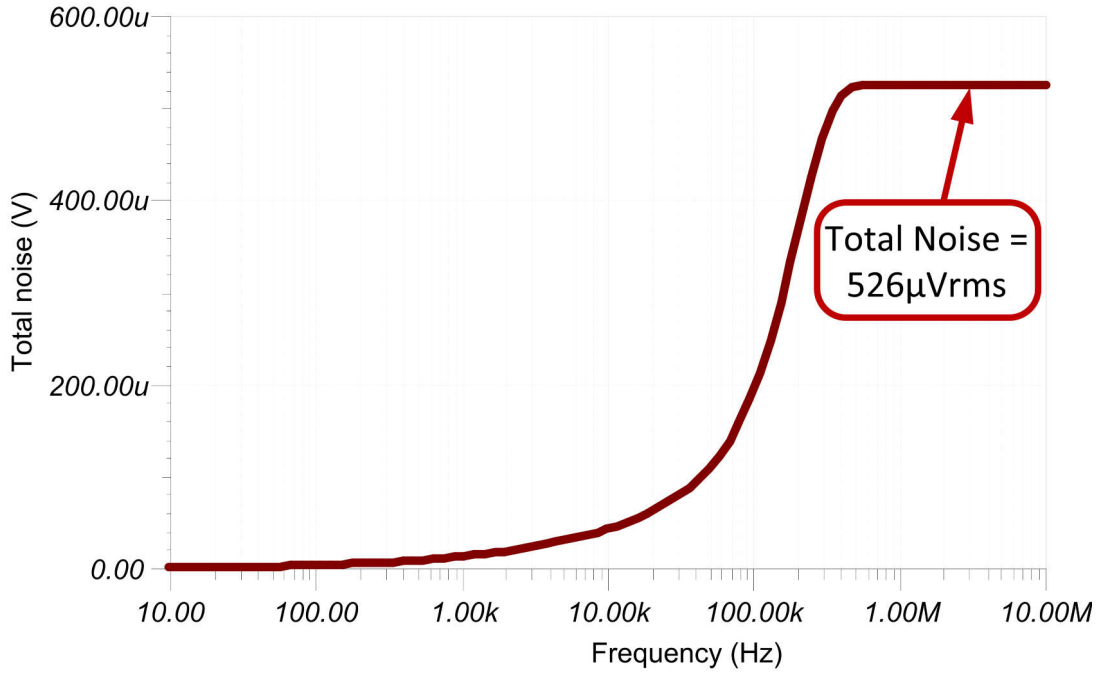
The simulated noise seen at the input of the ADC is greater than the expected calculated noise. This difference is due to noise peaking in the simulation model which is not included in the calculation. The following equations show that the ISO224 noise dominates the signal chain, and that the noise from the TLV9002 is negligible. See *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.

$$E_n = \text{Gain}(e_n) = \sqrt{(1.57 \times BW)}$$

$$E_{nISO224A} = \frac{1}{3} \times \frac{1}{2.43}\left(\frac{4\mu V}{\sqrt{Hz}}\right) \times \sqrt{1.57 \times 145kHz} = 262\mu V_{RMS}$$

$$E_{nTLV9002} = \frac{1}{2.43}\left(\frac{27nV}{\sqrt{Hz}}\right) \times \sqrt{1.57 \times 145kHz} = 5\mu V_{RMS}$$

$$E_{nISO224A + TLV9002} = E_{nISO224A} + E_{nTLV9002} = \sqrt{262^2\mu V_{RMS} + 5^2\mu V_{RMS}} = 262\mu V_{RMS}$$



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

TINA files for Isolated Design: SBAC226.

Design Featured Devices

Device	Key Features	Link	Similar Devices
ISO224	±12V single-ended input range, fixed gain of ⅓, yielding ±4V differential output, output common-mode voltage of 2.5V, 4.5V to 18V high-side power supply, 4.5V to 5.5V low side power supply, input offset: ±5mV at 25°C, ±42µV/°C maximum, gain error: ±0.3% at 25°C, ±50ppm/°C maximum, nonlinearity: ±0.01% maximum, ±1ppm/°C, high-input impedance of 1.25MΩ.	ISO224	www.ti.com/isoamps
ADS7142	Dual-channel, full-scale input span and reference set by AVDD, 12-bit performance by default, 16-bit performance with high precision mode, very low current consumption of 0.45µA at 600SPS.	ADS7142	https://www.ti.com/PrecisionADCs
TLV9002	Dual-channel, rail-to-rail input and output amplifier, low broadband noise of 2727nV/√ Hz, low input offset voltage of ±0.04mV.	TLV9002	https://www.ti.com/opamps

Trademarks

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Analog Engineer's Circuit

±12-V voltage sensing circuit with an isolated amplifier and differential input SAR ADC

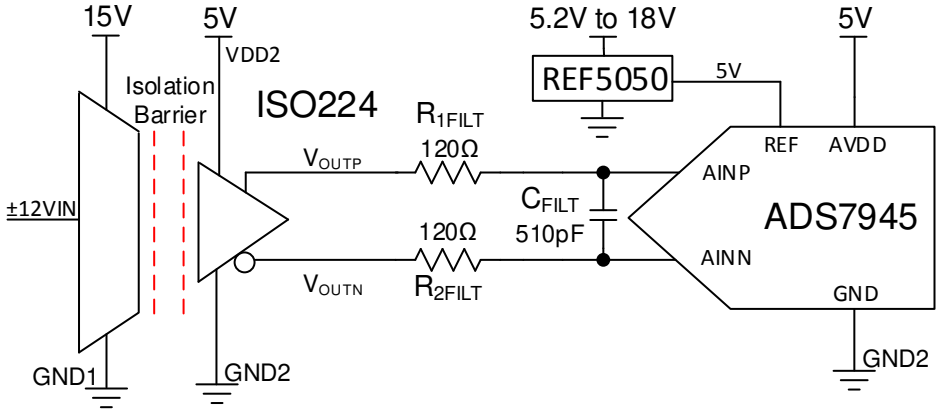
Alex Smith

ISO224 Input Voltage	ISO Output, ADC Input (V_{OUTP} - V_{OUTN})	Digital Output ADS7945
+12V	+4V	1999_H
–12V	–4V	$E666_H$

Power Supplies and Reference Voltages		
VDD1	**VDD2 and AVDD**	**REF5050 External Ref**
15V	5V	5V

Design Description

This circuit performs a ±12-V isolated voltage sensing measurement utilizing the ISO224 isolated amplifier and the ADS745 SAR ADC. The ISO224 can measure true differential signals of ±12V with a fixed gain of ⅓V/V and produces an isolated differential output voltage with an output common-mode voltage of VDD2 / 2. The ADS7945 is a fully differential input ADC with a full-scale input voltage of ±V_{REF} and a common-mode input voltage of V_{REF} / 2 ±200mV. Selecting a +5-V reference allows the ADS7945 to accept the full-scale and common-mode outputs from the ISO224. Capturing the ISO224 output with a fully differential input ADC doubles the system dynamic range compared to a single-ended conversion. Many high-voltage industrial applications such as *Protection Relays*, *Channel-to-Channel Isolated ±10V Analog Input Cards*, and *Inverter & Motor Control*. The equations and explanation of component selection in this design can be customized based on system specifications and needs.



Specifications

Specification	Calculated	Simulated
Transient ADC input settling at 100ksps	305µV	11µV
Conditioned signal range	±4V	±4V
Noise (at the input)	1.9mV_{RMS}	1.73mV_{RMS}
Closed-loop bandwidth	175kHz	185kHz

Design Notes

1. The ADS7945 was selected due to its low power and a compatible analog input structure with the ISO224.
2. Verify the systems linear operation for the desired input signal range. This is verified using simulation in the DC Transfer Characteristics selection.
3. Select COG capacitors for C_{FILT} to minimize distortion.
4. *Understanding and Calibrating the Offset and Gain for ADC Systems* covers methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors.
5. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{FILT} and C_{FILT}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select an isolated amplifier based on the input voltage range and determine the output common-mode voltage and output voltage range:

   ISO224:
   - ±12-V single-ended input range
   - Fixed gain of ⅓, yielding ±4-V differential output
   - Output common-mode voltage of +2.5V
   - 4.5-V to 18-V high-side power supply, 4.5-V to 5.5-V low-side power supply
   - Input Offset: ±5mV at 25°C, ±42µV/°C maximum
   - Gain Error: ±0.3% at 25°C, ±50ppm/°C maximum
   - Nonlinearity: ±0.01% max, ±1ppm/°C
   - High-input impedance of 1.25MΩ
2. Select an ADC with an appropriate common-mode and differential input range to pair with the +2.5-V common-mode and ±4-V differential output of the ISO224:

   ADS7945:
   - ±5-V maximum analog input range
   - Full-scale input span set by ±voltage reference
   - Input common-mode range of V_{REF} / 2 ±0.2V
   - 2.7-V to 5.25-V power supply
   - High SNR of 84, low power of 11.6mW at 2Msps
3. Select a voltage reference that supports the common-mode constraint set by the 2.5-V common-mode output of the ISO224 and the V_{REF} / 2 ±0.2-V common-mode input voltage of the ADS7945. This means that the reference output voltage must be 5V, low noise, and a configurable input voltage is preferred:

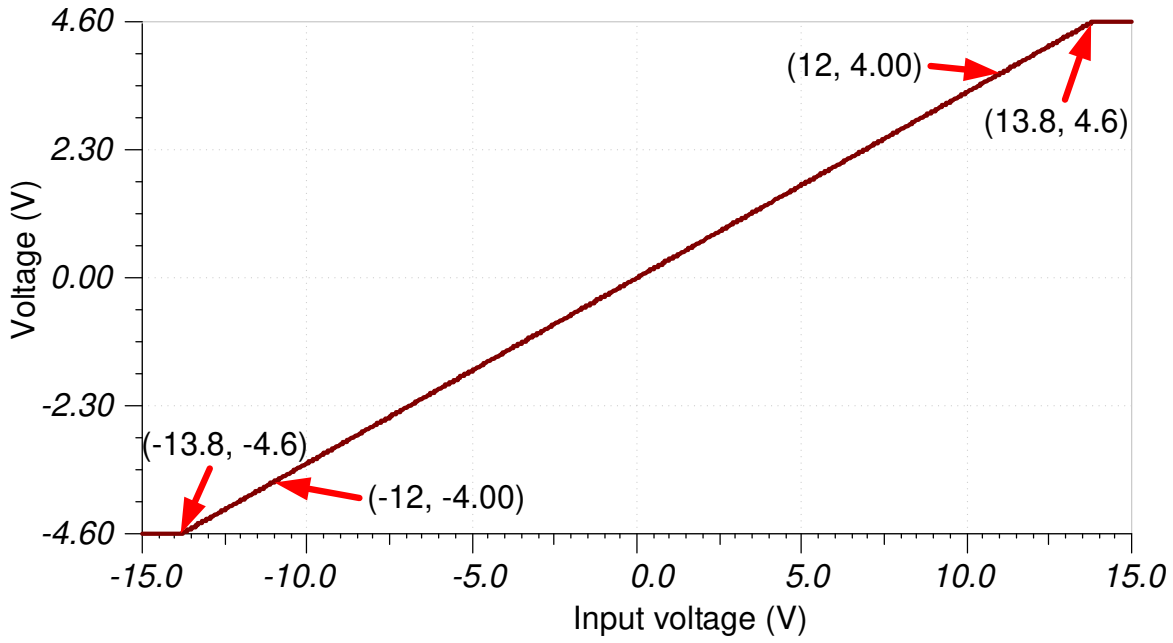
   REF5050:
   - 5-V output
   - 5.2-V to 18-V input voltage power supply
   - 3µVPP/V noise
4. Select R_{1FILT}, R_{2FILT}, and C_{FILT} for settling of the input signal and sample rate of 100ksps:

   Refine the R_{FILT} and C_{FILT} Values is a TI Precision Labs video showing the methodology for selecting R_{FILT} and C_{FILT}. The final value of 120Ω and 510pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

DC Transfer Characteristics

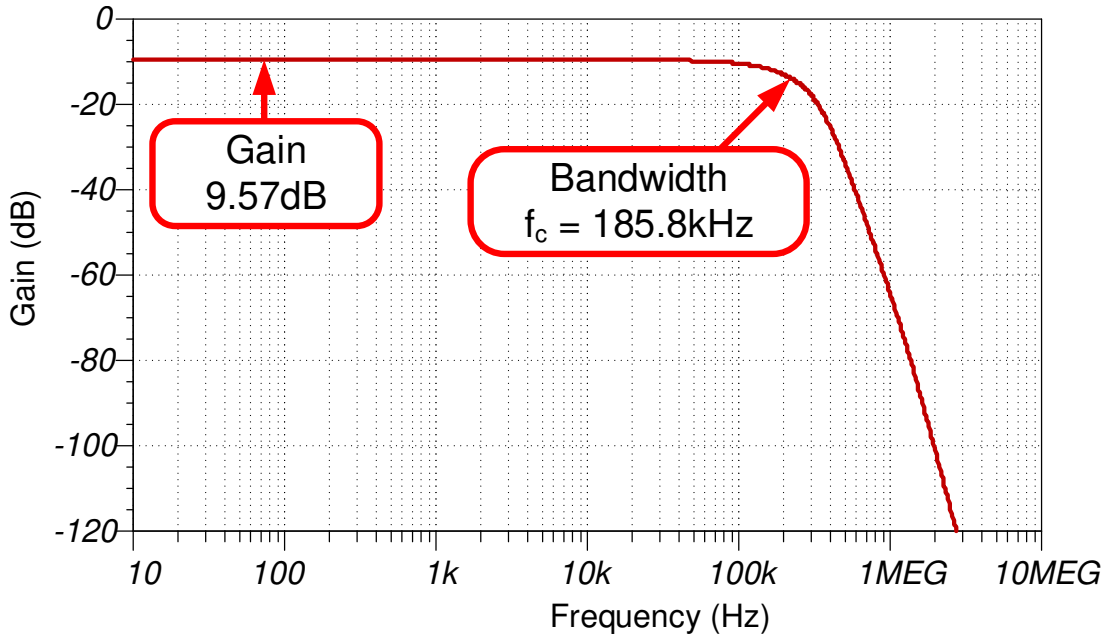
The following graph shows the simulated output for a ±15-V input. The desired linear range is a ±4-V output for a ±12-V input. This simulation shows that the linear output range is approximately ±4.6V which is well beyond the requirement.

The transfer function shows the ISO224 gain is ⅓ (that is, Gain · V_{IN} = V_{OUT}, (⅓)·(12V) = 4V).



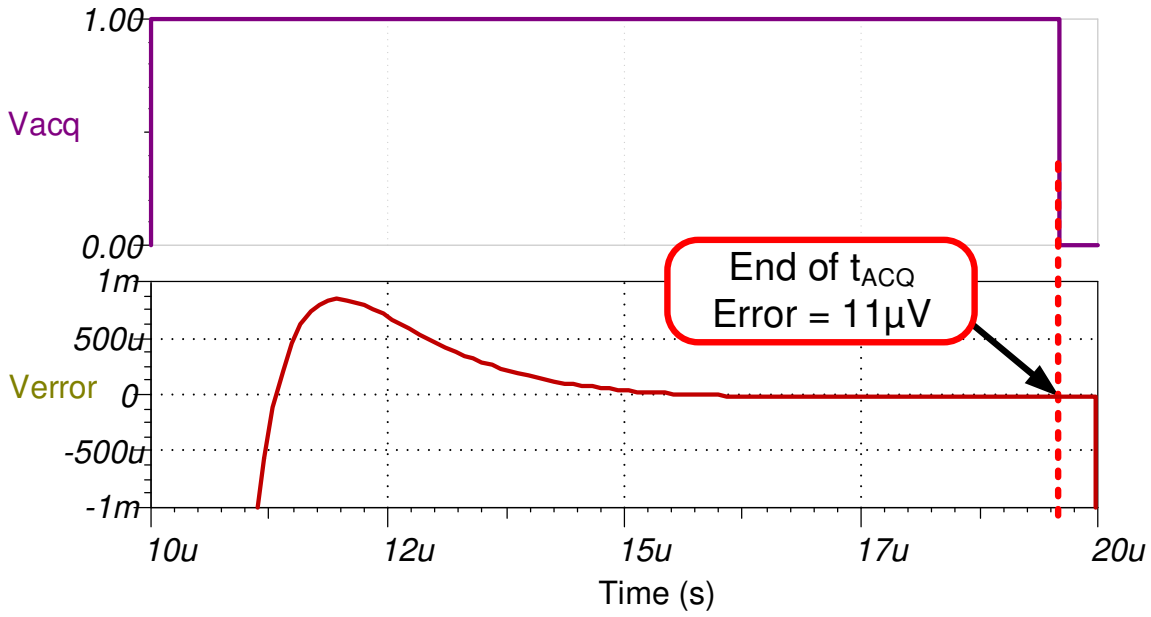
AC Transfer Characteristics

The simulated bandwidth is approximately 186kHz and the gain is –9.57dB (or 0.332V/V) which closely matches the expected gain and bandwidth for the ISO224 (specified fc = 175kHz, gain = 0.333V/V).



Transient ADC Input Settling Simulation

The following simulation shows the transient settling results with an acquisition time of 9.6µs. The 11-µV settling error is well within the 0.5 × LSB limit of 305µV. See *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.



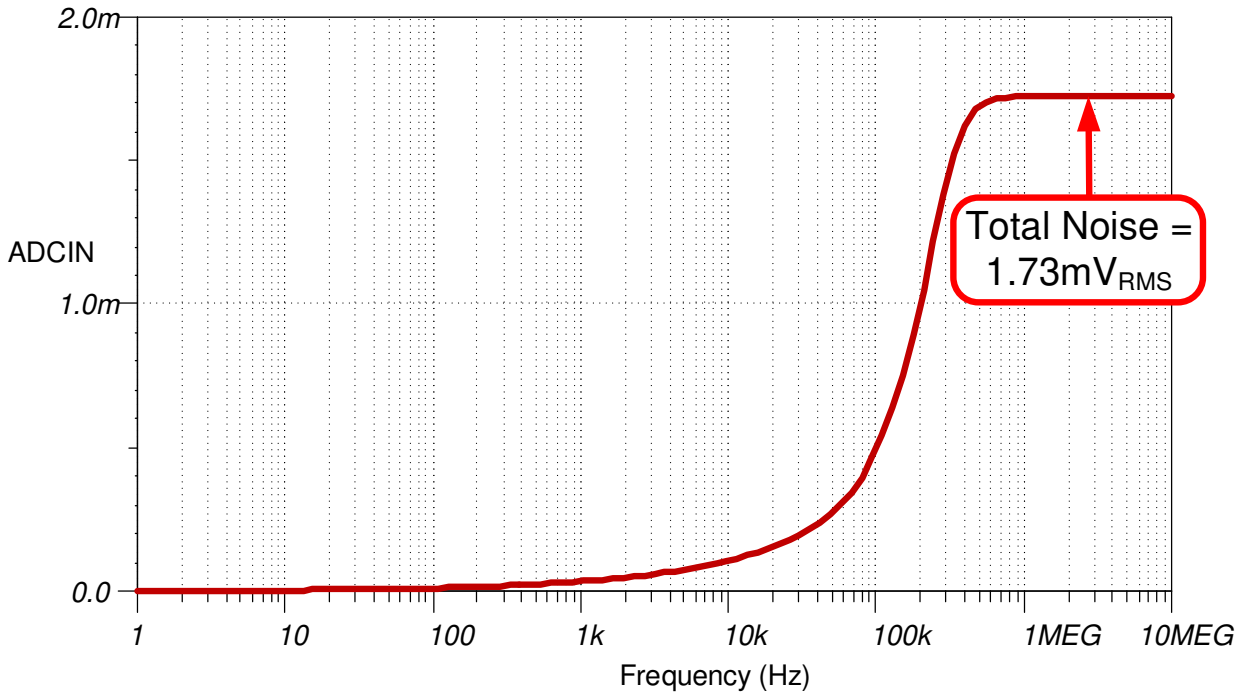
Noise Simulation

The following noise calculation looks only at the noise of the ISO224. The ISO224 noise is substantially higher than other noise sources in the circuit, so the total noise can be approximated as the ISO224 noise. The same method can be used for the B grade.

$$E_{nISO224A} = Gain(e_n)\sqrt{1.57 \cdot BW}$$

$$E_{nISO224A} = \frac{1}{3}\left(4\mu V / \sqrt{Hz}\right)\sqrt{1.57 \cdot 176kHz} = 0.7mV_{RMS}$$

The simulated noise is greater than the expected calculated noise. This difference is due to noise peaking in the simulation model. The noise peaking is not included in the calculation. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ISO224	±12-V single-ended input range, Fixed gain of ⅓, yielding ±4-V differential output, output common-mode voltage of +2.5V, 4.5-V to 18-V high-side power supply, 4.5-V to 5.5-V low side power supply, input offset: ±5mV at 25°C, ±42µV/°C max, gain error: ±0.3% at 25°C, ±50ppm/°C maximum, nonlinearity: ±0.01% maximum, ±1ppm/°C, high-input impedance of 1.25MΩ	www.ti.com/product/ISO224	www.ti.com/isoamps
ADS7945	±5 V max analog input range, full-scale input span set by ±voltage reference, input common mode range of V_{REF} / 2 ±0.2V, 2.7-V to 5.25-V power supply, high SNR of 84, low power of 11.6mW at 2Msps	www.ti.com/product/ADS7945	http://www.ti.com/opamps
REF5050	3ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	www.ti.com/product/REF5050	http://www.ti.com/vref

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

See the TINA files for Isolated Design.

Trademarks

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Analog Engineer's Circuit

Antialiasing Filter Circuit Design for Single-Ended ADC Input Using Fixed Cutoff Frequency

Manuel Chavez

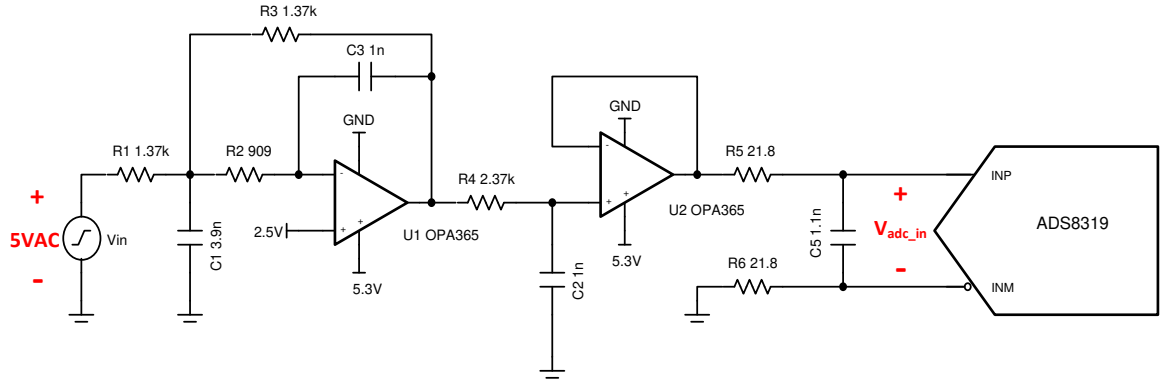
Input	ADC Input	Digital Output ADS8319
V_{in} Min = 0.1V	V_{adc_in} = 4.9V	$FAE1_H$ or 64225_{10}
V_{in}Max = V_{REF} = 4.9V	V_{adc_in} = 0.1V	$051F_H$ or 1311_{10}

Power Supplies

V_{cc}	V_{ee}	V_{cm}	V_{REF}	AVDD	DVDD
5.3V	GND (0V)	2.5V	5V	5V	5V

Design Description

This cookbook is intended to demonstrate a method of designing an antialiasing filter for a single-ended SAR ADC input using the Antialias Filter Designer on TI's *Analog Engineer's Calculator*. The objective of the tool is to find filter specifications that attenuates alias signals to one-half LSB of a given ADC. This design approach uses a fixed cutoff frequency and the example circuit uses the ADS8319 ADC. This single-ended device circuit is practical for low-power applications such as *data acquisition*, *lab instrumentation*, *oscilloscopes and digitizers*, *analog input modules*, and battery-powered equipment.



Specifications

Specification	Calculated / Goal	Simulated
Attenuate 1mV alias signal at Nyquist to ½ LSB $V_{in\_Nyquist}$ = 1mV at 250kHz	$V_{out\_Nyquist}$ <= ½ LSB ½ LSB = 38.14µV at 250kHz	$V_{out\_Nyquist}$ = 21µV Attenuation = –33.43dB
Transient ADC Input Settling	< 0.5 LSB or 38.15µV	91.5nV
Noise	78.9µV	87.77µV
Bandwidth	50kHz	50.1kHz

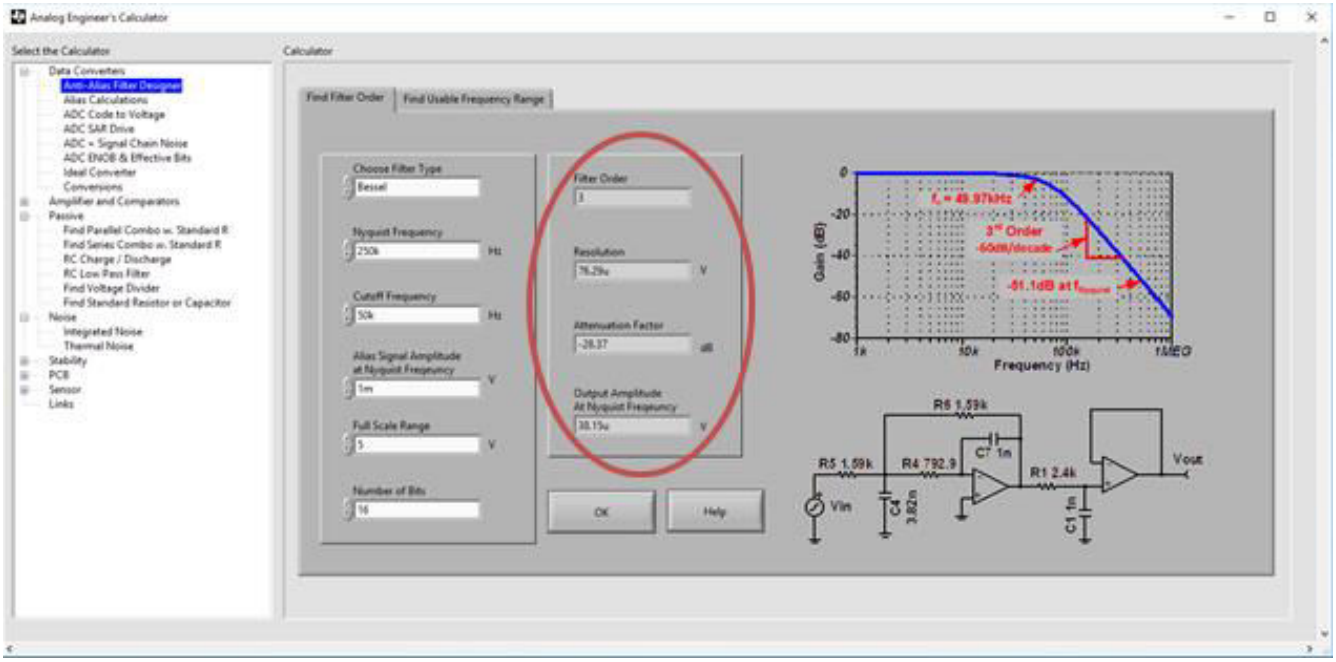
Design Notes

1. *TI Precision Labs* introduces the concept of frequency domain aliasing and describes how aliases are error sources to avoid or minimize. The video on *Aliasing and Anti-aliasing Filters* covers how an antialiasing filter can be used to minimize these aliasing errors.

2. The active filter in this cookbook is designed using TI's *Analog Engineer's Calculator* and *TI FilterPro*. This software can be used to design active filter circuits for many applications.
3. Use 0.1%–1% tolerance resistors and 5% tolerance capacitors or better for good system accuracy.
4. RC charge bucket circuits are specially designed for each system; TI's Precision Labs video on *Refining Rfilt and Cfilt Values* explains how to optimize the RC charge bucket.
5. Circuit simulations are modeled with schematics and diagrams made using *TINA-TI* simulation software.
6. For detail on choosing the right driver op amp, building and simulating the ADC model, and finding the RC charge bucket values, see the TI Precision Labs video series *Introduction to SAR ADC Front-End Component Selection*.

Component Selection

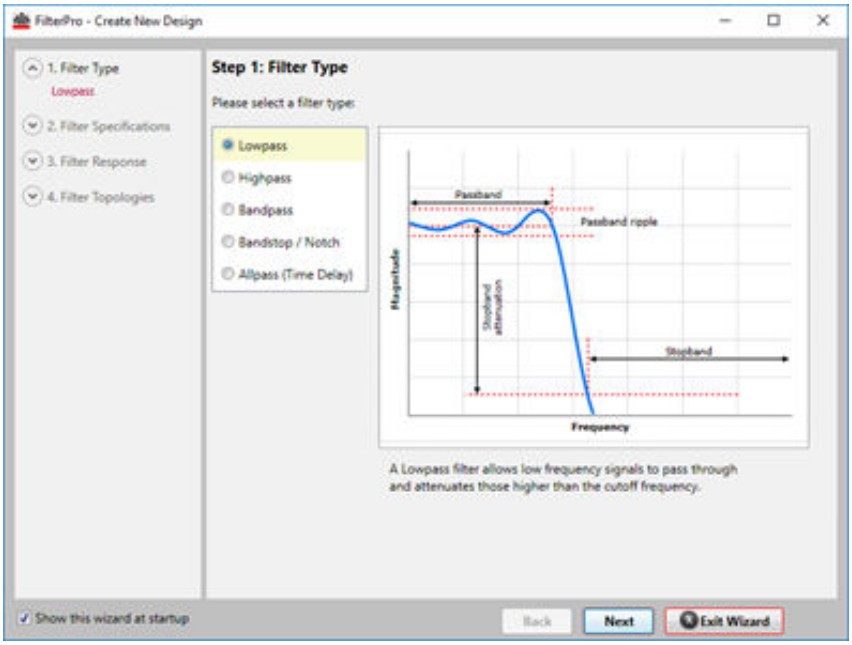
1. Once a single-ended ADC has been chosen, determine whether the antialias filter is designed with a set cutoff frequency or set filter order. If the frequency is set, continue through the following steps. If the filter order is set, use the "Find Usable Frequency Range" tab in the Analog Engineer's Calculator. Both methods use tools from the *Analog Engineer's Calculator*.
2. Using the *Find Filter Order* tab of the *Anti-Alias Filter Designer*, choose between a Bessel and Butterworth filter under *Choose Filter Type*. Bessel is chosen in this case for maximum flatness in the pass band and linear phase response.
3. Fill in the *Nyquist Frequency* to be ½ of the sampling rate of the ADC. The ADS8319 has a sampling rate of 500ksps so the Nyquist frequency is 250kHz.
4. Determine the desired cutoff frequency of the filter to be designed and enter it in the *Cutoff Frequency* box; a general guideline is for the cutoff frequency to be one decade above the desired input frequency. In this case, the input frequency is 5kHz so the cutoff frequency is set to 50kHz.
5. For the *Alias Signal Amplitude at Nyquist Frequency* field, enter the largest expected alias signal amplitude that attenuate to ½ LSB at the Nyquist frequency. This number ranges from microvolts up to full scale voltage. In this low-noise system, a maximum alias signal amplitude of 1mVpp is expected.
6. The *Full Scale Range* of the ADC is typically equal to Vref and is set to 5V in this system. The bit resolution of the ADS8319 is 16 bits and is filled into *Number of Bits*.
7. After clicking *OK*, the results displayed on the right side of the calculator are used to design the necessary antialias filter.



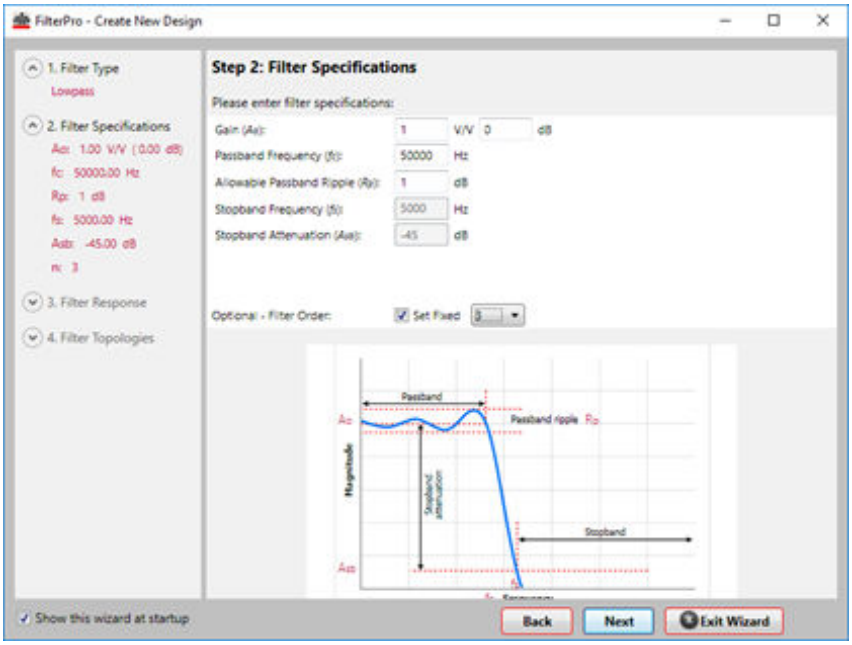
With the resulting filter specifications, the lowpass antialias filter can be designed by transcribing these numbers into TI FilterPro. The circuit specifications in this cookbook are $f_{nyquist}$ = 250k, f_c = 50k, V_{alias} = 1mV, FSR = 5V, and N bits = 16, so the Bessel example from Design Approach 1 is used continuing.

On startup, TI FilterPro asks for the filter specifications to design around. After the final screen, an active filter circuit is displayed, and this is the antialias filter of the system. Refer to the following screenshots for the steps using FilterPro.

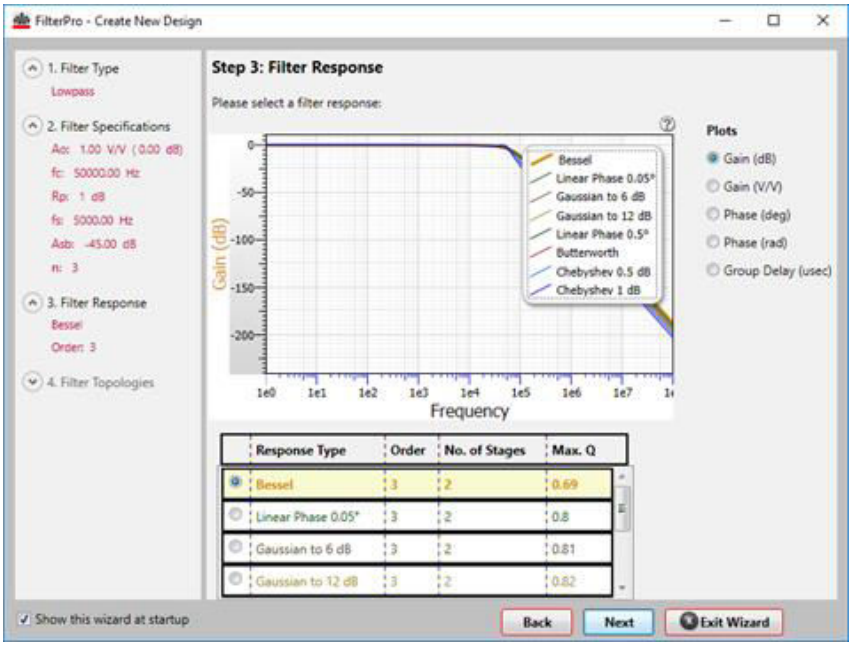
In step 1, *Lowpass* is selected since an antialias filter is a specific lowpass filter.



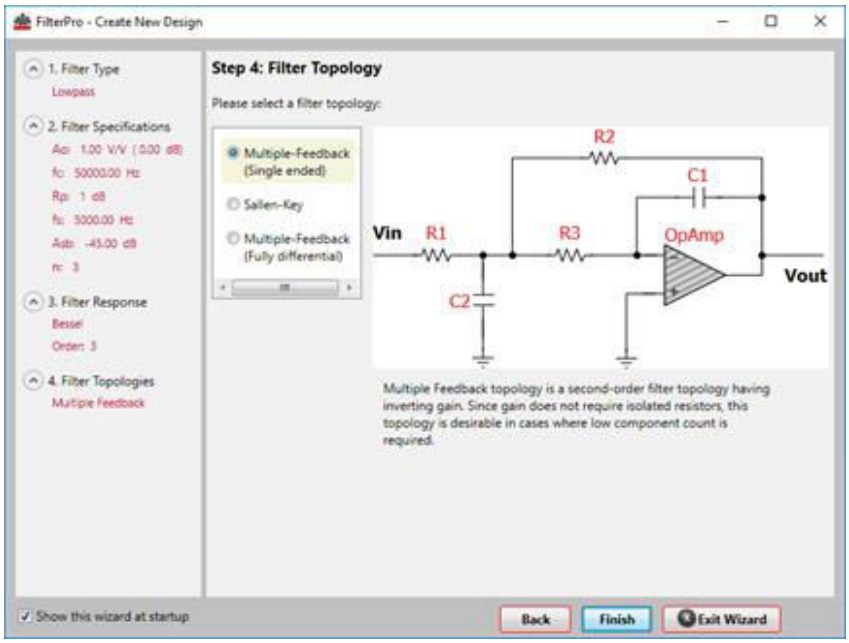
In step 2, the values for *Pass-band Frequency (f_c)* and filter order are filled in from the Analog Engineer's Calculator. The option to *Set Fixed* filter order must be selected to match calculated parameters.



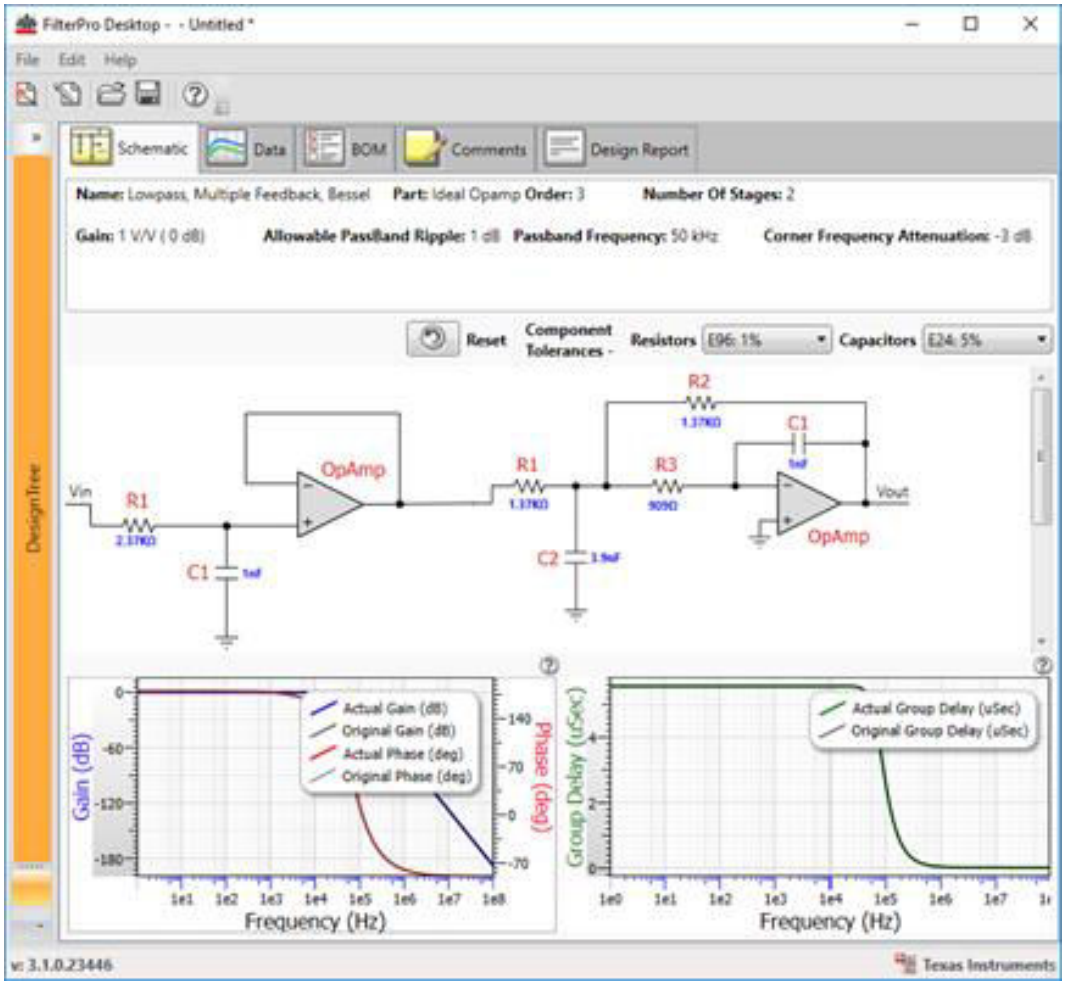
For step 3, select the filter type to match calculations; *Bessel* is chosen in this example for maximum flatness in the pass band and linear phase response.



Multiple feedback topology is chosen in step 4 because the filter attenuation is not limited by the bandwidth of the op amp. This topology has the disadvantages of inverting a signal and offering low input impedance. *Sallen-Key* can also be selected since it is a non-inverting topology with high-input impedance, but at higher frequencies the attenuation of the filter converges or even rises due to the bandwidth limitations of the op amp.



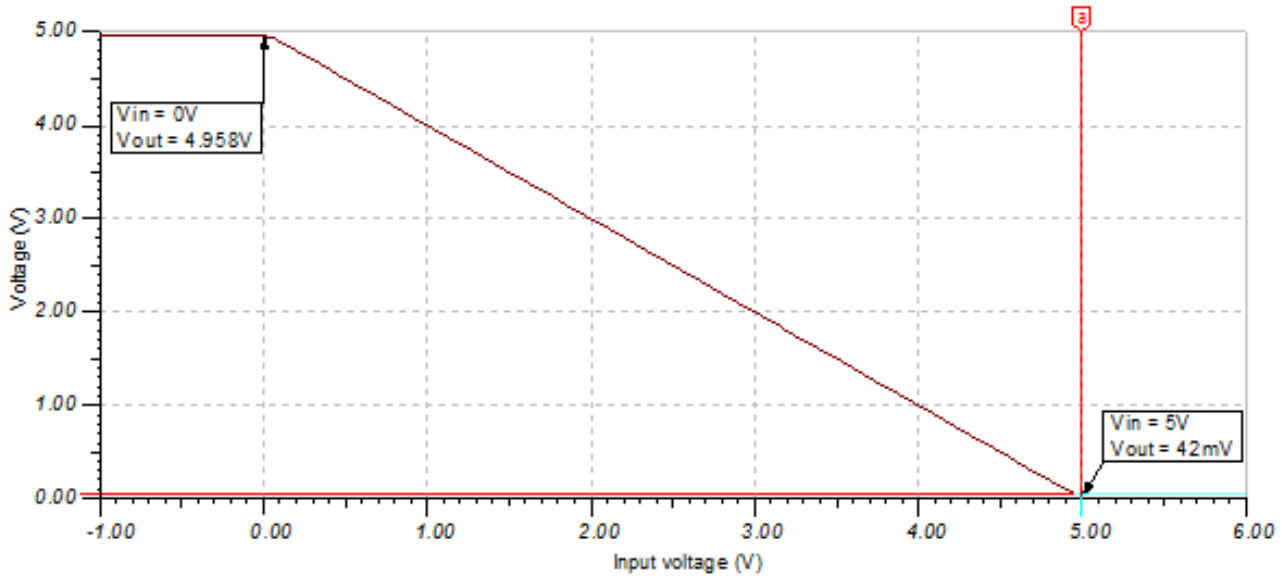
After clicking *Finish*, the filter schematic is displayed along with performance specifications of the resulting filter. Component tolerances can be adjusted using the right side drop-down menus; 1% resistors and 5% capacitors are chosen here as practical considerations. Component values can be modified by clicking on a number and entering new values.



The circuit previously pictured can be designed in TINA-TI for simulation. Performance characteristics are documented in the following sections.

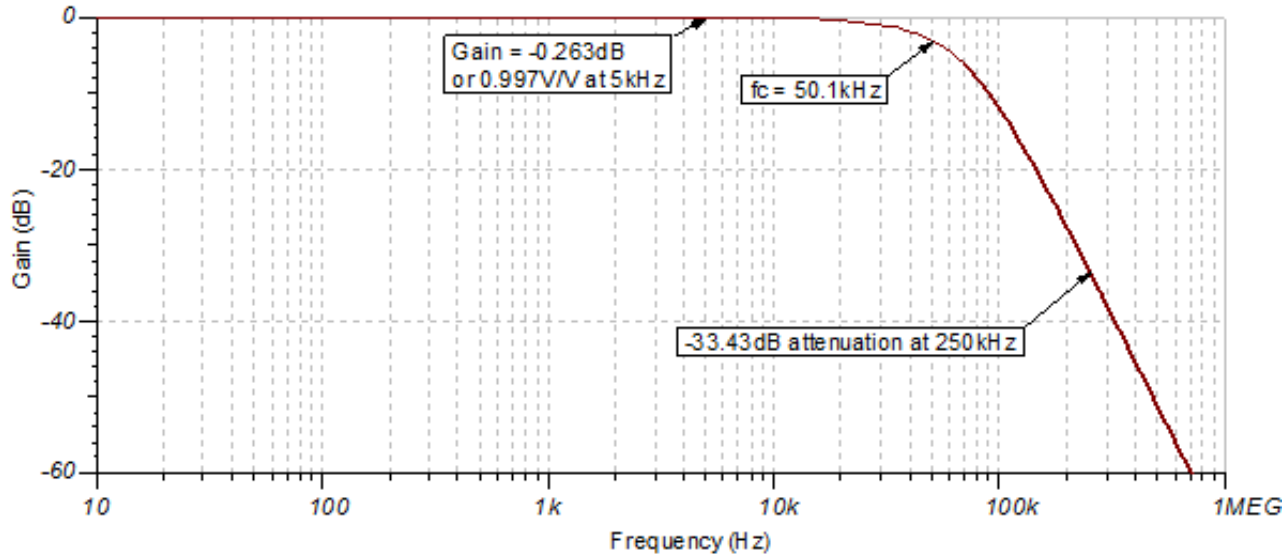
DC Transfer Characteristics

The following graph shows a linear output response for filter inputs from 0V to 5V. Since the filter amplifier is in inverting configuration, the output voltage is a function of $V_{out} = -V_{in} + 5V$.



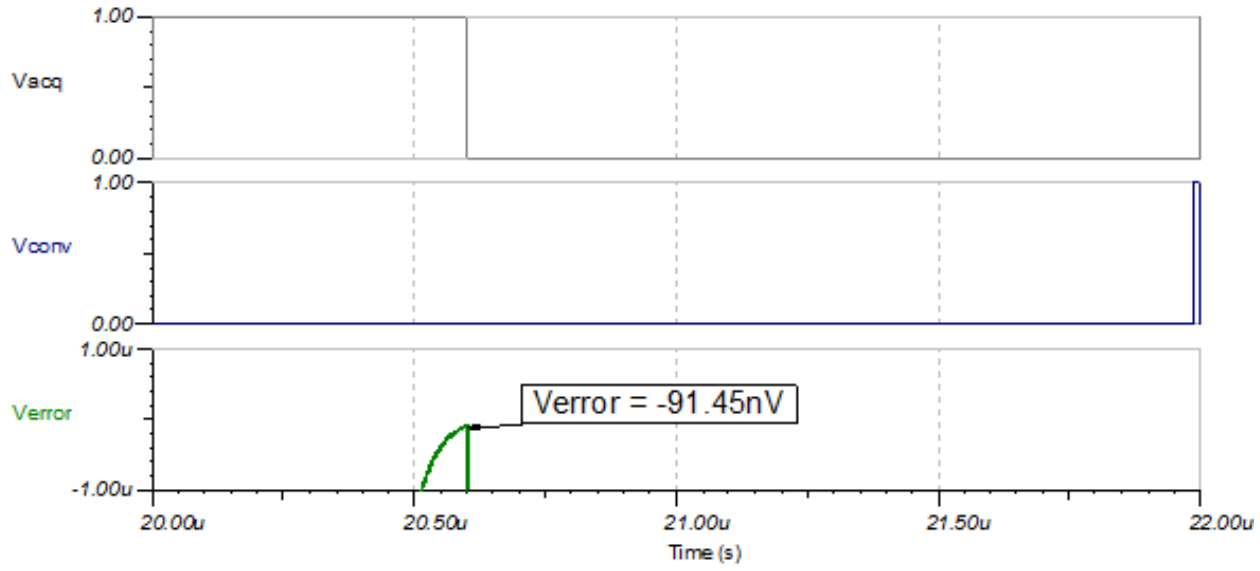
AC Transfer Characteristics

The bandwidth is simulated to be 50.1kHz, about 100Hz away from the desired value entered in the Analog Engineer's Calculator. At the Nyquist frequency, signals are attenuated by –33.43dB, which would lower the amplitude of the input alias signal to 21.3µV. See the TI Precision Labs *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows the ADS8319 settling to a 5-Vpp AC signal at 5kHz through the data acquisition period. This type of simulation shows that the RC charge bucket components are properly selected. See the TI Precision Labs video on *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.

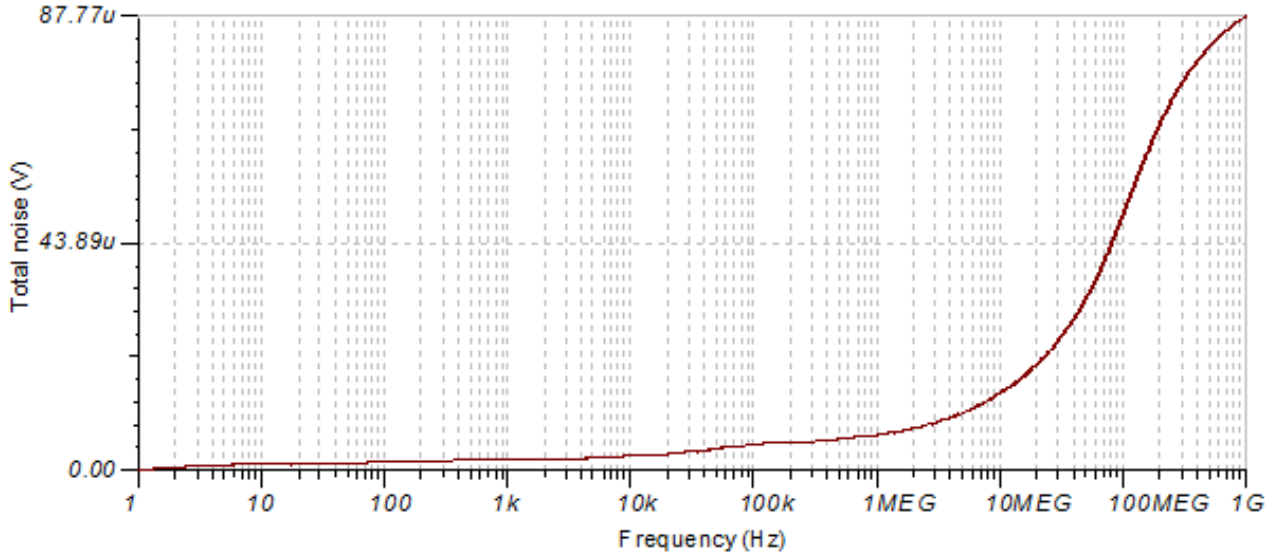


Noise Simulation

A simplified noise calculation is made here for a rough estimate. We neglect noise from the antialias filter in this calculation since it is attenuated for frequencies greater than 50kHz.

$$E_{nOPA365} = e_{nOPA365} \cdot G_{OPA}\sqrt{K_n \cdot f_c} = \left(7.2\,nV/\sqrt{Hz}\right) \cdot 1V/V\sqrt{1.57 \cdot 50MHz} = 63.8\mu V_{RMS}$$

The value for $e_{nOPA365}$ is taken from a data sheet noise curve. Note that calculated and simulated noise values match well. Some of the discrepancy between the simulated and calculated noise is due to inaccuracy from the bandwidth of the OPA365 model. See TI Precision Labs video on *Calculating the Total Noise for ADC Systems* for detailed theory on noise calculations.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8319	16-bit, 500kl, serial interface, micro-power, miniature, SAR ADC	Precision 16-Bit SAR Analog-to-Digital Converter (ADC) With SPI	Analog-to-digital converters (ADCs)
OPA365	50MHz, zero-crossover, low-distortion, high CMRR, RRI/O, single-supply operational amplifier	2.2V, 50MHz, Low-Noise, Single-Supply Rail-to-Rail Operational Amplifier	Operational amplifiers (op amps)

Link to Key Files

Texas Instruments, SBAC197 source files, support software

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (March 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to Data Converters. Added link to circuit cookbook landing page....	1

Trademarks

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Analog Engineer's Circuit

Circuit Showing Overstress Protection on ADC With Integrated Analog Front End

Dale Li

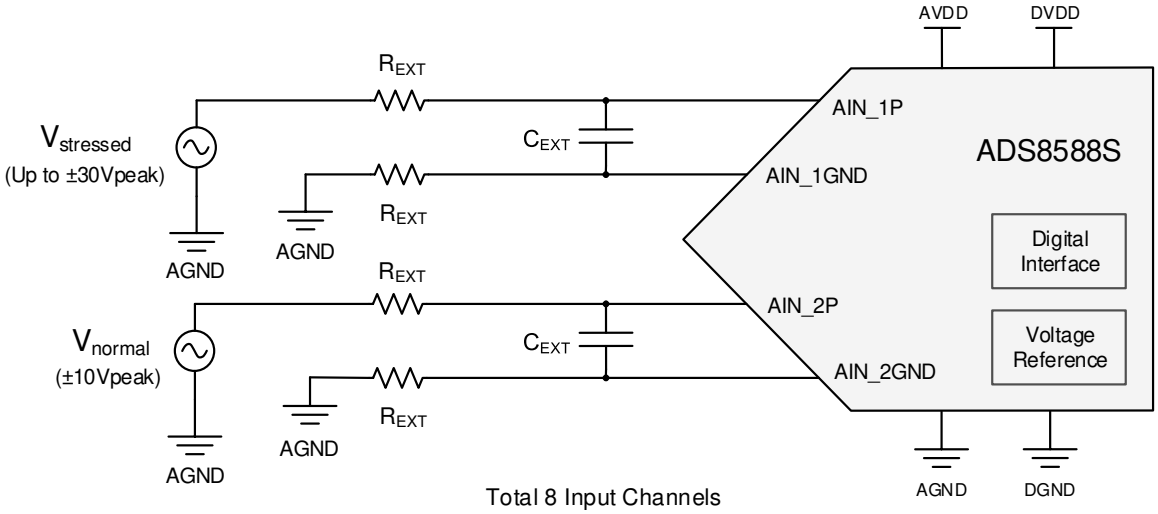
Input	ADC Input	Digital Output ADS7042
VinSEMin = –10V	CH_x = –10V	8000H
VinSE = 0V	CH_x = 0V	0000H
VinSEMax = +10V	CH_x = +10V	7FFFH

Power Supplies

AVDD	DVDD	Valid Input V_{normal}	Overvoltage Input $V_{stressed}$
5V	3.3V	±10V	

Design Description

For protection relay applications in smart grid markets, a simultaneous sampling ADC, such as ADS8588S, is widely used to maintain the phase information between different voltage and current. The working environment of these systems is very harsh and undesired signals with amplitudes up to ±30Vpk (60Vpp) can apply to the signal chain. Hence, it is important to protect the ADC input from overvoltage damage and also maintain good performance. This document shows how to design the overvoltage protection and also shows the performance impact of the overvoltage signal on adjacent channels. Finally, the performance impact results are compared between a Texas Instruments device and a pin for pin compatible competitor device.



Specifications

Specification	Calculated	Measured
60Vpp Overvoltage	Max Input Current = 1mA	SNR and THD performance and overvoltage feedthrough

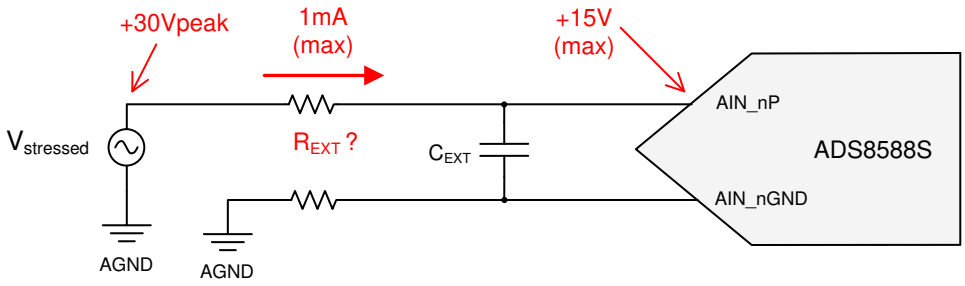
Design Notes

1. Use COG type capacitors for the C_{EXT} filter capacitor.
2. Review the *Electrical Overstress* video series for a theoretical explanation of overstress on amplifiers. Although this section covers amplifiers, the theory apples to data converters as well.

Component Selection

1. Find $R_{ext(min)}$ to limit the current less than 1mA. The suggested maximum current flowing into the ADS8588S input pins is ±10mA which is commonly required based on the internal structure of the ADC. This 10mA is an absolute maximum limit, and it is better to have some margins around this number, restricting the current less than 1mA is recommended. For this example design the minimum external resistance is 15kΩ.

$$R_{EXT} = \frac{30V - 15V}{1mA} = 15k\Omega$$

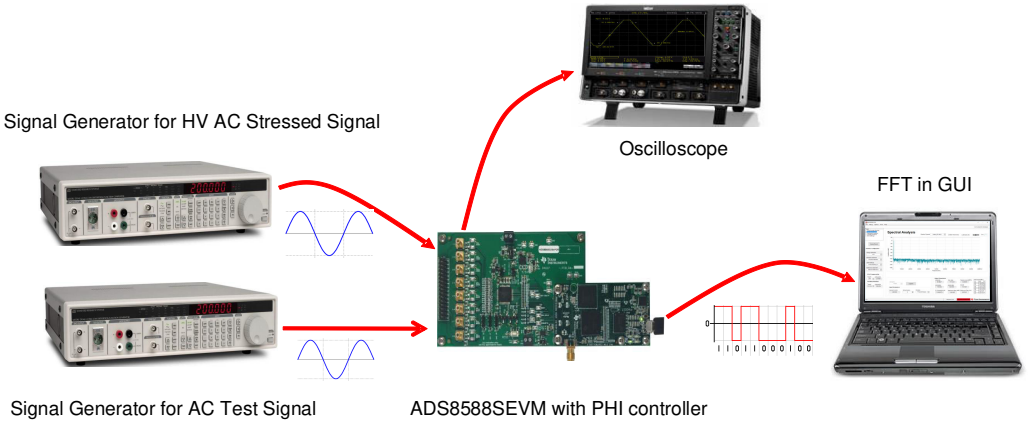


2. Choose R_{ext} or C_{ext} to set the bandwidth of the input filter to the desired frequency. Depending on the application, different cutoff frequencies are required. In this case the cutoff frequency must be 6.4kHz to accommodate 128 harmonics of a 50-Hz signal. In this case a 1-nF capacitor is also desired, as 1nF is a common industrial input filter capacitance value. After applying the equation, the external resistor (R_{ext}) is determined to be 24.9kΩ. Note that the external resistor calculated in this step is larger than the minimum resistance value from step 1 (is $R_{ext} > R_{ext(min)}$).

$$R_{EXT} = \frac{1}{2\pi \cdot f_c \cdot C_{EXT}} = \frac{1}{2\pi\,(6.4kHz)(1nF)} = 24.9k\Omega$$

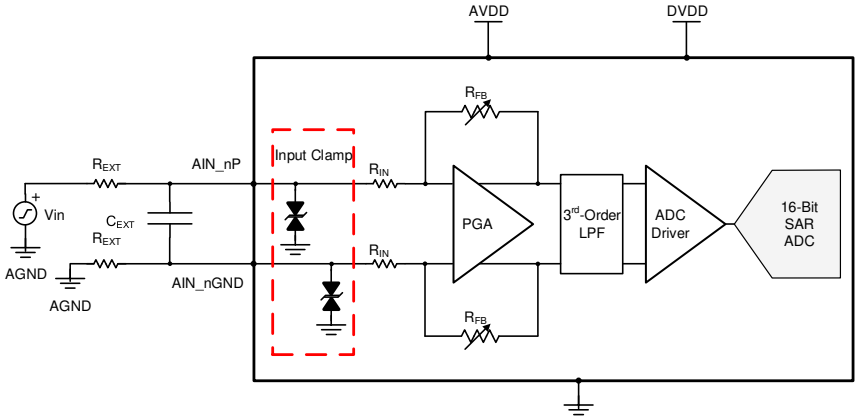
Test Setup

In a real world application with a multiple channel device, it is possible that one channel has an overvoltage signal applied to it and the other channels have valid signals on them. In this case it is desirable to have good performance on the channels with valid signals while protecting the channel with the overvoltage signal from damage. The measurements in this cookbook document are all done with an overvoltage signal applied to channel 1 and a valid signal applied to the other channels. All inputs are protected using the circuit designed in component selection. The following diagram shows the test setup.



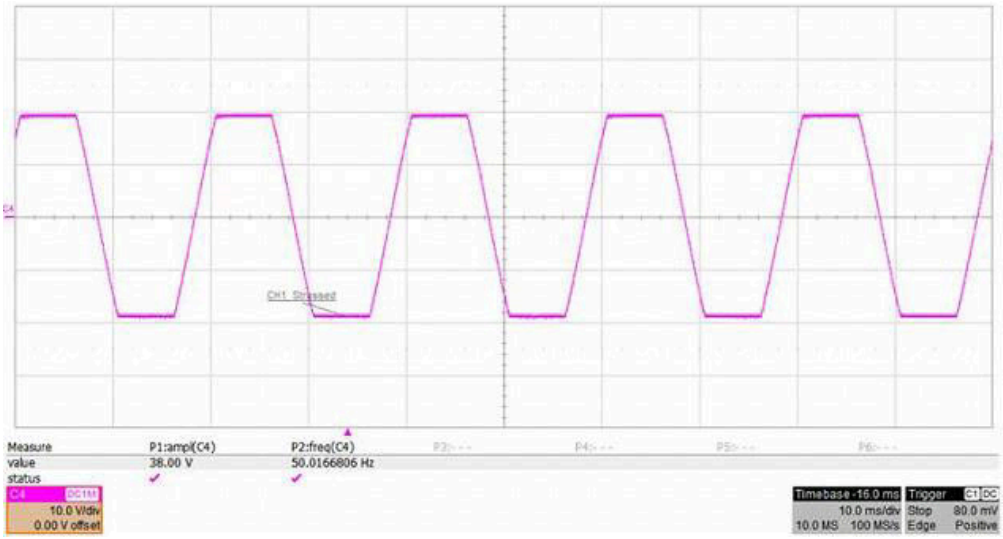
Device Protection

The following figure shows a simplified circuit for each analog input channel inside ADS8588S. An internal clamp protection circuit is designed on each of the 8 analog input channels and it allows each analog input to swing up to a maximum voltage of ±15V. For input voltages beyond ±15V the internal input clamp circuit turns on. Further increasing the overvoltage signal will result in higher current flow in the protection circuit (see the I-V Curve for input clamp protection circuit in the *ADS8588S 16-Bit, High-Speed, 8-Channel, Simultaneous-Sampling ADC with Bipolar Inputs on a Single Supply* data sheet). High input current can become destructive, degrading or even destroying the ADC device. This is why we limit the current to less than 1mA (see component selection section). Under a fault event the clamp protection circuit will turn on and limit the input voltage to approximately 15V and limit the current to less than 1mA.



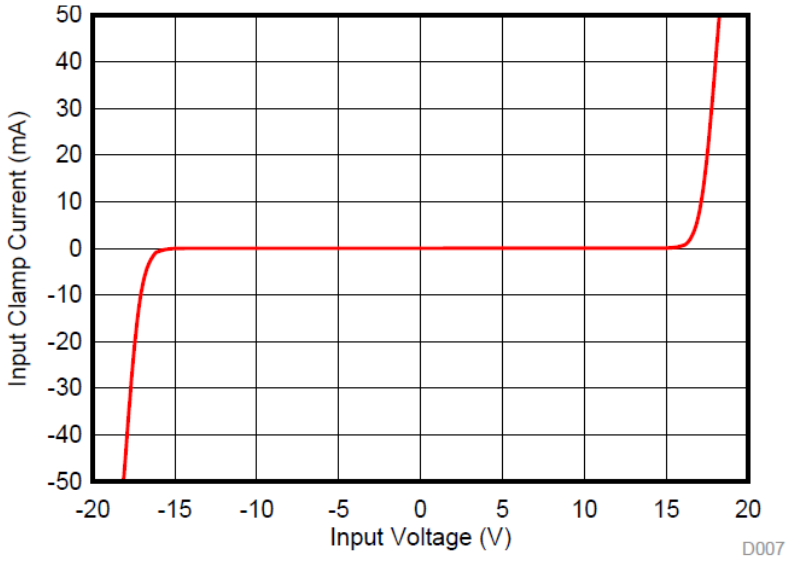
ADC Input (AIN_P) Under Overvoltage Condition

The following figure shows the ADC input voltage when the ±30Vpeak overvoltage signal is applied. Note that the clamp turns on and limits the ADC input to ±15Vpeak. The external resistor, R_{EXT}, limits the current to less than one milliamp to protect the ADC from damage.



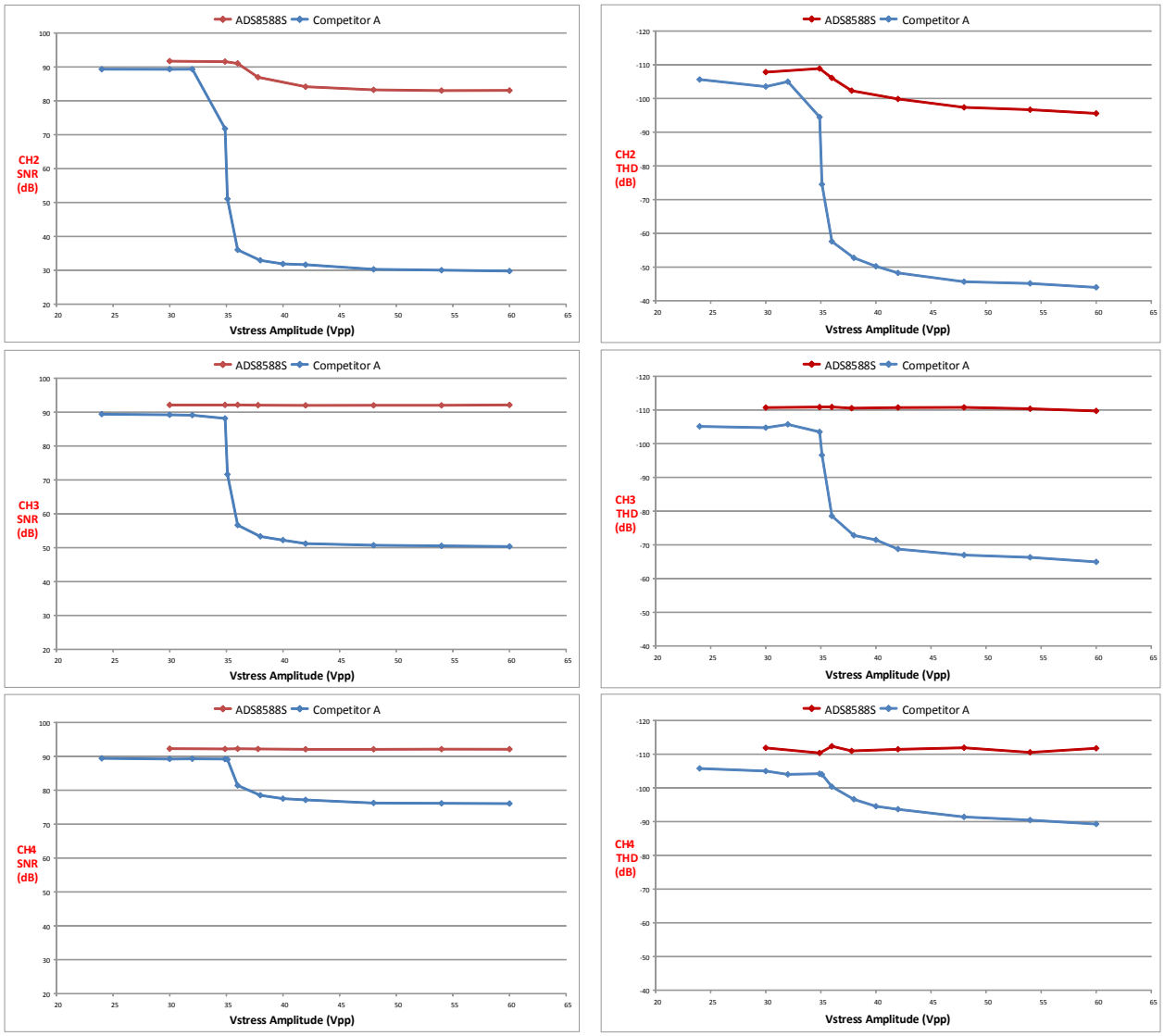
I-V Curve for the Internal Input Clamp Protection Circuit

The following figure shows the V-I curve for internal clamp. Note that it remains off and very low leakage for input voltage inside the ±15-V range. It turns on and limits the voltage outside of the ±15-V range.

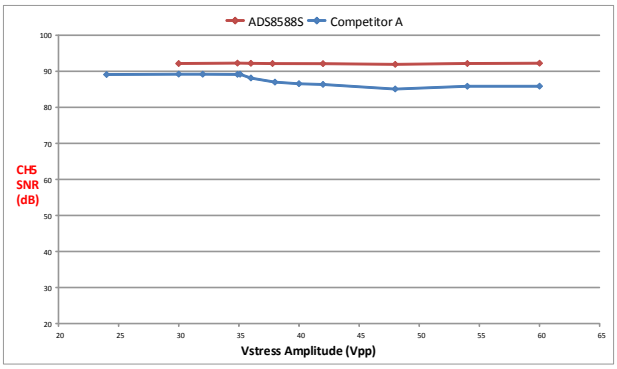


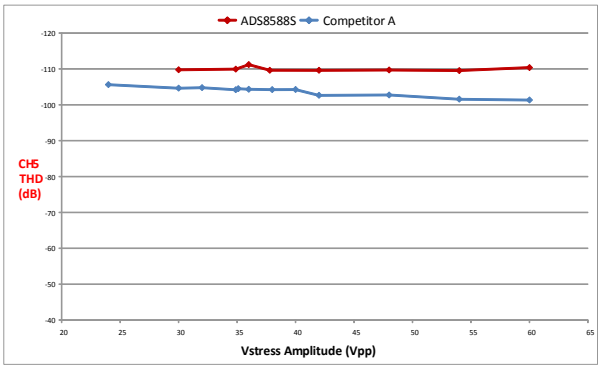
SNR and THD (Channel 1 = Overvoltage)

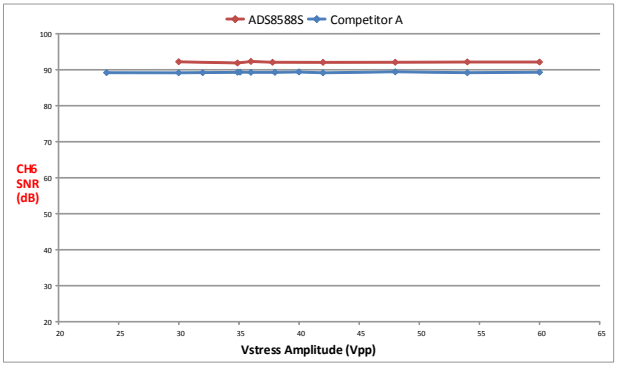
The following figures were taken with a ±30Vpeak (60Vpp) electrical overstress signal applied to channel 1 and the remainder of the channels are connected to a valid input signal (1kHz, –0.5dBFS sine wave). The SNR and THD of the channels with the valid input signal is measured with the overvoltage signal applied to channel 1. This test is done for the ADS8588S as well as a pin for pin comparable competitor device. Note that the ADS8588S SNR and THD are either not affected by the fault signal or the effect is minimal. Otherwise, the competitor device SNR and THD performance is substantially affected by the fault signal. Note that this circuit was also tested with ±15Vpeak, ±18Vpeak, ±21Vpeak, ±24Vpeak, and ±27Vpeak signals. As expected, larger overstress signals produce the worst-case results.

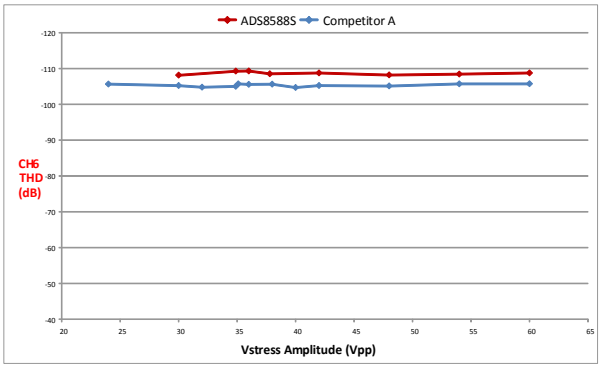


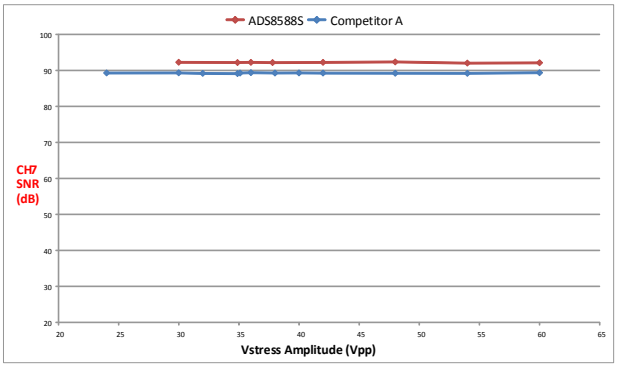
This is a continuation of the SNR and THD measurements where a ±30Vpeak (60Vpp) fault is applied to channel 1, and a valid input signal is applied to other channels performance verification.

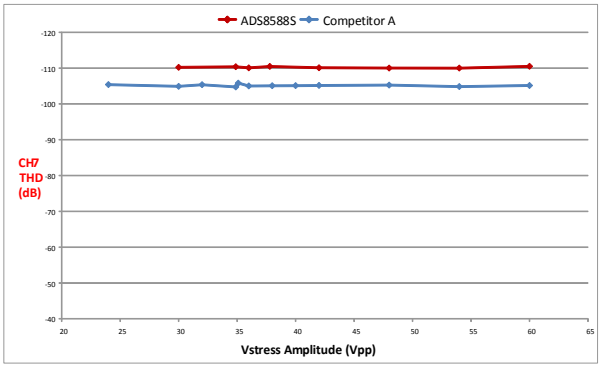


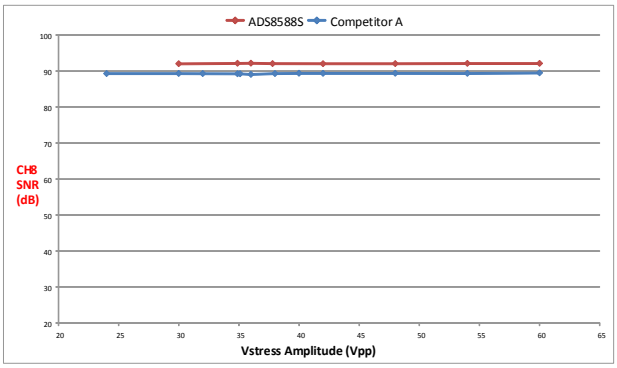


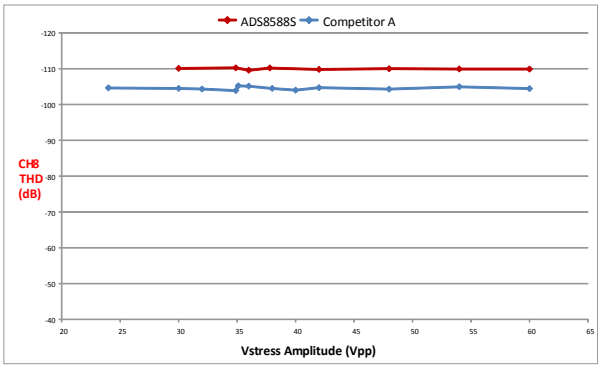






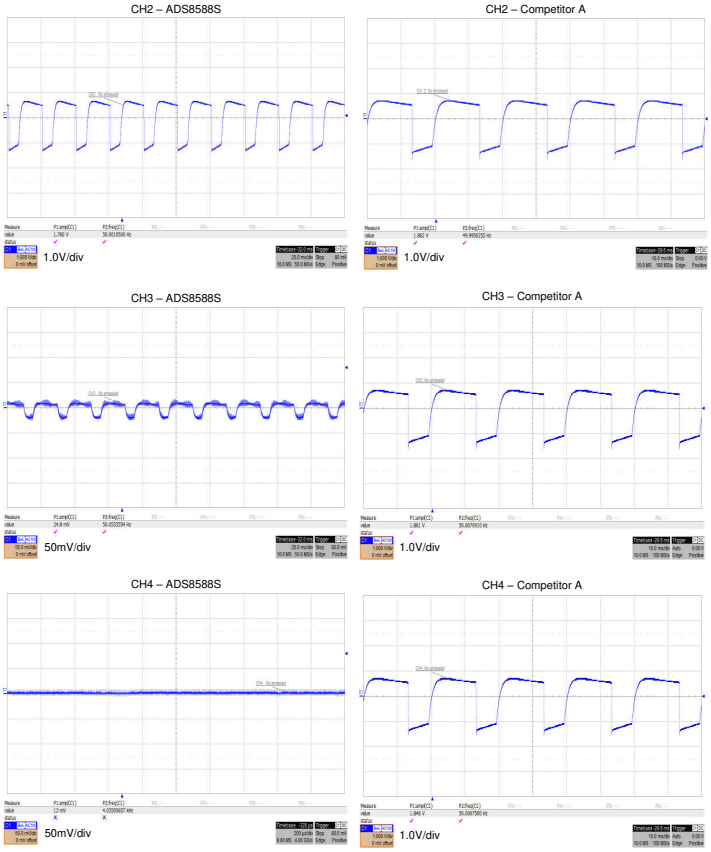




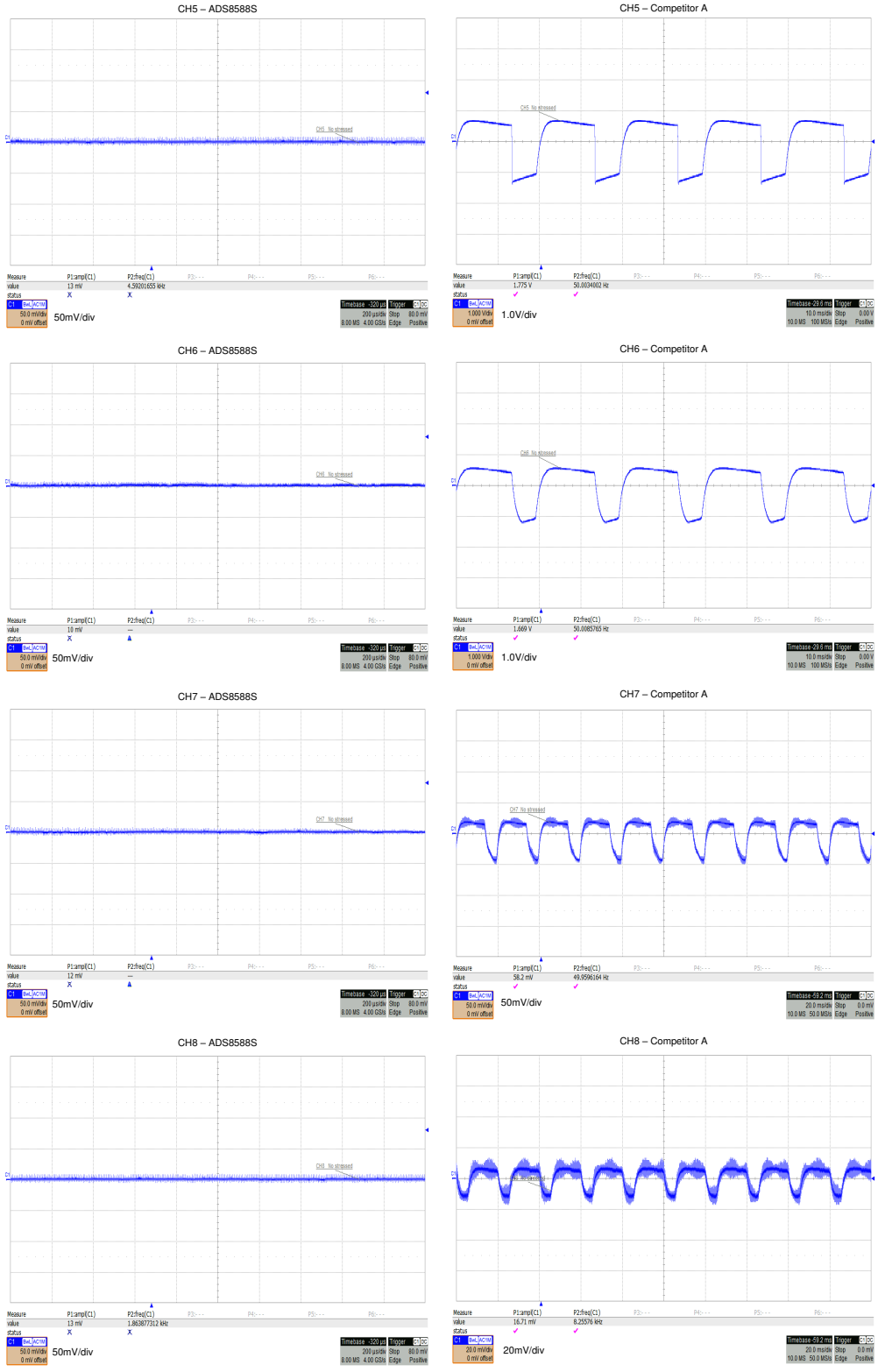


Feedthrough of Fault Signal to the Rest of the Channels

The following figures were taken with a ±30Vpeak (60Vpp) electrical overstress signal applied to channel 1 and the remainder of the channels are floating. The feedthrough of the overvoltage signal to the floating channels is measured using an oscilloscope. Note that both the ADS8588S and the competitor device are similar for channel 2. On the rest of the channels (CH3 to CH8) the feedthrough of the ADS8588S is much smaller than the TI device. This is a strong indication that for the ADS8588S the operation of channels with valid input signals will not be significantly impacted when one channel in the system has an overvoltage fault. Conversely, for the competitor device, all channels are adversely affected by the fault. Note that this circuit was also tested with ±15Vpeak, ±18Vpeak, ±21Vpeak, ±24Vpeak, and ±27Vpeak signals. As expected, larger overstress signals produce the worst case results.



This is a continuation of the feedthrough test showing that the ADS8588S channels with valid input signals are not affected by channels with faults.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8588S	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	16-Bit High-Speed 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply	Precision ADCs
REF5025	Low-noise, low drift, high precision voltage reference	2.5V, 3µVpp/V noise, 3-ppm/°C drift precision series voltage reference	Series voltage references

Design References

Texas Instruments, *Reducing Effects of External RC Filter Circuit on Gain and Drift Error for Integrated Analog Front Ends (AFEs): ±10V*, analog engineer's circuit

Texas Instruments, *Circuit to Increase Input Range on an Integrated Analog Front End (AFE) SAR ADC*, analog engineer's circuit

Trademarks

All trademarks are the property of their respective owners.

Analog Engineer's Circuit

Digitally-Isolated ADS8689 Circuit Design

Reed Kaczmarek

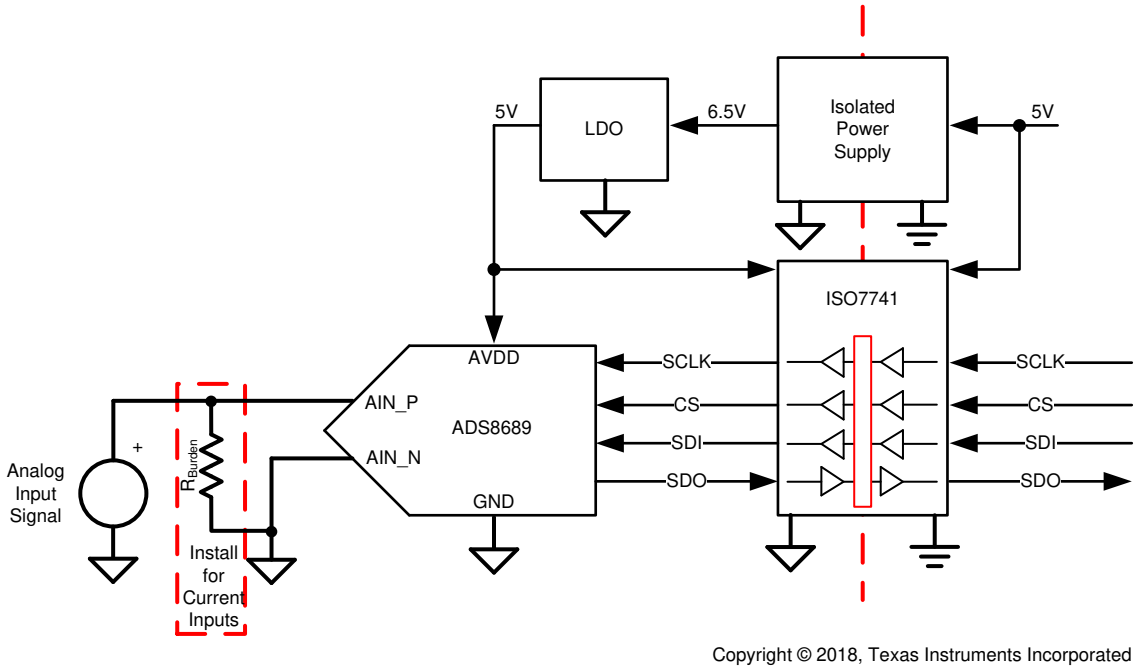
Input	ADC Input	Digital Output ADS7042
VinMin = –12.288V	AIN_P = –12.288V, AIN_N = 0V	8000_H or -32768_{10}
VinMax = 12.288V	AIN_P = 12.288V, AIN_N = 0V	$7FFF_H$ or 32767_{10}

Power Supplies		
AVDD	**Vee**	**Vdd**
5V	6.5V	5V

Design Description

This design shows a digitally isolated high-voltage SAR ADC that is capable of full AC performance at maximum throughput. This design is intended for channel-to-channel isolated analog input modules as well as measuring a signal with a very large common mode. Programmable logic controller, analog input modules, and many 4- to 20-mA signal applications benefit from this design. See *Isolated Power Supply Low-Noise, 5V, 100mA* for details on the isolated power supply design for these applications. This cookbook includes links to design files.

This circuit implementation is applicable in applications such as *Analog Input Modules*, *Electrocardiogram (ECG)*, *Pulse Oximeter*, and *Bedside Patient Monitors*.



Specifications

Specification	Calculated	Measured
SCLK Frequency	6.66MHz	6.67MHz
Sampling Rate	100ksps	100ksps
Signal-to-Noise Ratio (SNR)	92dB	Min: 92.29dB Max: 92.46dB
Total Harmonic Distortion (THD)	–112dB	Min: –108.8dB Max: –111.38dB

Design Notes

1. Select a SAR ADC that meets the input voltage range, sampling rate, and resolution for the system. This is covered in the *component selection* section.
2. Select a digital isolator that allows for the required isolation specification as well as the correct number of channels and channel directions. This is covered in the *component selection* section.
3. Install the burden resistor for current inputs. This design removes any common mode limitation of the inputs due to the channel-to-channel isolation. Select the burden resistor so that the maximum current input stays within the full scale range of the SAR ADC.

Component Selection

1. Select a SAR ADC that meets the input voltage range, sampling rate, and resolution for the system:
   - Desired input range: ±12V
   - Desired effective number of bits (ENOB): 14 bits
   - Desired sampling rate: 100ksps
   - ADS8689 input range: ±12.228V
   - ADS8689 ENOB: 14.8 bits
   - ADS8689 maximum sampling rate: 100ksps

   Note

   There is a wide selection of TI SAR ADCs that match the specifications in the previous list.
2. Select a digital isolator that allows for the required isolation specification as well as the correct number of bidirectional channels:
   - TI offers digital isolators with isolation rating ranging from 2.5kV_{RMS} to 5.7kV_{RMS}.
   - Choose isolation ratings based on the system requirements.
   - For a standard SPI interface, the digital isolator needs to be 4-channels with 3 channels in the same direction and 1 channel in the opposite direction.
   - The ISO774x is a digital isolator family for 4-channel devices with all combinations of channel directions and the ability to select a 2.5kV_{RMS} or a 5.0kV_{RMS} isolation rating.
3. Understand the expected delays to the digital signal from the digital isolator:
   - The ISO7741 has a typical propagation delay of 10.7ns with a maximum of 16ns.
   - Round trip isolation delay is 21.4ns typical or 32ns maximum.
   - SCLK is running at 6.66MHz resulting in a period of 150ns.
   - The typical round trip delay is 14% of the SCLK period.
   - The maximum round trip delay is 21% of the SCLK period.

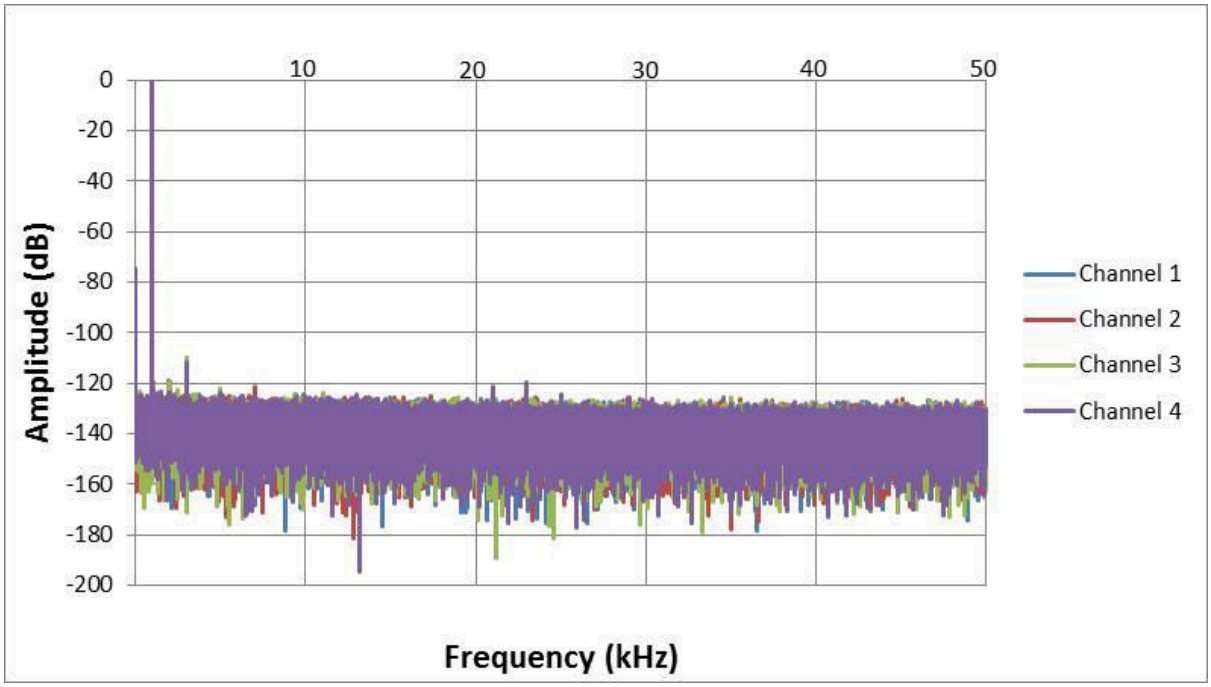
   Note

   The delay from the isolator results in a delay between the optimal SDO read relative to SCLK and the actual SDO read. This delay can be adjusted for by adding an SCLK return signal that travels through the digital isolator to all for the SDO to be read at exactly the correct time. Adding a return clock requires another channel of isolation.

Measured FFT

This performance was measured on a custom 4-channel, channel-to-channel isolated ADS8689 PCB. The input signal is a 24Vpp, 1-kHz sine wave. The AC performance indicates minimum SNR = 92.2dB and minimum THD = –108.8dB, which matches well with the specified performance of the ADC of SNR = 92dB and THD = –112dB.

Channel	SNR(dB)	THD (dB)
1	92.29	–109.95
2	92.38	–108.82
3	92.46	–109.53
4	92.42	–111.38



TVS Diode Performance Degradation

A 14-V bidirectional TVS diode was used in this design to protect the input of the SAR ADC. The TVS diode actually degrades total harmonic distortion (THD) due to the added capacitance. The THD was seen to be around 6dB worse with the TVS diode installed versus uninstalled.

Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8689 (1)	16 bit resolution, SPI, 100-ksps sample rate, single-ended input, and ±12.288-V input range.	16-Bit, 100-kSPS, 1-Ch SAR ADC with programmable (±12/±10/±6/±5/±2.5V) input ranges on +5V supply	Precision ADCs
ISO7741 (2)	High-speed, robust-EMC reinforced quad-channel digital isolator	Robust EMC, quad-channel, 3/1, reinforced digital isolator	Isolation

(1) The ADS8689 has in internal attenuator and programmable gain amplifier that allows for a wide input voltage range.
(2) The ISO7741 is used to isolate the digital input signals.

Link to Key Files

Texas Instruments, Source files for SBAA269, software support.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (February 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page	1

Trademarks

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Analog Engineer's Circuit

Reducing effects of external RC filter circuit on gain and drift error for integrated analog front ends (AFEs): ±10V

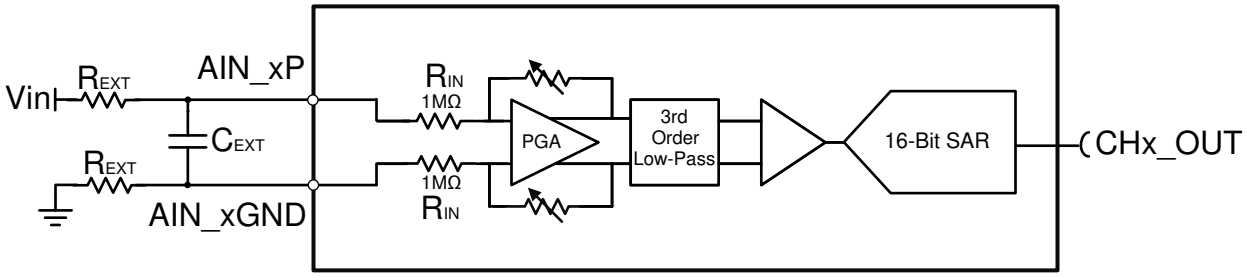
Cynthia Sosa

Input	ADC Input	Digital Output
VinMin = –10V	AIN-xP = –10V, AIN-xGND = 0V	-32768_{10}, 8000_{H}
VinMax = 10V	AIN-xP = 10V AIN-xGND = 0V	32767_{10}, $7FFF_{H}$

Power Supplies	
AVDD	**DVDD**
5V	5V

Design Description

This cookbook design describes how to select filter component values and how to minimize the gain error and drift introduced by this filter on a fully-integrated analog front end (AFE) SAR ADC. The design uses the input impedance drift at the full scale range of ±10V of the ADS8588S. This external RC filter minimizes external noise and provides protection from electrical overstress. Minimizing gain error and drift are important to end equipment such as: *Multi-Function Relays*, *AC Analog Input Modules*, and *Terminal Units*. This design describes two correction methods, a no-calibration correction factor and a 2-point calibration. Implementing calibration can minimize both the gain error introduced by the external resistor and the internal device gain error to negligible levels.



Specifications

Specification	Calculated	Measured
Introduced Gain Error (25°C)	0.9901%	0.9894%
Introduced Gain Error (125°C)	0.995%	–1.1388%
Introduced Gain Error Drift	0.49ppm/°C	–0.8031ppm/°C

Design Notes

1. Use low drift R_{EXT} resistors to maintain low drift and minimize gain error. This design uses resistors with a temperature coefficient of 25ppm/°C and ±0.1% tolerance.
2. The internal programmable gain amplifier (PGA) presents a constant resistive impedance of 1MΩ.
3. The R_{EXT} value introduced is directly proportional to the introduced error.
4. Calibration can also be used to eliminate system offset gain error.

5. The *TI Precision Labs – ADCs* training video series covers methods for calculating gain and offset error and eliminating these errors through calibration, see *Understanding and Calibrating the Offset and Gain for ADC Systems*. *Using SPICE Monte Carlo Tool for Statistical Error Analysis* explains how to use *Monte Carlo Analysis* for statistical error analysis.

Component Selection

External anti-aliasing RC filters reduce noise and protect from electrical overstress; if a large resistor value is used, then this further limits the input current. A large external resistive value also provides a low cutoff frequency, which is desired for relay protection applications as the input frequencies are usually 50 or 60Hz. Furthermore, a balanced RC filter configuration is required for better common-mode noise rejection; matching external resistors are present on both the negative and positive input paths. To minimize the introduced drift error, the external resistors needs to be low drift; 25ppm/°C resistors.

1. Choose a high-value R_{EXT} based on the desired cutoff frequency. A cutoff frequency of 320Hz was used to eliminate harmonics from a 50 or 60Hz input signal.

   R_{EXT} = 10kΩ
2. Choose C_{EXT}

$$C_{EXT} = \frac{1}{2 \cdot \pi \cdot f_C \cdot 2 \cdot R_{EXT}} = \frac{1}{2 \cdot \pi \cdot 320\,Hz \cdot 2 \cdot 10\,k\Omega} = 24.8\,nF$$

   Nearest standard capacitor value available, C_{EXT} = 24nF

Calculate Gain Error Drift

This section demonstrates how to calculate the introduced gain error drift. The additional drift from the external filter resistor is small compared to the internal device drift.

$$R_{IN} = 1M\Omega, \quad R_{EXT} = 10k\Omega, \quad C_{EXT} = 24nF$$

1. Calculate effective internal impedance due to maximum negative drift (–25ppm/°C)

$$R_{IN(-25ppm/°C)} = R_{IN} \cdot [Drift(ppm/°C) \cdot \delta T(°C) + 1]$$
$$R_{IN(-25ppm/°C)} = 1M\Omega \cdot [-25\,ppm/°C \cdot (125°C - 25°C) + 1]$$
$$R_{IN(-25ppm/°C)} = 0.9975\,M\Omega$$

2. Calculate effective external resistance due to maximum positive drift (25ppm/°C)

$$R_{EXT(+25ppm/°C)} = R_{EXT} \cdot [Drift(ppm/°C) \cdot \delta T(°C) + 1]$$
$$R_{EXT(+25ppm/°C)} = 10\,k\Omega \cdot [25\,ppm/°C \cdot (125°C - 25°C) + 1]$$
$$R_{EXT(+25ppm/°C)} = 10.025\,k\Omega$$

3. Calculate nominal gain error introduced by the external resistor at room temperature

$$GainError(R_{EXT})_{RoomTemp} = \frac{1}{1 + \frac{R_{IN}}{R_{EXT}}}$$
$$GainError(R_{EXT})_{RoomTemp} = \frac{1}{1 + \frac{1M\Omega}{10\,k\Omega}}$$
$$GainError(R_{EXT})_{RoomTemp} = 0.009901 \text{ or } 0.9901\%$$

4. Calculate nominal gain error introduced by the external resistor at highest rated temperature

$$GainError(R_{EXT})_{125°C} = \frac{1}{1 + \frac{0.9975\,M\Omega}{10.025\,k\Omega}}$$

$$GainError(R_{EXT})_{125°C} = 0.009950 \text{ or } 0.995\%$$

5. Calculate gain error drift introduced by the external resistor

$$GainError\_Drift(R_{EXT}) = \frac{GainError(R_{EXT})_{RoomTemp} - GainError(R_{EXT})_{125°C}}{\delta T} \cdot 10^6$$

$$GainError\_Drift(R_{EXT}) = \frac{0.009901 - 0.00950}{(125°C - 25°C)} \cdot 10^6$$

$$GainError\_Drift(R_{EXT}) = -0.49 ppm / °C$$

The maximum gain error temperature drift of the ADS8588S is ±14ppm/°C, which is orders of magnitude larger than the calculated drift error introduced, making the introduced error negligible. The minimal drift error introduced by the external resistors has greatly to do with the low drift coefficient of the input impedance (±25ppm/ºC).

To measure the introduced gain error drift, two test signals are sampled and applied at 0.5V from the full scale input range within the linear range of the ADC. The signals are applied and sampled with and without the external RC filter present. These measurements are performed at both temperatures, 25°C and 125°C. The percent gain errors are solved for by finding the percent error of the ideal slope and the measured slope for each of the four distinctive test conditions, resulting in four distinct percent gain error measurements. The drift (ppm/°C) with and without the RC present is then calculated by converting the percent gain errors to decimal format then following step 5 shown above. The introduced gain error drift is then solved for by subtracting the drift of the RC and no RC present.

Uncalibrated Correction

An uncalibrated correction targets to solve the input voltage before any losses occur due to the RC filter by working backwards from the ADC measured samples using a voltage divider.

1. Apply known test signal and measure equivalent code

V_{in}	Measured Code	Equivalent Measured Input
9.5V	30841	9.412

2. Calculate the input voltage before RC losses

$$V_{IN\_NoLoss} = V_{IN\_Equivalent} \cdot \frac{R_{EXT} + R_{IN}}{R_{IN}}$$

$$V_{IN\_NoLoss} = 9.412 \cdot \frac{1M\Omega + 10\,k\Omega}{1M\Omega}$$

$$V_{IN\_NoLoss} = 9.50612\,V$$

Uncalibrated Correction Measurements

Using a voltage correction can be beneficial, but not the most comprehensive. The correction factor can have a worst-case error of 0.2456% at room temperature due to change in internal impedance.

Room Temperature (25°C) Measurements				
V_{in}	Code	Reading	Correction	Error %
9.5	30841	9.412	9.506120	0.0644
8.5	27594	8.421	8.505210	0.0613

Room Temperature (25°C) Measurements				
V_{in}	Code	Reading	Correction	Error %
5	16232	4.954	5.003540	0.0708
0	1	0	0.000000	–
–5	–16230	–4.953	–5.002530	0.0506
–8.5	–27593	–8.421	–8.505210	0.0613
–9.5	–30839	–9.411	–9.505110	0.0538

2-Point Calibration Method

A two point calibration applies and samples two test signals at 0.5V from the full scale input range within the linear range of the ADC. These sample measurements are then used to calculate the slope and offset of the linear transfer function. Calibration eliminates both the gain error introduced by the external resistor and the internal device gain error.

1. Apply test signal at 2.5% of input linear range

Vmin	Measured Code
–9.5V	–30839

2. Apply test signal at 97.5% of input linear range

Vmax	Measured Code
9.5V	30841

3. Calculate slope and offset calibration coefficients

$$m = \frac{Code_{max} - Code_{min}}{V_{max} - V_{min}}$$

$$m = \frac{30841 - (-30839)}{9.5 - (-9.5)} = 3246.3158$$

$$b = Code_{min} - m \cdot V_{min}$$

$$b = (-30839) - 3246.3 \cdot (-9.5\,V) = 1.0001$$

4. Apply calibration coefficient to all subsequent measurements

$$Vin_{Calibrate} = \frac{Code - b}{m}$$

$$Vin_{Calibrate} = \frac{30841 - 1.0001}{3246.3158} = 9.5000$$

2-Point Calibration Method Measurements

Calibration Coefficients

m = 3246.3158; *b* = 1.0001

At room temperature without calibration, a gain error is present. Once calibration is applied to the measured results from the ADC, the gain error is minimized to nearly zero.

Room Temperature (25°C) Measurements					
V_{IN}	Code	Uncalibrated V_{IN}	Calibrated V_{IN}	Voltage Error Without Calibration %	Voltage Error With Calibration %
9.5	30841	9.412	9.500000	–0.926316	–0.000001
8.5	27594	8.421	8.499789	–0.929412	–0.002480

Room Temperature (25°C) Measurements					
V_{IN}	Code	Uncalibrated V_{IN}	Calibrated V_{IN}	Voltage Error Without Calibration %	Voltage Error With Calibration %
5	16232	16232	4.999822	–0.920000	–0.003568
0	1	0	0.000000	–	–
–5	–16230	–4.953	–4.999822	–0.0940000	–0.003567
–8.5	–27593	–8.421	–8.500097	–0.929412	0.001144
–9.5	–30839	–9.411	–9.500000	–0.936842	0.000000

When exposed to high temperatures, the gain error increases, as expected. Once calibration is applied, the voltage error is decreased but not eliminated; the error still present is the drift error.

High Temperature (125°C) Measurements					
V_{IN}	Code	Uncalibrated V_{IN}	Calibrated V_{IN}	Relative Voltage Error Without Calibration %	Relative Voltage Error With Calibration %
9.5	30826	9.407	9.495379	–0.978947	–0.048639
8.5	27582	8.417	8.496093	–0.976471	–0.045968
5	16224	4.951	4.997357	–0.980000	–0.052854
0	0	0	–0.000308	0	–
–5	–16224	–4.951	–4.997973	–0.980000	–0.040531
–8.5	–27581	–8.417	–8.496401	–0.976471	–0.042344
–9.5	–30826	–9.407	–9.495995	–0.978947	–0.042153

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8588S	16-bit, high-speed 8-channel simultaneous-sampling ADC with bipolar inputs on a single supply	www.ti.com/product/ADS8588S	www.ti.com/adcs

Trademarks

All trademarks are the property of their respective owners.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2019) to Revision B (September 2024) **Page**

- Updated the format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision * (April 2018) to Revision A (January 2019) **Page**

- Downscale title, updated header on first page..... 1

Analog Engineer's Circuit

Isolated Power Supply, Low-Noise Circuit: 5V, 100mA

Reed Kaczmarek

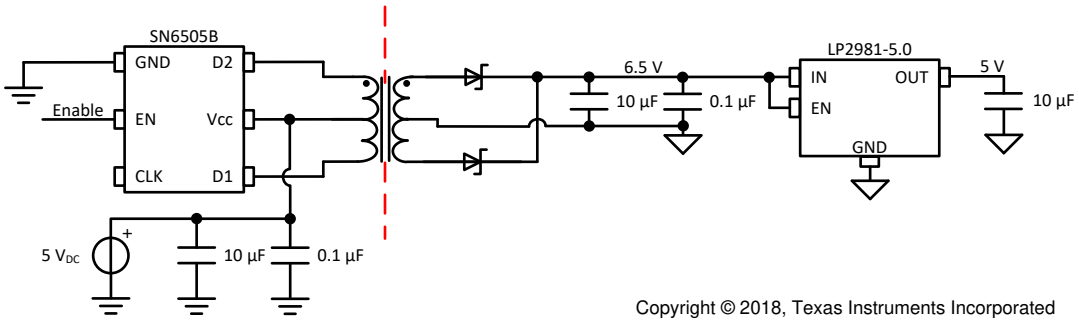
Power Supplies

AVDD	Vee	Vdd
5.0V	6.5V	5.0V

Design Description

This design shows an isolated power supply using a transformer driver and a low dropout regulator (LDO). This design is intended to be combined with a digitally-isolated SAR ADC, such as in a *Digitally-Isolated ADS8689 Design*. *Industrial applications* that require an isolation interface are the primary application for this design in combination with a SAR ADC. The transformer driver and LDO can be selected differently based on the output current requirements and output voltage noise requirements. This power supply was built and tested on a PCB with the ADS8689 and later in this document the performance of the ADS8689 is shown to prove the effectiveness of the power supply.

This circuit implementation is applicable in applications such as *analog input modules*, *electrocardiograms (ECGs)*, *pulse oximeters*, and *bedside patient monitors*.



Specifications

Specifications

Specification	Goal	Measured
LDO Output Current	< 100mA	16mA per channel
LDO Output Voltage Noise	< 1mV$_{RMS}$	N/A
ADS8689 Signal-to-Noise Ratio (SNR)	92dB	92.4dB
ADS8689 Total Harmonic Distortion (THD)	–112dB	111.3dB

Design Notes

1. Determine the supply current that is needed on the secondary side of the transformer. This information is used for component selection.
2. Choosing the transformer and transformer driver are very important to creating a correct isolated power supply.
3. The CLK pin on the SN6505B connects to an external clock or left floating to use the internal 420-kHz clock.

Component Selection

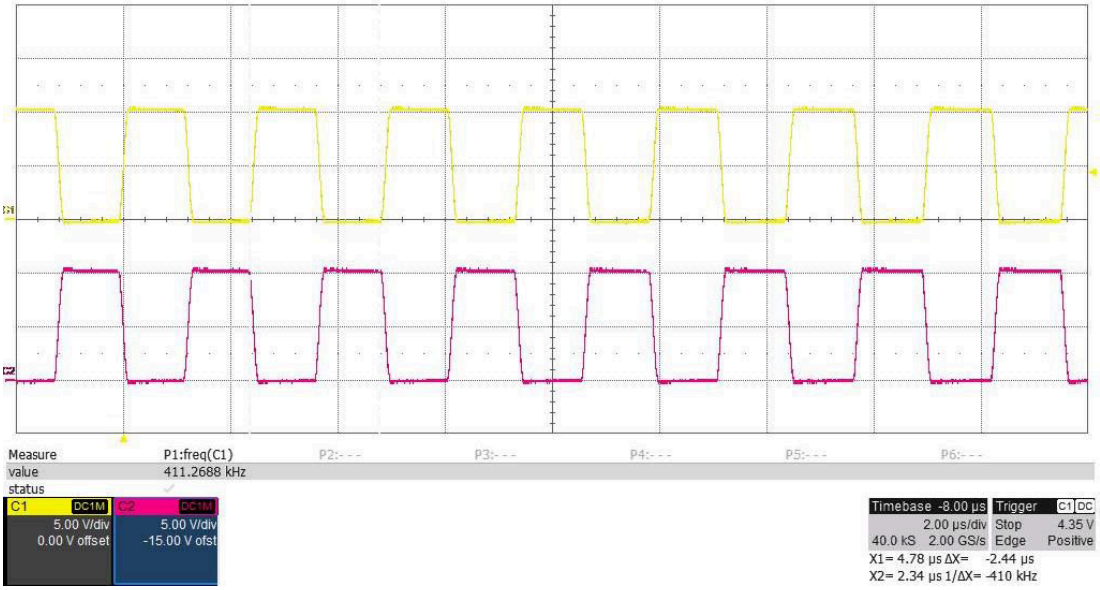
1. Select a transformer driver based on the required output current.
   - SN6505 will provide up to 1A of output current. The SN6505A has a 160-kHz internal clock and the SN6505B has a 420-kHz internal clock.
   - SN6501 will provide up to 350mA of output current.
2. Select a transformer with the desired turns ratio and current rating.
   - This design takes 5-V input and produces 6.5-V output. The turns ratio is determined as shown in the following:

$$\frac{n_p}{n_s} = \frac{V_{IN}}{V_{OUT}} = \frac{5V}{6.5V} = \frac{1}{1.3} \quad (1)$$

   - The 760390014 from Wurth Electronics was used in this design since it has a 1:1.3 turns ratio and a current rating that meets the 100-mA design specification.
3. Select a low dropout regulator (LDO) to use the transformer output and produce a low-noise supply voltage.
   a. Select the LDO to meet the output current requirement of the system and output voltage noise requirement of the system.
   b. The LP2981-5.0 is a fixed output voltage LDO that was selected for this design. This LDO is able to provide 100mA of output current. Also, the LDO output is accurate with only 160μV_{RMS} of output voltage noise.
4. Select the rectifier diodes for the fast switching of the SN6505B.
   - The *SN6505x Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet recommends using low-cost Schottky rectifier MBR0520L.
   - The forward voltage drop will take away from the output voltage of your isolated power supply.
   - The diodes must be rated for the expected current level for this supply.

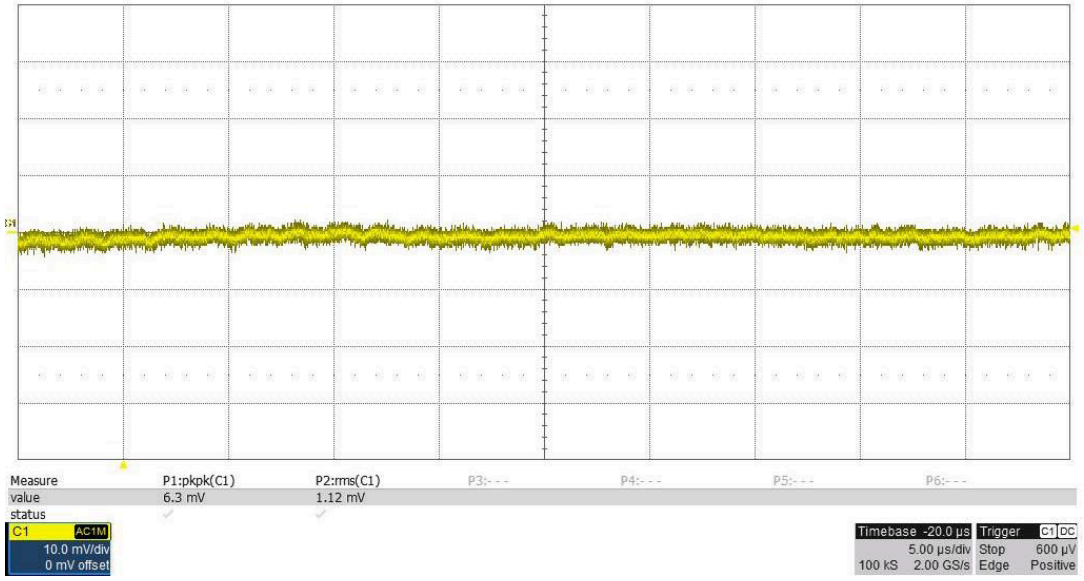
Measured Transformer Driver Outputs

The following image is an oscilloscope capture of the two transformer drive lines from the SN6505B. These are 0V to 5V pulses at a frequency of 411kHz.



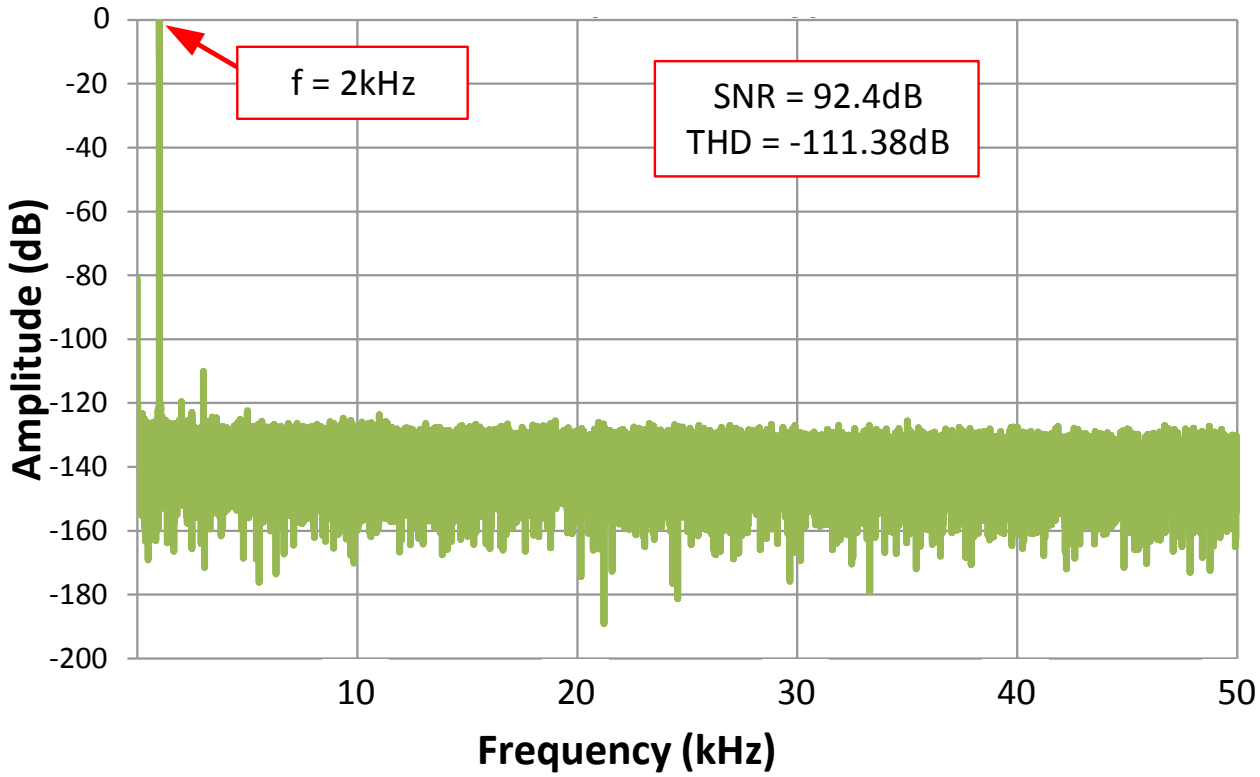
Measured SN6505B Stage Output Ripple

The following image is an oscilloscope capture of the output voltage following the rectifiers of the SN6505B power stage. This is the input to the LP2981-5.0 LDO. Result: 1.12mV_{RMS}.



Measured FFT

This power supply was implemented on a channel-to-channel isolated ADS8689 PCB. Measuring the AC performance of the ADS8689 proves the effectiveness of this isolated power supply. The AC performance indicates SNR = 92.4dB and THD = –111.3dB, which matches well with the specified performance of the ADC: SNR = 92dB and THD = –112dB).



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8689	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	16-Bit, 100kSPS, 1-Ch SAR ADC with programmable (±12/±10/±6/±5/±2.5V) input ranges on +5V supply	Analog-to-digital converters (ADCs)

(continued)

Device	Key Features	Link	Similar Devices
SN6505B	Low-Noise 1A, 420-kHz transformer driver	Low-noise, 1A, 420-kHz transformer driver with soft start for isolated power supplies	Transformer drivers
LP2981	100mA ultra-low dropout regulator with shutdown	100mA, 16V, low-dropout voltage regulator with enable	Linear and low-dropout (LDO) regulators

Trademarks

All trademarks are the property of their respective owners.

Revision History

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Changes from Revision A (March 2019) to Revision B (September 2024) **Page**

- Updated the format for tables, figures, and cross-references throughout the document 1

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- Downstyle the title and changed title role to Data Converters and added link to circuit cookbook landing page.....1

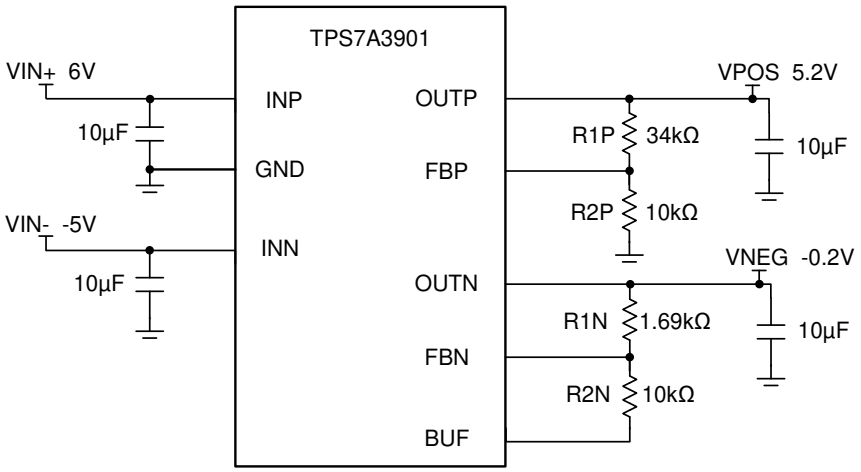
Analog Engineer's Circuit

Powering a dual-supply op-amp circuit with one LDO

LDO Input	LDO Output	Output Noise Level
Vin+ > 6V	5.2V	27µVRMS
Vin– < –5V	–200mV	22µVRMS

Design Description

This design shows a power supply that can be used to create a positive operational-amplifier (op amp) supply and a small negative op-amp supply. This small negative voltage is adjustable and is necessary in many operational amplifiers to verify linearity down to ground. This design shows the TPS7A3901 as the power supply for creating the positive and negative voltage rails for operational amplifier circuits. This low dropout regulator (LDO) differs from most in the ability to regulate small negative voltages, as the following image shows. This is a generic circuit implementation that can be used in many *Industrial* applications.



Specifications

Measured Performance of ADS8900B With LDO

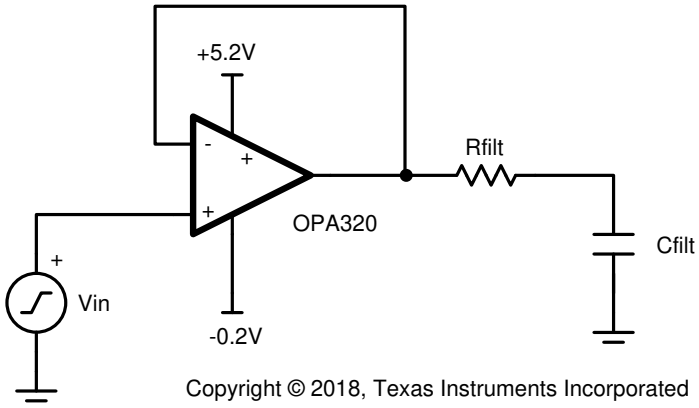
Parameter	Test Condition	Data Sheet Specification	Measured ADS8900B Performance
SNR	Vin_max = 5V, Vin_min = 0V	104.5dB	102.2dB
THD	Vin_max = 5V, Vin_min = 0V	–125dB	–123.5dB

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open-loop gain specification.
2. Set the adjustable LDO outputs to match the linear range of op amp.
3. Select X7R capacitors according to the temperature performance.
4. In cases where a negative supply is not available, an alternative method is to use a *Low Noise Negative Bias Generator* (LM7705).

Component Selection

1. A common configuration shows in the following image using an OPA320 in a buffer configuration with a 0V to 5V desired linear signal swing. The power supplies are both 200mV away from the desired input and output swing. This topology makes sure of linear input and output swing for this amplifier.

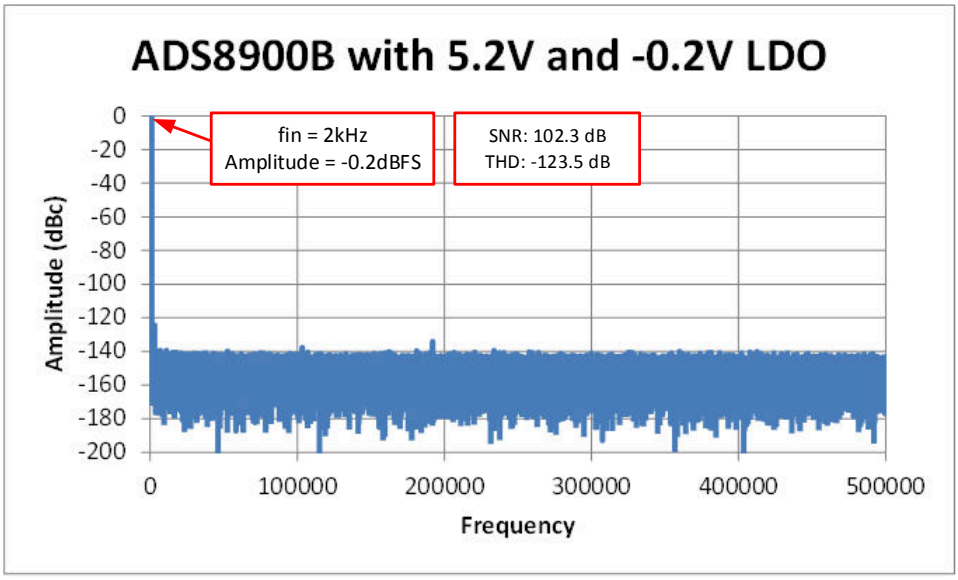


2. Select the components for the adjustable LDO outputs. Using the previous OPA320 example, the rails for the system are –200mV and +5.2V.

Desired Output	R1	R2
+5.2V	34kΩ	10kΩ
–200mV	1.69kΩ	10kΩ

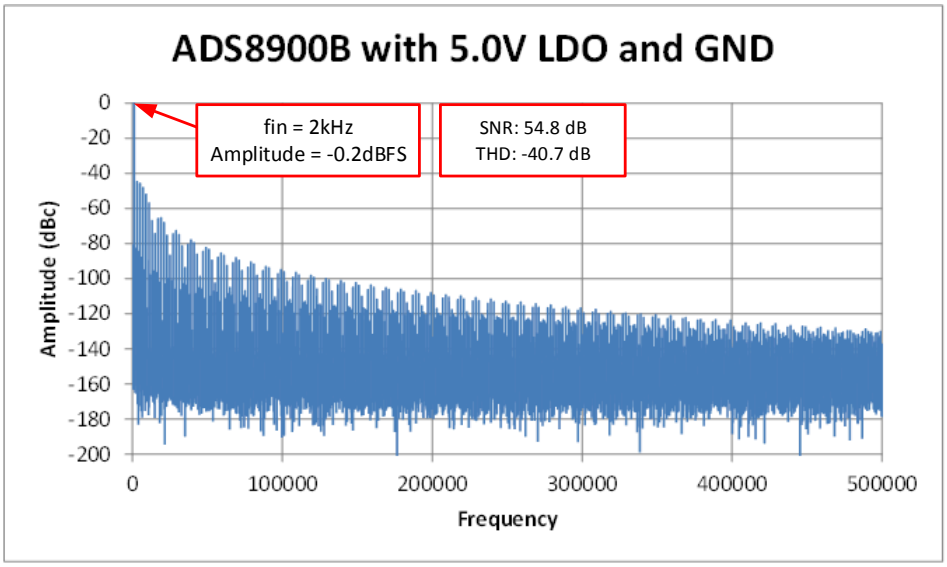
ADS8900B 20-Bit FFT Taken With LDO Adjusted to 5.2V and –0.2V

The FFT in the following was measured with an input signal very near full scale ±5V (–0.2dBFS). Note that the SNR and THD is very good compared to the case where the supply is adjusted to 5V and GND. Note the TPS7A3901 is a convenient way to generate a linear –0.2-V supply.



ADS8900B 20-Bit FFT Taken With LDO Adjusted to 5.0V and GND

The FFT shown in the following image was measured with an input signal very near full scale ±5V (–0.2dBFS). Note that the SNR and THD is poor compared to the case where the supply is adjusted to 5.2V and –0.2V.



Design Featured Devices

Device	Key Features	Link	Similar Devices
TPS7A3901	The TPS7A39 device is a dual, monolithic, high-PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150mA of current. The device has a wide output voltage range of 1.2V to 30V for the positive output and –30V to 0V for the negative output. This device is an excellent choice for generating a small negative supply voltage that is useful in cases where a single-supply amplifier needs a small negative supply so that the output can linearly swing to 0V.	www.ti.com/product/TPS7A39	www.ti.com/product/LM7705 (1)
ADS8900B	Bipolar differential inputs, SAR ADC with internal reference buffer, SPI interface	www.ti.com/product/ADS8900B	www.ti.com/adcs
OPA320	Precision, Zero-Crossover, 20Mhz, RRIO, CMOS Operational Amplifier	www.ti.com/product/opa320	www.ti.com/opamp

(1) The LM7705 is another option for a negative voltage supply and is not an LDO regulator, but instead the device is a switched-capacitor regulator.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Trademarks

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Analog Engineer's Circuit

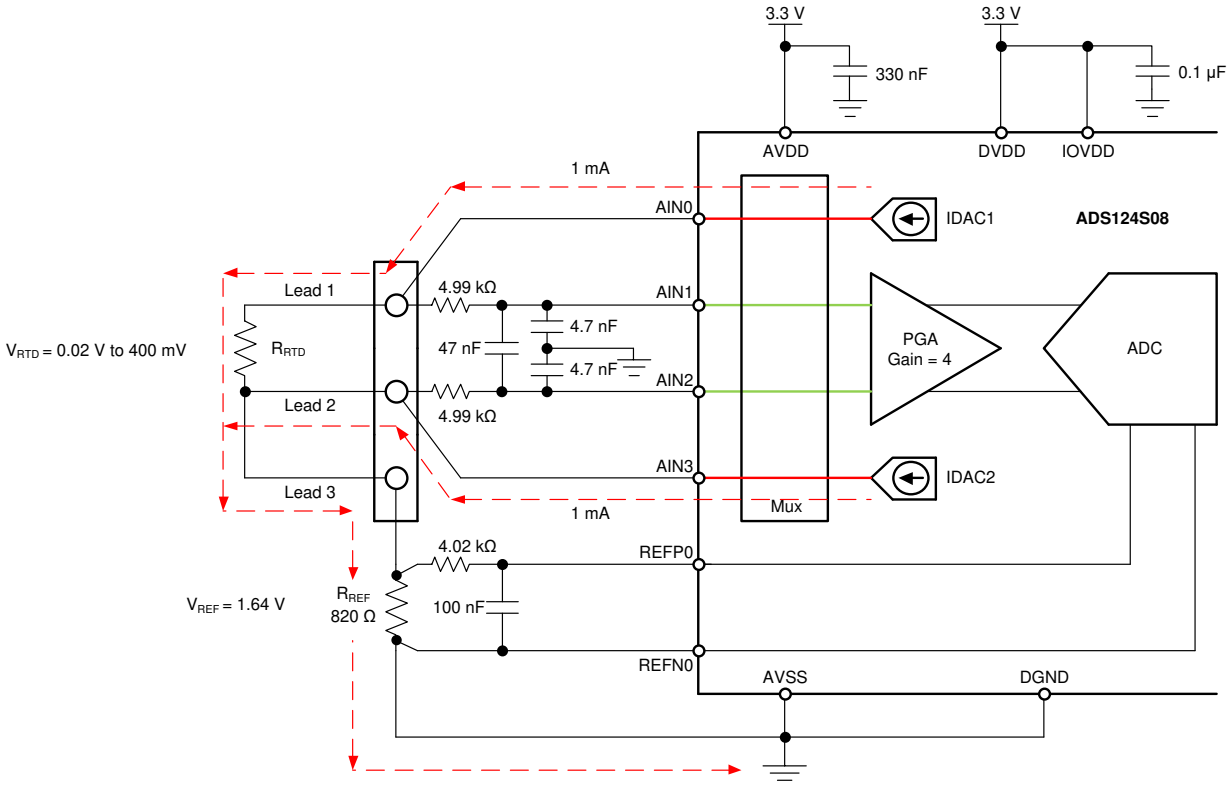
Three-Wire PT100 RTD Measurement Circuit With Low-Side Reference and Two IDAC Current Sources

Joseph Wu

Power Supplies		
AVDD	**AVSS**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD using the ADS124S08. This design uses two matched IDAC excitation currents for lead-resistance cancellation. This topology creates a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC register settings and pseudo code is provided to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.
7. This design shows connections to four input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, *thermocouple*, or other measurements.
8. Because of lead-resistance cancellation, the three-wire measurement offers more accuracy than comparable *two-wire RTD measurements*. For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Use two matched IDAC current sources to cancel the lead-resistance error.

   Two matched IDAC current sources are used for lead-resistance cancellation. Assuming the resistances of lead 1 and lead 2 are the same, and the currents of IDAC1 and IDAC2 are the same, then the lead-resistance error may be cancelled. Cancellation can be shown through the measured voltages at AIN1 and AIN2.

   IDAC1 drives current into the RTD through lead 1. IDAC2 drives a matched current into lead 2. The voltage at AIN1 is calculated with the following equation.

   $$V_{AIN1} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})$$

   At the same time, voltage at AIN2 is also calculated.

   $$V_{AIN2} = I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})$$

   The measurement of the ADC is the difference between AIN1 and AIN2, which is the subtraction of the first two equations to get the following.

   $$V_{AIN1} - V_{AIN2} = [I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})] - [I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})]$$

   The R_{LEAD3} and R_{REF} terms drop out.

   $$V_{AIN1} - V_{AIN2} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) - I_{IDAC2} \bullet R_{LEAD2}$$

So if R_{LEAD1} and R_{LEAD2} are equal and I_{IDAC1} and I_{IDAC2} are equal (to become I_{IDAC}), then the lead resistance errors cancel.

$V_{AIN1} – V_{AIN2} = I_{IDAC} • R_{RTD}$

3. Determine values for the IDAC excitation currents and reference resistor.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01°C.

   After selecting the IDAC current magnitude, set R_{REF} = 820Ω. Using two matched 1-mA excitation currents sets the reference at 1.64V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

   $V_{AIN1} = (I_{IDAC1} • R_{RTD}) + [(I_{IDAC1} + I_{IDAC2}) • R_{REF}] = (1mA • 400Ω) + (2mA • 820Ω) = 2.04V$

   $V_{AIN2} = (I_{IDAC1} + I_{IDAC2}) • R_{REF} = 2mA • 820Ω = 1.64V$

   $V_{INMAX} = 1mA • 400Ω = 400mV$

4. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As shown in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the absolute input voltage must satisfy the following:

   $AVSS + 0.15V + [|V_{INMAX}| • (Gain − 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD − 0.15V − [|V_{INMAX}| (Gain − 1) / 2]$

   $0V + 0.15V + [|V_{INMAX}| • (Gain − 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V − 0.15V − [|V_{INMAX}| (Gain − 1) / 2]$

   $0.75V < V_{AIN1}, V_{AIN2} < 2.55V$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.04V and 1.64V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage seen at the IDAC output is within the current source compliance voltage. The IDAC1 pin is AIN0 which has the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.04V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC pin must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $AVSS < V_{AIN0} = V_{AIN1} < AVDD − 0.6V$

   $0V < V_{AIN0} < 2.7V$

With the previous result, the output compliance of the IDAC1 is satisfied. Because the IDAC2 pin is always at a lower voltage than the IDAC1 voltage, both current sources are in the compliance range.

5. Select values for the differential and common-mode input filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $$f_{IN\_DIFF} = 1 / [2 \cdot \pi \cdot C_{IN\_DIFF} (R_{RTD} + 2 \cdot R_{IN})]$$

   $$f_{IN\_CM} = 1 / [2 \cdot \pi \cdot C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$$

   For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.6kHz.

   The bandwidth for the reference input filtering is approximated in the following equation.

   $$f_{REF} = 1 / [2 \cdot \pi \cdot C_{REF} \cdot (R_{REF} + R_{IN\_REF})]$$

   For the reference input filtering, R_{IN_REF} = 4.02kΩ and C_{REF} = 100nF. This sets the differential filter bandwidth to 330Hz. Because REFN0 is set to ground, the common-mode filtering is removed. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidth close may reduce noise in the measurement.

   For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

6. If IDAC current mismatch error is significant, use two measurements to chop the error (optional).

   One of the original assumptions in the lead-resistance cancellation is that IDAC1 and IDAC2 match. If the two IDAC currents do not match, the mismatch causes an error that appears as gain error. The voltage across the RTD comes from the current of IDAC1, while the voltage across the reference resistor comes from the current of IDAC1 + IDAC2. For the ADS124S08, the typical IDAC current mismatch for a 1-mA IDAC current is 0.07%. This mismatch error leads to a gain error of 0.35% in the measurement. To remove this current mismatch error, the IDAC excitation currents may be chopped. This involves taking two measurements with the IDAC currents swapped.

   For chopping, first take a measurement with IDAC1 set to AIN0 and IDAC2 set to AIN3. Then set IDAC1 to AIN3 and IDAC2 to AIN0, swapping the current sources, and take a second measurement. In the first case, IDAC1 drives the RTD, in the second case IDAC2 drives the RTD. In both cases, the sum of IDAC1 and IDAC2 drive the reference resistor. By averaging the two chopped cases, the mismatch error is removed from the measurement. For a more detailed analysis of chopping see the IDAC Current Chopping section of the *A Basic Guide to RTD Measurements* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as

a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC (without IDAC current chopping):

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot (V_{RTD} / V_{REF}) = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC1} \cdot R_{RTD}) / [(I_{IDAC1} + I_{IDAC2}) \cdot R_{REF}]$$

If I_{IDAC1} is equal to I_{IDAC2} then the IDAC current terms drop out.

$$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC} \cdot R_{RTD}) / (2 \cdot I_{IDAC} \cdot R_{REF}) = 2^{22} \cdot \text{Gain} \cdot (R_{RTD} / R_{REF})$$

$$R_{RTD} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{22})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Three-Wire PT100 RTD Measurement with Low-Side Reference and Two IDAC Current Sources Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	12h	Positive reference buffer enabled, negative reference buffer disabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	30h	IDAC1 set to AIN0, IDAC2 set to AIN3
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation
07h (1)	IDACMUX	03h	IDAC1 set to AIN3, IDAC2 set to AIN0

(1) This second IDACMUX setting and conversion is used for chopping IDAC excitation current sources (optional).

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 *firmware example code* is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;// RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
05// Write to 6 registers
12// Select AINP = AIN1 and AINN = AIN2
0A// PGA enabled, Gain = 8
14// Continuous conversion mode, low-latency filter, 20-SPS data rate
12// Positive reference buffer enabled, negative reference buffer disabled,
  // REFP1 and REFN1 reference selected, internal reference always on
07// IDAC magnitude set to 1mA
30;// IDAC1 set to AIN0, IDAC2 set to AIN3
Set CS high;
Set CS low; // For verification, read back configuration registers
Send 22// RREG starting at 02h address
```

```
05// Read from 6 registers
00 00 00 00 00 00;// Send 6 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Set CS low;// Configure the device for first chopped measurement
Send 47// WREG starting at 07h address
00// Write to 1 register
30;// IDAC1 set to AIN0, IDAC2 set to AIN3
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data, Record Measurement 1
Set CS high;
Set CS low;// Configure the device for chopped current sources (optional)
Send 47// WREG starting at 07h address
00// Write to 1 register
03;// IDAC1 set to AIN3, IDAC2 set to AIN0
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data, Record Measurement 2
Set CS high;
Average Measurement 1 and Measurement 2;
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*

- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2020) to Revision C (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

Analog Engineer's Circuit

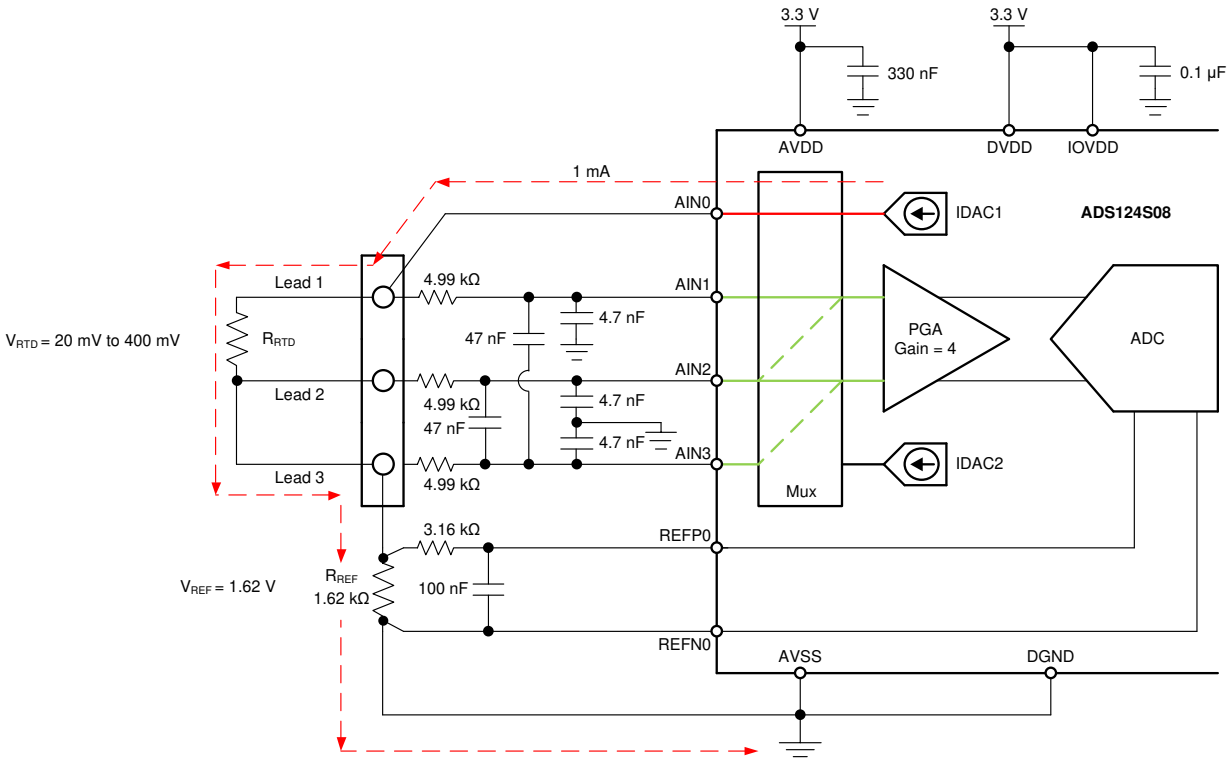
Three-Wire PT100 RTD Measurement Circuit With Low-Side Reference and One IDAC Current Source

Joseph Wu

Power Supplies		
AVDD	**AVSS, DGND**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD with a low-side reference using the ADS124S08. In comparison to a *Three-Wire PT100 RTD Measurement Circuit With Low- Side Reference and Two IDAC Current Sources* with a single measurement, this design uses a single IDAC excitation current source and a second measurement to remove the lead resistance error. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.
7. This design shows connections to four input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The three-wire RTD measurement offers more accuracy than comparable two-wire RTD measurements but also gives better immunity from the IDAC current mismatch than with a three-wire RTD measurement using matched IDAC current sources. For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   Start with a design where the excitation current is driven into lead 1 of the RTD, flowing through the RTD, and out the RTD through lead 3. At this point, ignore the lead resistance error, so that the measurement from AIN1 to AIN2 only measures the RTD resistance.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01°C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD} + R_{REF}) = 1mA \cdot (400\Omega + 1620\Omega) = 2.02V$

$V_{AIN2} = I_{IDAC1} \cdot R_{REF} = 1mA \cdot 1620\Omega = 1.62V$

$V_{INMAX} = 1mA \cdot 400\Omega = 400mV$

3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As shown in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the absolute input voltage must satisfy the following:

   $AVSS + 0.15V + [|V_{INMAX}| \cdot (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0V + 0.15V + [|V_{INMAX}| \cdot (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0.75V < V_{AIN1}, V_{AIN2} < 2.55 V$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02V and 1.62V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

   $0V < V_{AIN0} < 2.7V$

   With the previous result, the output compliance of the IDAC is satisfied.

4. Use two different measurements to measure the RTD resistance and cancel the lead-resistance error.

   The first measurement of the ADC is measured across AIN1 and AIN2, with the lead resistances included.

   $\text{Measurement 1} = V_{AIN1} - V_{AIN2} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})$

   Because the IDAC current does not pass through lead 2, its resistance is never part of the measurement. The input multiplexer of the ADC is then set to make a second measurement across AIN2 and AIN3. This measures the voltage drop across the resistance from lead 3.

   $\text{Measurement 2} = V_{AIN2} - V_{AIN3} = I_{IDAC1} \cdot R_{LEAD3}$

   Measurement 2 is subtracted from measurement 1 to get the following result.

   $\text{Measurement 1} - \text{Measurement 2} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] - (I_{IDAC1} \cdot R_{LEAD3})$

   If the lead resistances are equal, then the lead-resistance error drops out to get the final result.

   $\text{Measurement 1} - \text{Measurement 2} = I_{IDAC1} \cdot R_{RTD}$

5. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are

selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10 kΩ, to allow for proper input sampling for the ADC.

With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

$$f_{IN\_DIFF} = 1 / [2 \cdot \pi \cdot C_{IN\_DIFF} (R_{RTD} + 2 \cdot R_{IN})]$$

$$f_{IN\_CM} = 1 / [2 \cdot \pi \cdot C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$$

For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5kHz.

The bandwidth for the reference input filtering is approximated in the following equation.

$$f_{REF} = 1 / [2 \cdot \pi \cdot C_{REF} \cdot (R_{REF} + R_{IN\_REF})]$$

For the reference input filtering, R_{IN_REF} = 3.16kΩ and C_{REF_DIFF} = 100nF. This sets the reference filter bandwidth to 330Hz. Because REFN0 is set to ground, the common-mode filtering is removed. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC. First, the result from measurement 1 is shown.

$$\text{Output Code 1} = 2^{23} \cdot \text{Gain} \cdot [(V_{RTD} + V_{LEAD1}) / V_{REF}] = 2^{23} \cdot \text{Gain} \cdot [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot [(R_{RTD} + R_{LEAD1}) / R_{REF}]$$

$$R_{RTD} + R_{LEAD1} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{23})]$$

Then the result from measurement 2 is shown.

$$\text{Output Code 2} = 2^{23} \cdot \text{Gain} \cdot (V_{LEAD3} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC1} \cdot R_{LEAD3}) / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot (R_{LEAD1} / R_{REF})$$

$$R_{LEAD3} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{23})]$$

If the lead resistances are assumed to be equal, then the subtract the result of measurement 2 from measurement 1 to get the equivalent RTD resistance.

$$R_{RTD} = R_{REF} \cdot [(\text{Output Code 1} - \text{Output Code 2}) / (\text{Gain} \cdot 2^{23})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Three-Wire PT100 RTD Measurement Circuit with Low-Side Reference and One IDAC Current Source Using the ADS124S08

Register Address	Register Name	Setting	Description
02h(1)	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	12h	Positive reference buffer enabled, negative reference buffer disabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation
02h(2)	INPMUX	23h	Select AINP = AIN2 and AINN = AIN3

(1) This input multiplexer setting is for measurement 1.
(2) This input multiplexer setting is for measurement 2, as a measurement of the lead-resistance error.

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;// RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
05// Write to 6 registers
12// Select AINP = AIN1 and AINN = AIN2
0A// PGA enabled, Gain = 4
14// Continuous conversion mode, low-latency filter, 20-SPS data rate
12// Positive reference buffer enabled, negative reference buffer disabled
  // REFP0 and REFN0 reference selected, internal reference always on
07// IDAC magnitude set to 1mA
F0;// IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low; // For verification, read back configuration registers
Send 22// RREG starting at 02h address
05// Read from 6 registers
00 00 00 00 00 00;// Send 6 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Set CS low;// Configure the device for measurement 1
Send 42// WREG starting at 02h address
00// Write to 1 register
12;// Select AINP = AIN1 and AINN = AIN2
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
```

```
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
Set CS low;// Configure the device for measurement 2
Send 42// WREG starting at 02h address
00// Write to 1 register
23;// Select AINP = AIN2 and AINN = AIN3
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
Subtract measurement 2 from measurement 1;// Remove lead-resistance error
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*
- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements*
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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2020) to Revision B (September 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

Changes from Revision * (December 2018) to Revision A (March 2020)	Page
• Changed schematic to remove filtering from REFN0	1
• Changed bandwidth calculation for reference input filter	1
• Changed Register Settings Table to disable negative reference buffer	1
• Changed Pseudo Code Example to disable negative reference buffer	1

Analog Engineer's Circuit

Ultra-Small, Precision Analog Temperature Sensor Measurement Circuit With ADC

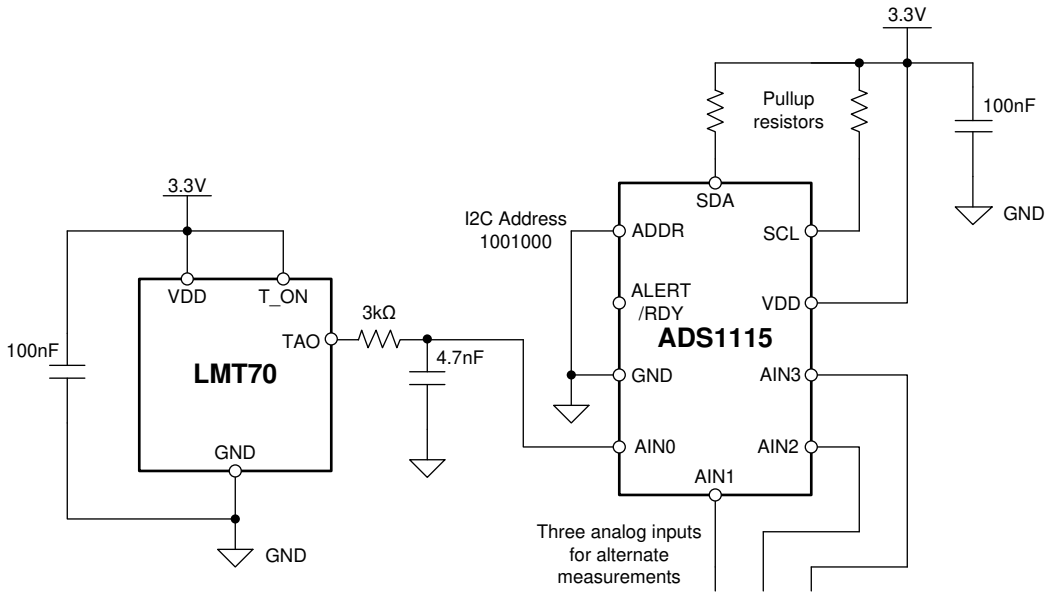
Joseph Wu

Temperature (°C)	LMT70 Output Voltage (mV)	TLA2024 Digital Output
–55	1375.219	55F4h (22004d)
125	302.785	12EDh (4845d)

Power Supplies	
VDD	**GND**
3.3V	0V

Design Description

This circuit design describes a temperature measurement circuit using a precision analog temperature sensor and a 16-bit ADC. The *LMT70* device temperature sensor gives an output voltage dependent on the temperature from –55°C to 150°C, and can be used as a remote measurement when placed away from the ADC. The *ADS1115* ADC is used to measure the output voltage of the LMT70. With the internal voltage reference of the ADC, this circuit makes a compact, low-power solution to accurately measure temperature. Included in this design are ADC register settings to configure the device and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab and field instrumentation*, and *factory automation and control*.



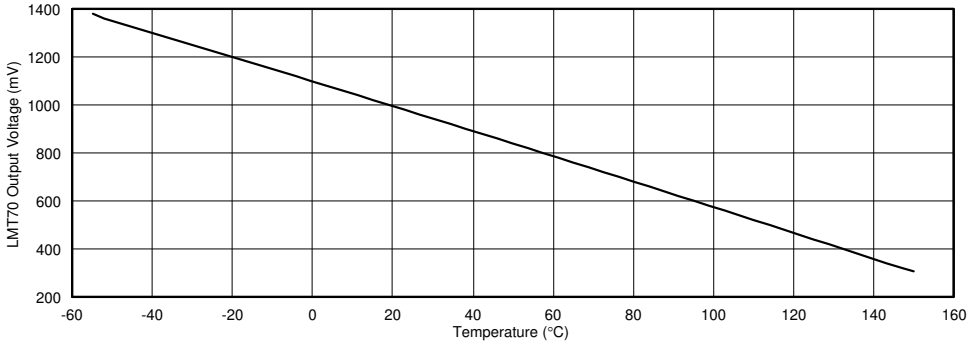
Design Notes

1. Use supply decoupling capacitors for the power supplies. VDD must be decoupled with at least a 0.1-µF capacitor to GND. See the *ADS111x Ultra-Small, Low-Power, I²C-Compatible, 860-SPS, 16-Bit ADCs With Internal Reference, Oscillator, and Programmable Comparator* and *LMT70, LMT70A ±0.05°C Precision Analog Temperature Sensor, RTD and Precision NTC Thermistor IC* data sheets for details on power-supply recommendations.
2. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Because of size, this may not always be practical and X7R capacitors are the next best alternative.
3. Conversion tables and temperature transfer functions for the temperature sensor shown in this application note are also found in the LMT70 data sheet in more detail.
4. While the LMT70 has a recommended operation range of –55°C to 150°C, the ADS1115 has an operating range of –40°C to 125°C. If the full operational range of the LMT70 is needed, the device should be placed remotely from the ADC.
5. This circuit design is shown with the LMT70 connected as a single-ended measurement to AIN0 of the ADS1115, while the remaining three input channels can be used for other measurements. If the temperature sensor is the only sensor measurement, then the ADS1114 can be used and AIN0 is connected to the LMT70 and AIN1 is connected to ground for the same function.
6. If less resolution can be tolerated for the ADC, the ADS1015 or the TLA2024 can be substituted. Both devices are similar to the ADS1115, communicate through I²C, and use similar configuration registers. If SPI communication is required, the ADS1118 or the ADS1018 may be substituted.
7. This application circuit may be used for thermocouple cold-junction measurement. For more information about thermocouple measurements see *A Basic Guide to Thermocouple Measurements*..

Component Selection

1. Identify the range of operation for the temperature sensor.

   The LMT70 has a temperature measurement range of –55°C to 150°C. With this temperature range, the output voltage of the LMT70 varies from 1375mV to 303mV with a negative temperature slope. This range is used to maximize the resolution of the measurement, considering the full-scale range of the ADC. The LMT70 output transfer function is shown in the following figure.



   Despite the appearance, the LMT70 output transfer function is not linear. Accurately determining the temperature requires interpolation from a lookup table or calculation from a polynomial equation.

2. Determine gain and input range of the ADC.

   The ADS1115 has a programmable gain amplifier (PGA) implemented through scaled capacitive sampling, not as a true amplifier. With this PGA, the input range extends to the full supply range, and can be used to set the ADC to one of six different full-scale ranges (FSR).

   As mentioned previously, the LMT70 has an output range of 1375mV to 303mV when the temperature measurement range is –55°C to 150°C. To maximize the resolution, choose the smallest ADC full-scale range that encompasses the temperature measurement range. With this measurement range, the ADC FSR can be set to ±2.048V. At –55°C, the ADC output code would read 55F4h or 22004 in decimal and at 150°C would read 12Edh or 4845 in decimal. Using this setup, the temperature measurement would be 17159 codes. This gives a basic resolution of 0.012°C per code.

   If the temperature measurement range is limited to 15°C as the lowest temperature, then the output voltage of the LMT70 is limited to 1.024V. With this limit, the ADC FSR range can be set to ±1.024V, maximizing the resolution of the ADC.

   The ADS1115 reports data as a differential 16-bit ADC. Even if the ADC is used to make a single-ended measurement, the ADC reports the data as differential. A single-ended measurement is reported with 15-bits of resolution.
3. Select values for the input filtering for the ADC inputs.

   Often, the ADC input is filtered with basic RC filtering. If there is input filtering, the input current of the ADC reacts with any series filter resistance to create an error. For the ADS1115 device, the input current is modeled as equivalent differential and common-mode input impedance. With the negative input grounded, the equivalent input impedance can be approximated as the differential and common-mode impedance in parallel.

   Using the FSR of ±2.048V, the ADS1115 differential input impedance is 4.9MΩ and the common-mode impedance is 6MΩ. The equivalent input impedance is approximately 2.7MΩ. If the series filter resistance is much smaller than the equivalent input impedance, the gain error of the measurement is not impacted from the filtering.

   For delta-sigma type ADCs like the ADS1115, the bandwidth of the input filtering is set to be at least ten times higher than the data rate. If the ADS1115 is run at the highest data rate of 860SPS, then the input filter can be set to higher than 8.6kHz. The LMT70 can drive limited capacitance and its data sheet gives specific guidance for series resistances used with different load capacitance. For a suitable filter, use R_S = 3kΩ and C_{LOAD} = 4.7nF. This sets the input filtering bandwidth to 11.3 kHz. If a different data rate is used, or if the ADS1015 or TLA2024 is used, then this bandwidth can be recalculated for a different data rate. Regardless, follow the guidelines of the capacitive load drive for the LMT70 device as stated in the data sheet.

Configuration Register Settings

The configuration register sets the mode of operation and configuration of the ADC. Configurations include all of the settings described in the previous sections. Nine fields across 16 bits are used to configure the device. Configuration register field descriptions are shown with bit names and positions, read and write usage, and reset values in the following table.

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1h	R/W-0h			R/W-2h			R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE	
R/W-4h			R/W-0h	R/W-0h	R/W-0h	R/W-3h	

The OS bit sets the operational status and starts a single conversion. The MUX[2:0] bits set the input multiplexer to select the analog input. The MODE bit sets the device to single-shot conversion mode. The DR[2:0] bits set the data rate of the device. The remaining fields are used for the ADC comparator settings which are not used in this design. See the *ADS111x Ultra-Small, Low-Power, I²C-Compatible, 860-SPS, 16-Bit ADCs With Internal Reference, Oscillator, and Programmable Comparator* data sheet for more details on the configuration register.

For this application, one ADC channel is used to measure the LMT70. The multiplexer is set to measure AIN0 to GND, the FSR is set to ±2.048V, and the data rate is set to 860SPS. The settings for the configuration register fields in the ADS1115 are shown in the following table.

Bit	Field	Setting	Description
15	OS	1	Start conversion
14:12	MUX[2:0]	100	Single-ended input measurement, AINP–AINN = AIN0–GND, selection of the first channel
11:9	PGA[2:0]	010	FSR = ±2.048V, sets the ADC to be able to measure the full supply range of 0V to VDD
8	MODE	1	Operation in single-shot conversion mode
7:5	DR[2:0]	111	Data rate = 860SPS
4	COMP_MODE	0	Traditional comparator
3	COMP_POL	0	Active low
2	COMP_LAT	0	Non-latching comparator
1:0	COMP_QUE[1:0]	11	Comparator is disabled

Combining these bits from the field descriptions, the configuration register values are 1100 0101 1110 0011 or C5E3h.

Channel Cycling With the ADS1115

The ADS1115 has four analog input channels from a configurable multiplexer connected to the ADC. The LMT70 temperature measurement is made only with the ADS1115 channel connected to AIN0, leaving inputs at AIN1, AIN2, and AIN3 available for alternate measurements.

To cycle through each channel of the system, start each conversion, wait for the conversion to complete, and then read back the data. Then start the conversion for the next channel. Repeating this sequence for all four inputs in the system cycles through all channels. A write to the configuration register starts the conversion and configures the ADC for the proper mode of operation. The communication starts with a write to the I^2C slave address of the device. The I^2C write is followed by three bytes. The first byte is 01h to indicate the configuration register. The next two bytes are the data written to the configuration register. The complete communication of four bytes is shown in the following table.

I^2C Address: 1001000 Write	Address Pointer: Configuration Register	Configuration MSB: Start Conversion, Set Input, FSR, Single-Shot Mode	Configuration LSB: 860SPS, Comparator Disabled
1001 0000	0000 0001	1100 0101	1110 0011

The master then waits for the conversion to complete. For this example, the ADS1115 device is set to the fastest data rate of 860SPS. Because the device uses an internal oscillator, there is some variation in the data rate. To ensure that the device is read after the ADC completes a conversion, the microcontroller waits for the maximum time required for the conversion to complete. This wait time is the nominal data period plus 10% (to compensate for the internal oscillator variation of the device). An additional 20µs is added for the wake up time of the ADC for each single-shot conversion. The total wait time is calculated in the following equation.

$$\text{Wait time} = \text{nominal data period} + 10\% + 20\mu s$$

As an example, if the device is run at 860SPS, the nominal data period is 1.16ms. The necessary wait time would be:

$$\text{Wait time} = (1.16ms \times 1.1) + 20\mu s = 1.30ms$$

A read from the device starts with a write to the register pointer for the conversion data register (00h) and then another read of two bytes from the same I^2C address. The following shows the read of the LMT70 measurement data following the configuration of the ADC. The complete communication of five bytes is shown in the following table.

I^2C Address: 1001000 Write	Address Pointer: Configuration Data Register	I^2C Address: 1001000 Read	Read Conversion Data MSB	Read Conversion Data LSB
1001 0000	0000 0000	1001 0001	xxxx xxxx	xxxx xxxx

Other ADS1115 channels can be cycled in any order through by repeating this sequence. Data is collected by setting the configuration register, waiting for the conversion to complete, and then reading the conversion data.

Measurement Conversion

Conversions for the output voltage of the temperature sensor are relatively straightforward based on the full-scale range of the ADC. The output voltage of the LMT70 device is calculated with the following:

$$\text{Output Code} = 2^{15} \times [V_{AIN0} / (2.048V)]$$

$$\text{LMT70 Output Voltage} = V_{AIN0} = (\text{Output Code}) \times (2.048) / (2^{15})$$

An electrical characteristics temperature lookup table follows. The voltage measurement can be converted to temperature by using interpolation with the following lookup table.

Temperature (°C)	VTAO (mV) (typical value)	Local Slope (mV/°C)
–55	1375.219	–4.958
–50	1350.441	–4.976
–40	1300.593	–5.002
–30	1250.398	–5.036
–20	1199.884	–5.066
–10	1149.070	–5.108
0	1097.987	–5.121
10	1046.647	–5.134
20	995.050	–5.171
30	943.227	–5.194
40	891.178	–5.217
50	838.882	–5.241
60	786.360	–5.264
70	733.608	–5.285
80	680.654	–5.306
90	627.490	–5.327
100	574.117	–5.347
110	520.551	–5.368
120	466.760	–5.391
130	412.739	–5.430
140	358.164	–5.498
150	302.785	–5.538

As an alternative, the output voltage of the LMT70 can be modeled with a second order transfer function. Using the least squares sum method, a best fit second order transfer function is generated using the values in the previous table. A limited temperature range of –10°C to 110°C can be used to generate an accurate transfer function with one set of coefficients. Over the full temperature range of –55°C to +150°C, a single second order transfer function has increased error at the temperature extremes and requires a different set of coefficients. The transfer function is shown in the following equation:

$$T_M = a \times (VTAO)^2 + b \times (VTAO) + c$$

where:

Coefficient	Best fit for –55°C to 150°C	Best fit for –10°C to 110°C
a	–8.451576E-06	–7.857923E-06
b	–1.769281E-01	–1.777501E-01
c	2.043937E+02	2.046398E+02

and VTAO is in mV and T_M is in °C. For an in-depth discussion of conversion methods, consult the LMT70 data sheet.

Pseudo Code Example

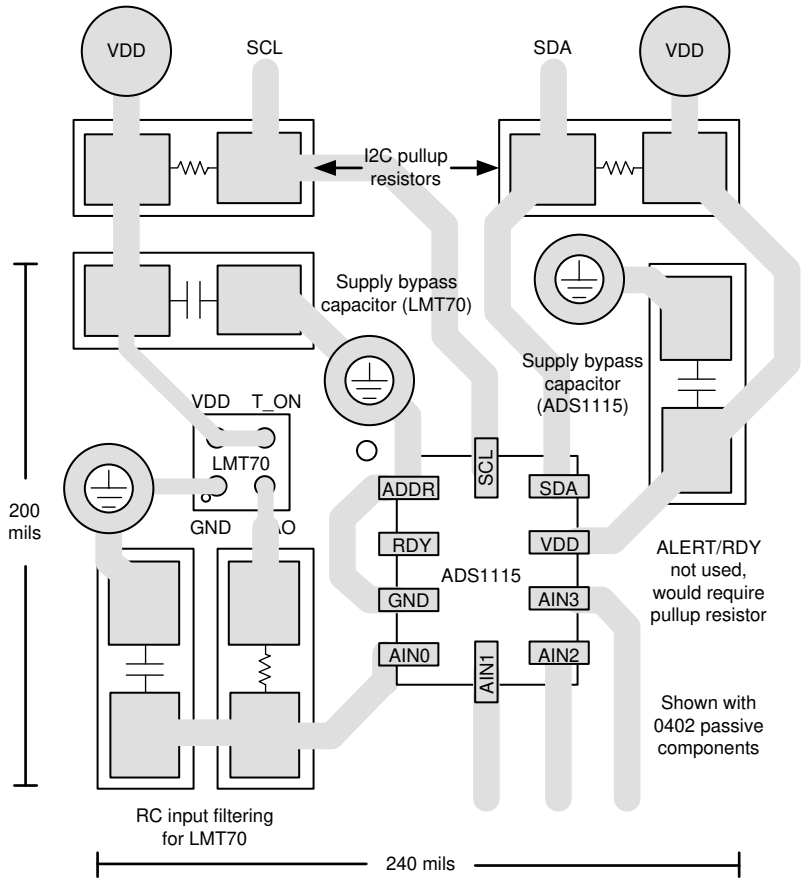
The following example shows a pseudocode sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS1115 in single-shot conversion mode. The ADC first read is for the LMT70 temperature sensor, using the AIN0 channel. Data is taken by using the maximum data period, allowing for time to wake up the device, configure the ADC, take a single conversion, and set up other ADC measurements. Other measurement channels are similarly used with a write to the configuration register and start of a conversion, wait for the conversion to complete, and a read back of the conversion.

```
Configure microcontroller for I2C communication, I2C address=1001000 (48h)
Loop
{
Send 90h 01h C5h E3h //
// Start write to address 48h, write bit 0 (90h)
// Configuration register 01h
// Set C1E3h, AIN0-GND, FSR=±2.048V, Single-shot conversion, DR=860SPS, stop
Wait 1.30ms // Wait for data period, +10% for internal oscillator variation, +20us
Send 90h 00h 91h xxh xxh // Read back ADC conversion data
// Start write to address 48h, write bit 0 (90h)
// Conversion register 00h, stop
// Start read from address 48h, read bit 1 (91h)
// Read back 2 bytes, stop
// Measurements from AIN1, AIN2, and AIN3 (optional)
 Send configuration for channel 1
Wait for conversion to complete
Read channel 1
Send configuration for channel 2
Wait for conversion to complete
Read channel 2
Send configuration for channel 3
Wait for conversion to complete
Read channel 3
}
```

For more details on the configuration of the ADS1115, see the data sheet or the *Precision measurement circuit with 16 singled-ended channels and I^2C interface circuit*.

Layout Example

The following shows an example layout with the LMT70 and ADS1115 devices. RC input filtering is added using 0402 resistors and capacitors. The resulting layout is about 200 mils by 240 mils. This measurement does not include the I^2C pullup resistors. A single set of these resistors are required for each system.



Example Layout

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS1115	ADS111x ultra-small, low-power, I^2C-compatible, 860-SPS, 16-bit ADCs with internal reference, oscillator, and programmable comparator	http://www.ti.com/product/ADS1115	Link to similar devices Link to similar SPI devices
LMT70	LMT70, LMT70A ±0.05°C Precision Analog Temperature Sensor, RTD and Precision NTC Thermistor IC	http://www.ti.com/product/LMT70	

Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

For direct support from TI Engineers use the TI E2E community:

TI e2e.ti.com

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

Analog Engineer's Circuit

Ultra-Small, Low-Cost Analog Temperature Sensor Measurement Circuit With ADC

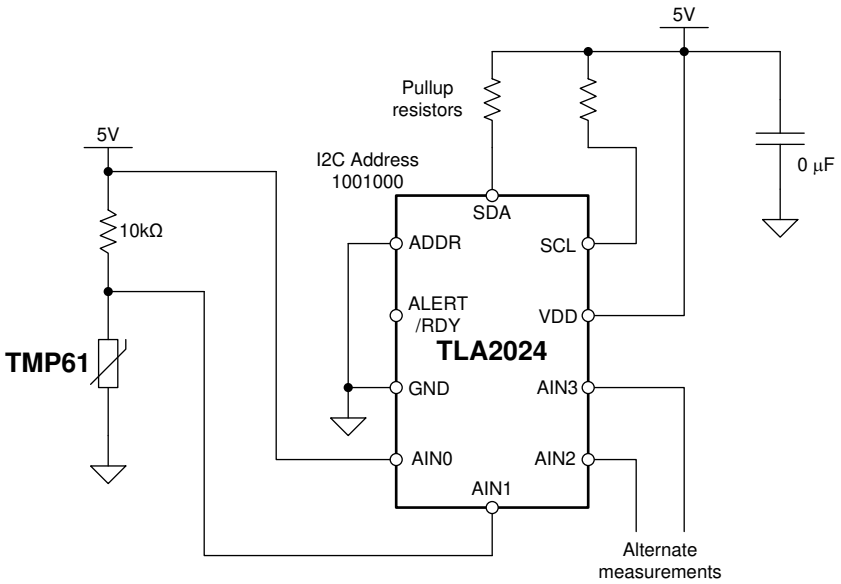
Joseph Wu

Temperature (°C)	Resistor Voltage (mV)	TLA2024 Digital Output Code	TMP61 Voltage (mV)	TLA2024 Digital Output Code
–40	3012.5	3E1h	1987.5	5E2h
125	1781.1	649h	3218.9	37Ah

Power Supplies	
VDD	GND
5V	0V

Design Description

This circuit design describes a temperature measurement circuit using a linear thermistor and a 12-bit ADC. The *TMP61* linear thermistor resistance changes depending on the temperature from –40°C to 125°C, and can be used as a remote measurement when placed away from the ADC. The *TLA2024* ADC is used to measure the voltage across a TMP61 and a precision resistor. With the internal voltage reference of the ADC, this circuit makes a compact, low-cost, and low-power solution to measure temperature. Included in this design are ADC register settings to configure the device and pseudo code is provided to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab and field instrumentation*, and *factory automation and control*.



Design Notes

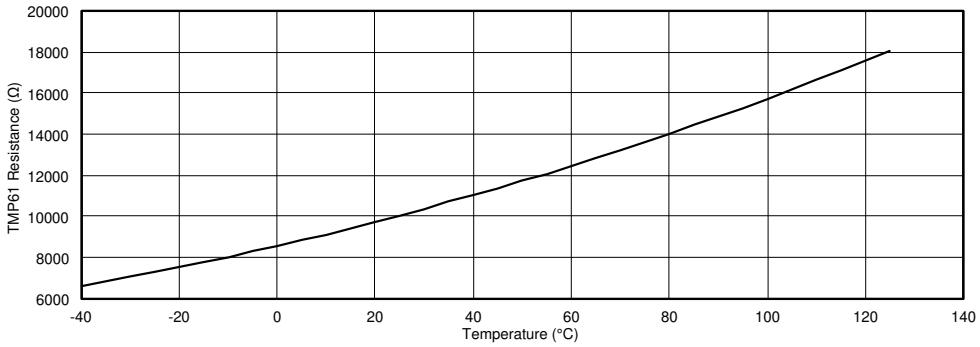
1. Use supply decoupling capacitors for the supply. The TLA2024 VDD must be decoupled with at least a 0.1-µF capacitor to GND. See the *TLA202x Cost-Optimized, Ultra-Small, 12-Bit, System-Monitoring ADCs Data Sheet* for details on power supply recommendations.
2. Polynomial equations or a lookup table can be used to convert the TMP61 resistance to temperature. For details, download the *Thermistor Design Tool*.
3. Temperature measurement with the TMP61 only uses two of the four analog inputs (AIN0 and AIN1) on the TLA2024. The remaining two analog inputs can be used for another differential measurement or two single-ended measurements.
4. The TLA2024 can be used to measure supply voltage with an extra measurement cycle, but not an extra analog input. AIN0 is already connected to the 5-V supply and can be measured as a single-ended setting for the multiplexer using the ±6.144V FSR setting.
5. If more resolution is needed for the ADC measurement, the ADS1115 can be substituted. The ADS1115 is similar to the TLA2024, it communicates through I^2C, and uses similar configuration registers. If SPI communication is required, the ADS1018 may be substituted.
6. For more information about the TI silicon-based linear thermistors and applications, see *TI's linear thermistors overview* and *Temperature Sensing with Thermistors*.

Component Selection

1. Identify the range of operation for the temperature sensor.

   The TMP61 has a temperature measurement range of –40°C to 125°C. With this range, the resistance of the TMP61 varies from 6537Ω to 17853Ω with a positive temperature slope. This range is used to maximize the resolution of the measurement, considering the full-scale range of the ADC.

   The following image shows the TMP61 resistance transfer function.

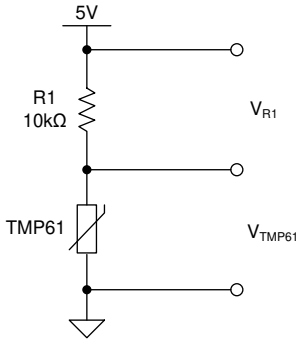


   While this transfer function is not completely linear, it is more linear that standard PTC thermistors. As mentioned previously, a lookup table or polynomial equation is required to determine the temperature based on the resistance.

   For more information about thermistor temperature conversion for the TMP61, download the *Thermistor Design Tool*. The tool contains resistance tables, example temperature conversion methods, and code examples.

2. Determine a precision resistor value for a voltage divider with the TMP61.

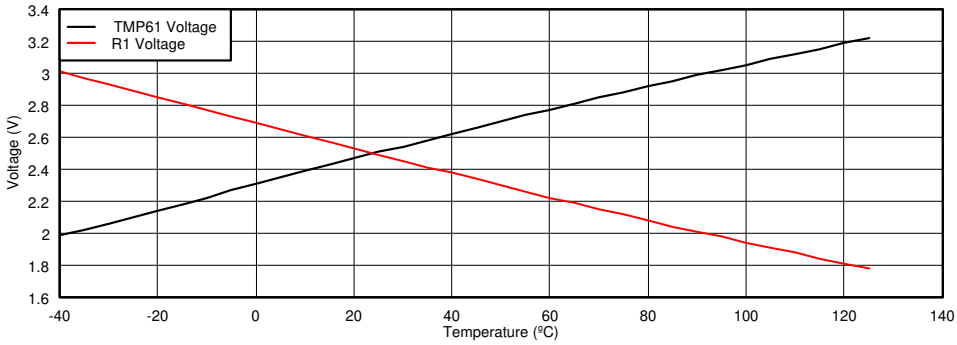
   To set up the measurement, a voltage divider is created from the TMP61 and a precision resistor (R1) using the supply.



   First, the ADC measures the voltage across R1 using one channel of the multiplexer of the TLA2024. This measurement of a known resistance is the first of two measurements to determine the resistance of the TMP61. Then, the ADC measures the voltage across the TMP61 with a second channel. These two measurements yield two output ADC codes.

   With the known resistance of R1, the resistance of the TMP61 can be calculated from the ratio of the output codes from the two ADC measurements. Because R1 acts as a reference of comparison for the resistance of the thermistor, this resistor must be accurate. Any error in the resistance reflects as an error in the measurement of the TMP61 resistance.

   The reference resistor value of R1 is chosen as 10kΩ for convenience. The room temperature resistance of the TMP61 at 25°C is roughly also 10kΩ. At this temperature, the thermistor is near the midpoint of the temperature range. If the 25°C is the midpoint, both the resistor measurement and TMP61 with be of similar voltage magnitude through the temperature range. The voltage across R1 and the TMP61 are shown against temperature in the following figure.



   Voltages of R1 and the TMP61 vary from approximately 1.8V to 3.2V. Even as the R1 varies in voltage, the resistance is known to be a constant 10kΩ. The measurement of this voltage is compared to the measurement of the TMP61 voltage to calculate the ratio between the resistances.

3. Determine the gain and input range of the ADC.

   The TLA2024 has a programmable gain amplifier (PGA) implemented through scaled capacitive sampling, not as a true amplifier. With this PGA, the input range extends to the full supply range, and can be used to set the ADC to one of six different full-scale ranges (FSR). To maximize the resolution, choose the smallest ADC full-scale range that encompasses the temperature measurement range.

   Based on the temperature range from –40°C to 125°C you can determine the voltages across the two resistive elements. The first measurement of the voltage across the 10-kΩ resistor varies from 3012.5mV to 1781.1mV. The second measurement of the TMP61 voltage varies conversely from 1987.5mV to 3218.9mV. With these voltage ranges, the ±4.096V FSR can be used to measure both the resistor and the TMP61. Because both use the same ADC and FSR, the gain error difference between the measurements is very small. Using this setup, the temperature measurement range covers 616 codes for both R1 and the TMP61. This gives a basic resolution of approximately 0.27°C per code.

   Because the resistors have the same current, the ADC output codes are proportional to the resistances. The output voltage does not need to be calculated and the resistance of the TMP61 can be calculated based on the ratio of the ADC codes for both measurements.

   The TLA2024 reports data as a differential 16-bit ADC. Even if the ADC is used to make a single-ended measurement, the ADC reports the data as differential. A single-ended measurement is reported with 15-bits of resolution.

Configuration Register Settings

The configuration register sets the mode of operation and configuration of the ADC. Configurations include all of the settings described in the previous sections. Six fields across 16 bits are used to configure the device. Configuration register field descriptions are shown with bit names and positions, read and write usage, and reset values in the following table.

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1h	R/W-0h			R/W-2h			R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DR[2:0]			RESERVED				
R/W-4h			Always write 03h				

The OS bit sets the operational status and starts a single conversion. The MUX[2:0] bits set the input multiplexer to select the analog input. The MODE bit sets the device to single-shot conversion mode. The DR[2:0] bits set the data rate of the device. See the *TLA202x Cost-Optimized, Ultra-Small, 12-Bit, System-Monitoring ADCs data sheet* for details on the configuration register.

For this application, the ADC is first set to measure the voltage across R1, using the multiplexer to measure from AIN0 to AIN1. The FSR is set to ±4.096V, with a data rate of 1600SPS. The settings for the configuration register fields in the TLA2024 are shown in the following table.

Bit	Field	Setting	Description
15	OS	1	Start conversion
14:12	MUX[2:0]	000 101	Single-ended input measurement, AINP – AINN = AIN0 – AIN1, first measurement of R1 Differential input measurement, AINP – AINN = AIN1 – GND, second measurement of TMP61
11:9	PGA[2:0]	001	FSR = ±4.096V, sets the ADC to be able to measure the full supply range of 0V to VDD
8	MODE	1	Operation in single-shot conversion mode
7:5	DR[2:0]	100	Data rate = 1600SPS
4:0	Reserved	00011	Always write 03h

Combining these bits from the field descriptions, the configuration register values are 1000 0011 1000 0011 or 8383h. This configures the first measurement of the R1 resistor.

In the second measurement, the multiplexer is then set to measure the voltage across the TMP61. For this measurement, the only change is to set the input to measure from AIN1 to GND as a single-ended measurement. The configuration register is set to 1101 0011 1000 0011 or D383h.

Channel Cycling For The TLA2024

The TLA2024 has four analog input channels from a configurable multiplexer connected to the ADC. Making the temperature measurement requires measurements only from AIN0 and AIN1 of the TLA2024 (one differential measurement and one single-ended measurement). However, the last two channels can also be included to cycle through all measurements.

To make these measurements, The ADC is programmed to cycle through the system, start each conversion, wait for the conversion to complete, and then read back the data. Then start the conversion for the next channel. Repeat each measurement for the four single-ended input channels, before moving on to the next channel.

Repeating this sequence in the system cycles through all channels. A write to the configuration register starts the conversion and configures the ADC for the proper mode of operation. The communication starts with a write to the I^2C slave address of the device. The I^2C write is followed by three bytes. The first byte is 01h to indicate the configuration register. The next two bytes are the data written to the configuration register. The complete communication of four bytes to setup the R1 resistor measurement is shown in the following table.

I²C Address: 1001000 Write	Address Pointer: Configuration Register	Configuration MSB: Start Conversion, Set Input, FSR, Single-Shot Mode	Configuration LSB: 128SPS, Comparator Disabled
1001 0000	0000 0001	1000 0011	1000 0011

The master then waits for the conversion to complete. For this example, the TLA2024 device is set to the default data rate of 1600SPS. Because the device uses an internal oscillator, there is some variation in the data rate. To ensure that the device is read after the ADC completes a conversion, the microcontroller waits for the maximum time required for the conversion to complete. This wait time is the nominal data period plus 10% (to compensate for the internal oscillator variation of the device). An additional 20µs is added for the wake up time of the ADC for each single-shot conversion. The total wait time is calculated in the following equation.

Wait time = nominal data period + 10% + 20µs

As an example, if the device is run at 1600SPS, the nominal data period is 625µs. The necessary wait time would be:

Wait time = (625µs × 1.1) + 20µs = 708µs

A read from the device starts with a write to the register pointer for the conversion register (00h) and then another read of two bytes from the same I²C address. The following shows the read of the R1 resistor measurement data following the first configuration of the ADC. The complete communication of five bytes is shown in the following table.

I²C Address: 1001000 Write	Address Pointer: Conversion Data Register	I²C Address: 1001000 Read	Read Conversion Data MSB	Read Conversion Data LSB
1001 0000	0000 0000	1001 0001	xxxx xxxx	xxxx xxxx

After collecting the data for R1, the TLA2024 is configured to measure the voltage across the TMP61. The communication of four bytes to setup the TMP61 measurement is shown in the following table.

I²C Address: 1001000 Write	Address Pointer: Configuration Register	Configuration MSB: Start Conversion, Set Input, FSR, Single-Shot Mode	Configuration LSB: 128SPS, Comparator Disabled
1001 0000	0000 0001	1101 0011	1000 0011

After waiting for the ADC to complete to the conversion, the same previous five byte read of the conversion data register is used to retrieve the data as shown in the previous table. The other remaining TLA2024 channels can be cycled in any order through by repeating this sequence.

Measurement Conversion

As mentioned previously, the ADC data does not need to be converted to voltage. The ratio of the ADC output codes is equivalent to the ratio of the R1 and TMP61 resistances. With OutputCode1 from the R1 measurement and OutputCode2 as the TMP61 measurement, the TMP61 resistance can be calculated from the following equation:

TMP61 resistance = 10kΩ × (OutputCode2 / OutputCode1)

Note that for the TLA2024, the data format is 12 bits with four bits zero padded on the right. A full-scale reading is 7FFh and would be read from the conversion register as 7FF0h.

Download the *Thermistor Design Tool* to make the TMP61 conversion from resistance to temperature. With the tool, the conversion can be made from calculation from a lookup table, a fourth order polynomial, or a Steinhart-Hart equation.

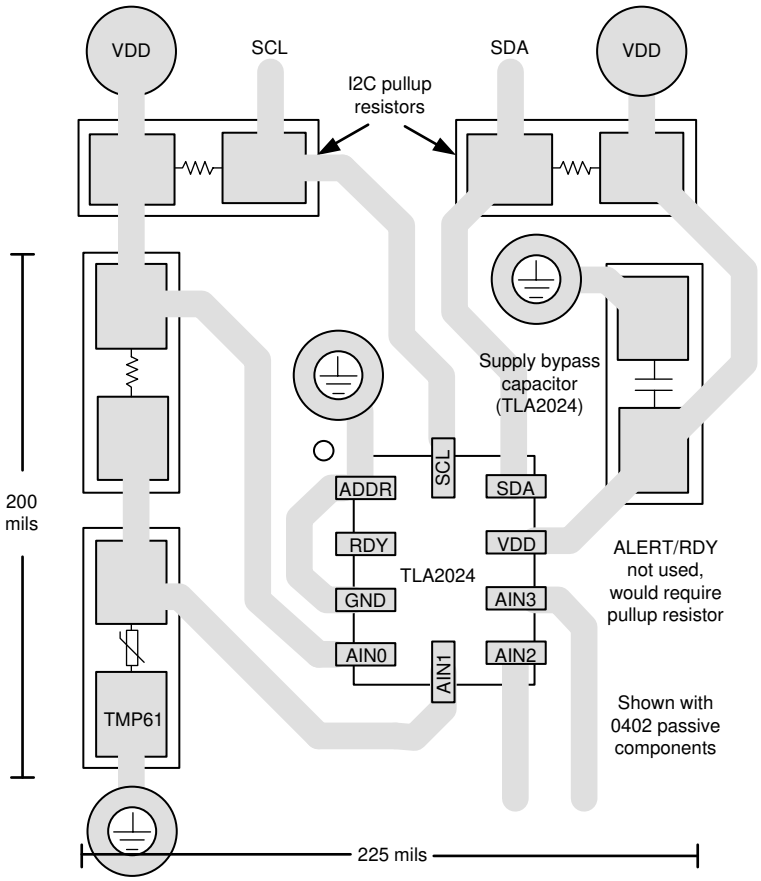
Pseudo Code Example

The following example shows a pseudocode sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the TLA2024 in single-shot conversion mode. The ADC first read is for the reference resistor R1, using a differential measurement of AIN0 and AIN1. Data is taken by using the maximum data period, allowing for time to wake up the device, configure the ADC, take a single conversion, and set up other ADC measurements. A second measurement is then made with a single-ended measurement AIN1 for the TMP61 with a similar method. Other measurement channels are similarly used with a write to the configuration register and start of a conversion, wait for the conversion to complete, and a read back of the conversion.

```
Configure microcontroller for I2C communication, I2C address=1001000 (48h)
Loop
{
Send 90h 01h 83h 83h // Measure R1 voltage as Data1
// Start write to address 48h, write bit 0 (90h)
// Configuration register 01h
// Set 8383h, AIN0-AIN1, FSR=±4.096V, Single-shot conversion, DR=1600SPS, stop
Wait 708us // Wait for data period, +10% for internal oscillator variation, +20us
Send 90h 00h 91h xxh xxh // Read back ADC conversion data
// Start write to address 48h, write bit 0 (90h)
// Conversion register 00h, stop
// Start read from address 48h, read bit 1 (91h)
// Read back 2 bytes, stop
Send 90h 01h 83h 83h // Measure TMP61 voltage as Data2
// Start write to address 48h, write bit 0 (90h)
// Configuration register 01h
// Set D383h, AIN1-GND, FSR=±4.096V, Single-shot conversion, DR=1600SPS, stop
Wait 708us // Wait for data period, +10% for internal oscillator variation, +20us
Send 90h 00h 91h xxh xxh // Read back ADC conversion data
// Start write to address 48h, write bit 0 (90h)
// Conversion register 00h, stop
// Start read from address 48h, read bit 1 (91h)
// Read back 2 bytes, stop
// Calculate resistance of TMP61 as R_TMP61
Calculate R_TMP61 from 10kOhms*Data2/Data1
// Convert R_TMP61 to temperature with example code from the Thermistor Design Tool
// Measurements from AIN2 and AIN3 (optional)
Send configuration for channel 2
Wait for conversion to complete
Read channel 2
Send configuration for channel 3
Wait for conversion to complete
Read channel 3
}
```

Layout Example

The following shows an example layout of the TLA2024 device with the TMP61. Bypass capacitance is placed for the ADC using an 0402 capacitor. The resulting layout is about 200 mils by 225 mils. This measurement does not include the I^2C pullup resistors.



Example Layout

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
TLA2024	TLA202x Cost-Optimized, Ultra-Small, 12-Bit, System-Monitoring ADCs	http://www.ti.com/product/TLA2024	Link to similar devices Link to similar SPI devices
TMP61	TMP61 ±1% 10-kΩ Linear Thermistor With 0402 and 0603 Package Options	http://www.ti.com/product/TMP61	

Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, *Thermistor Design Tool*
- Texas Instruments, *Temperature Sensing with Thermistors*

For direct support from TI Engineers use the E2E community:

TI e2e.ti.com

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

Analog Engineer's Circuit

Active-Filtering Circuit for Audio DACs

Paul Frost

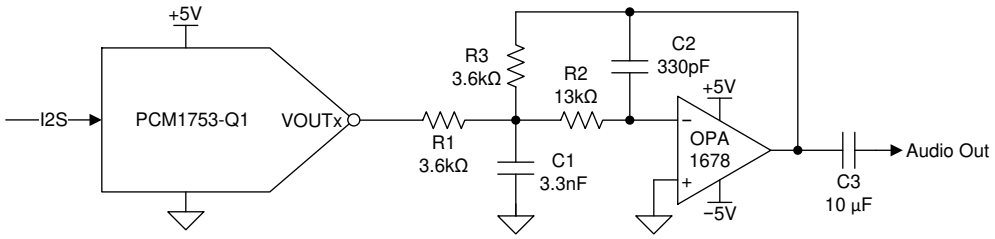
Design Goals

Filter Characteristics

Filter Input	Cutoff Frequency	Filter Gain
$4V_{PP}$, $1.42V_{RMS}$	–3dB at 23kHz	–1V/V, 0dB

Design Description

This circuit shows the implementation of a second-order active-filter for audio digital-to-analog converter (DAC) applications. In applications such as automotive head units, home theater soundbars, and AV receivers, it is critical to minimum undesirable noise in the audible range, approximately 20Hz to 22kHz. For this reason, many delta-sigma type audio DACs implement noise shaping techniques that force the noise generated by the over-sampling functionality of the DAC outputs side of the audible range, this is process is called 'noise-shaping,' while the actual noise is called 'out-of-band noise.' Many common audio DACs, such as the PCM1753-Q1, have noise-shaping that forces the out-of-band noise to approximately 50% the sampling rate, f_S, of the digital source. While this noise is not generally considered audible, it can have detrimental effects on the amplifier circuits that are found on the output of audio DACs. For example, this out-of-band noise may be aliased by class-D amplifiers that operate at higher frequencies back into the audible range. In addition, this noise would also experience the same analog gain of the output amplifiers if no filtering is implemented. The second-order active-filter design allows a higher level of noise attenuation closer to the audible band than a simple, first-order RC filter. In addition, it allows the audio output of the system to have a lower impedance and current drive than the audio DAC can provide due to the output drive capabilities of the op amp featured in the filter.



Design Notes

1. It is important to note that the f_C of the design is optimized for a sample rate of at least 44.1kHz, which is common in audio systems. The f_C should be approximate 50% of the sample rate, to attenuate the out-of-band noise from the delta-sigma modulator. If a higher frequency sample rate is used, move the cutoff frequency further out in the frequency domain to allow a wider bandwidth from the audio DAC.
2. Not all audio DACs require a second-order active filter. Some audio DACs feature different noise-shaping architectures that moves the out-of-band noise further away from the audible range, meaning that a simple RC filter may be enough to attenuate the unwanted noise.
3. Most audio system feature a DC blocking capacitor to allow the audio output to be ground centered. In this design, put the blocking capacitor directly on the output of the DAC, but as the amplifier will also have some small offset, the capacitor is generally placed directly on the output of the filter or the input of the amplifier or headphone driver that would proceed the active filter.

Design Steps

1. Select a DAC based on the needs of the application. Consider the required signal-to-noise ratio (SNR), total harmonic distortion and noise (THD+N), and supported I2S interface sample rates. While most audio DACs support rates ranging from 16kHz to 192kHz, not all support rates like 384kHz or 768kHz. Higher rates result in noise shaping that moves the out-of-band noise further from the audible range, but not all audio sources can provide them.
2. The amplifier selected for the design (OPA1678) is a CMOS input amplifier. CMOS input amplifiers have lower current noise at the inputs of the amplifier at lower frequencies than JFET type amplifiers. The current-noise translates to voltage-noise on the output as the filter features input large resistance values, so it is important to select an amplifier with low current-noise.
3. Select the resistor and capacitor values for the filter to have a –3dB point at approximately 23kHz. The f_C of the circuit can be calculated using the following equation:

$$f_C = \frac{1}{2\pi\sqrt{R2 \cdot R3 \cdot C1 \cdot C2}}$$

4. The capacitors used for the filter must be COG/NP0 type ceramics. COG/NP0 type capacitors have a lower voltage coefficient of capacitance, meaning that the capacitive value of the component is less impacted by the voltage bias across the device. As the capacitors are key for performance of the filter, other types of ceramic capacitors should be avoided in the signal path.
5. Thin-film resistors are recommended for the resistive elements in the filter. All resistors feature voltage noise, which is well understood to be dependent on resistance and temperature, as shown in the first equation following. But resistors also have a current noise, which is dependent on the voltage across the resistor, frequency, and a constant, *C*, that is dependent on the material of which the resistor is composed, as shown in the second equation that follows.

$$S_T = 4kRT$$

where

- k is Boltzmann's constant
- R is resistance
- T is temperature

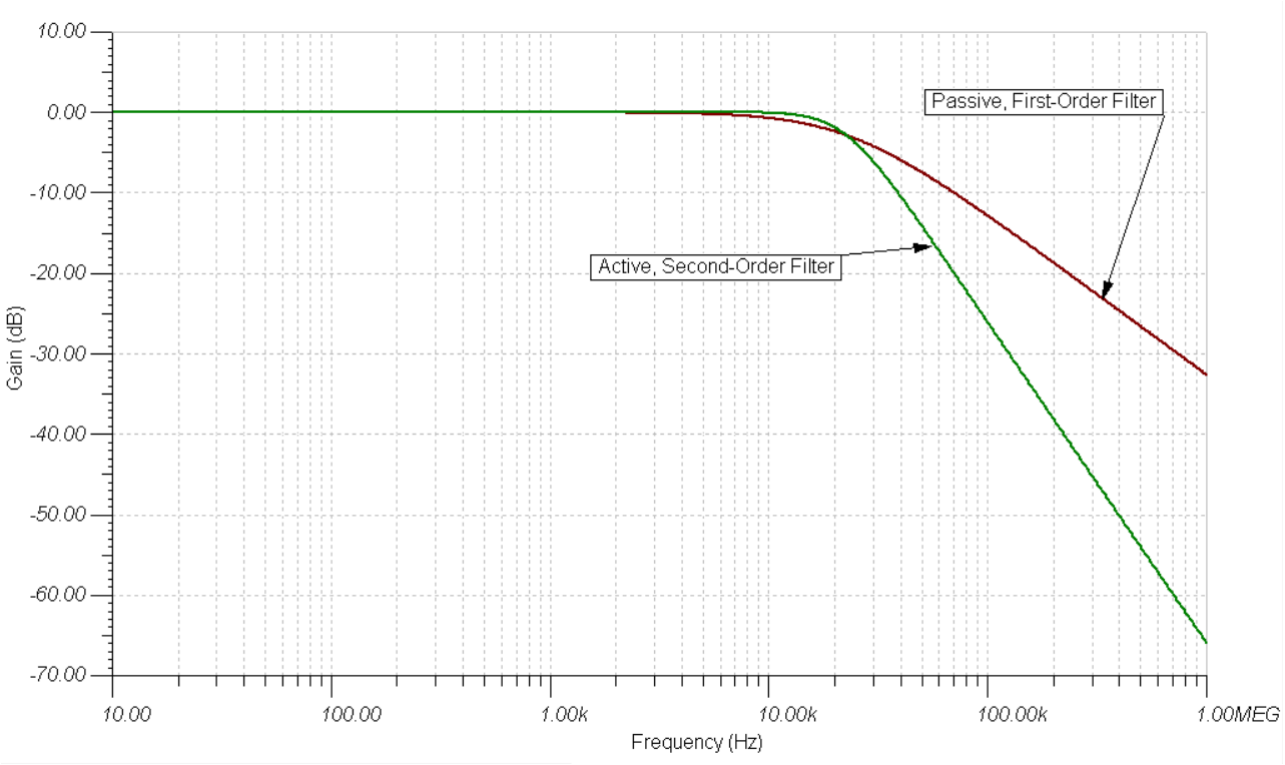
$$S_E = (C \times U^2) \div f$$

where

- C is a constant derived from the resistor material
- U is the differential voltage across the resistor
- f is the frequency

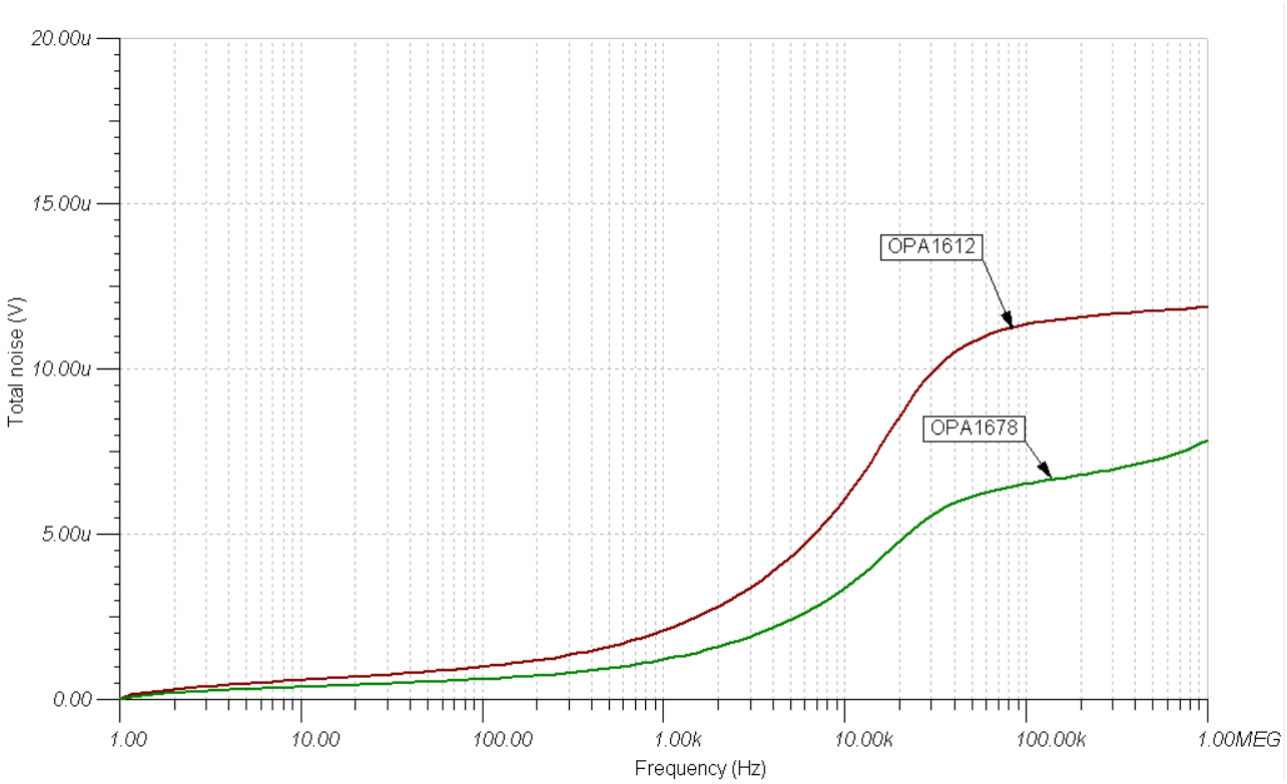
Simulated Filter Response

The following graph shows the simulated filter response of the second-order active filter as well as the response of a simple, first order RC filter with approximately the same fC. Note that the filter roll-off for the first order filter is –20dB/decade, while the roll-off for the active filter is –40dB/decade.



Simulated Noise Performance

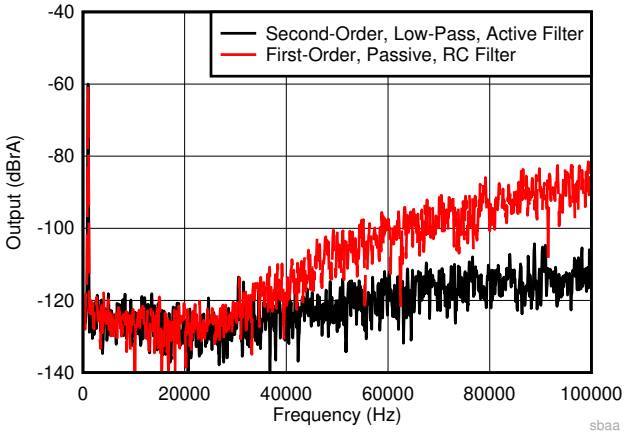
The following graph shows the simulated total noise contribution of the circuit, with the exception of the DAC. The was simulated using the OPA1678, which is specified as having 4.5nV/√ Hz at 1kHz, and the OPA1612, which is specified as having 1.1nV/√ Hz at 1kHz. The results show that the contribution of the current noise in the system result in a greater total noise in the OPA1612 versus the OPA1678, even though the OPA1612 has lower voltage noise.



Measured Output Spectrum

The output of the DAC was measured in the frequency domain with the second-order, active-filter as well as the first-order RC filter. The output of the DAC was set to –60dB full-scale amplitude at 1kHz frequency with a sample rate of 48kHz.

The graph shows that the out-of-band noise begins to increase at around 24kHz, which is expected given the noise-shaping of the PCM1753-Q1. The second-order filter has approximately a 20dB lower output at 100kHz when compared to the RC filter.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
PCM1753-Q1, PCM1754-Q1 (1)	24-bit resolution, 106dB typical SNR, 0.002% typical THD+N, single-ended, voltage-output, audio DAC	Automotive 106-dB SNR stereo digital-to-analog converter (DAC) (software control)	Audio DACs
OPA1678	Low distortion, low noise, low input current, dual amplifier for audio applications	Single Channel 450nA Precision Nanopower Operational Amplifier	Audio Op-Amps Overview

(1) The PCM1753 and PCM1754 are similar parts, only differentiated by being SPI controlled versus HW controlled.

Design References

Texas Instruments, SBAM410 circuit source files, software

Other Links:

Texas Instruments, Precision DAC Learning Center, portfolio overview

Texas Instruments, *Designing a Premium Audio System*, video

Texas Instruments, Audio DACs, portfolio overview

Trademarks

All trademarks are the property of their respective owners.

Auxiliary Circuits for High-Performance Audio

Paul Frost

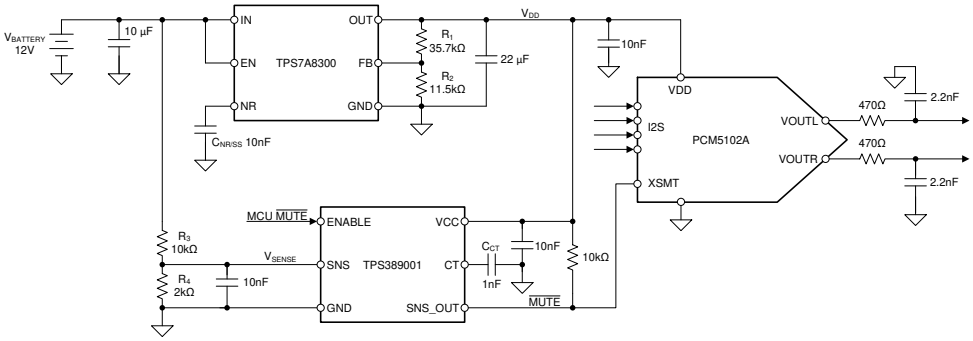
Design Goals

LDO Input Voltage	LDO Output Voltage	Voltage Supervisor Mute Threshold(1)
12V	3.3V	7V

(1) If the $V_{BATTERY}$ voltage is below this threshold, MUTE should be asserted.

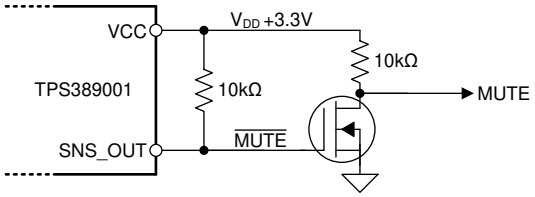
Design Description

Power conditioning is a critical aspect in audio applications. Circuits commonly found in automotive head units and premium aftermarket automotive audio systems will implement a hardware level mute that verifies that the audio digital-to-analog converters (DACs) and amplifiers are muted as supplies are established. The supplies will also need some conditioning to reduce noise coupled into the audio DAC. This circuit shows a low-noise, low-dropout (LDO) voltage regulator used to generate the +3.3-V supply for an audio DAC. An added benefit of an LDO is that there is a wider input voltage range at which the LDO can maintain the supply voltage. A voltage supervisor is used to notify the DAC when the source of the LDO begins to collapse, so the audio DAC can soft-mute the output before its supply is removed. This will reduce unwanted clicking or pops during shutdown and startup.



Design Notes

1. In this circuit the DAC mutes the output when soft-mute pin (XSMT) is held low, but not all DACs feature active-low mute inputs. Some devices feature enable signals for other devices such as mute switches and amplifiers require MUTE to be active high. In those cases, a simple N-channel MOSFET can be added to the output to invert the signal.



2. During power-up events, the capacitor on the CT pin (C_{CT}) of the supervisor allows additional delay from when the SNS pin value rises above the threshold voltage and when the SNS_OUT goes high. This can be used to the delay the deactivation of the $\overline{\text{MUTE}}$ output for the LDO to establish its voltage (as it must charge the output capacitors). In addition, this can be useful if there are other devices that need time to initialize

before the DAC comes out of mute. The additional propagation delay can be calculated using the following equation:

$$t_{PD} = C_{CT} \times 1.07s + 25\mu s$$

3. Brown-out events occur when the supplies of a device are partially reduced, but not low enough to issue a full power-on reset (POR) within the device. For this reason, it is recommended to confirm a full reset occurs during these events. The supervisor circuit accomplishes this as the XSMT acts as a reset circuit for the audio DAC.
4. Most audio DACs operate in either a VCOM or VREF architecture. The VCOM architecture uses a simple voltage divider from the supply to create the output amplitude reference. This is beneficial as it ensures that there will not be output clipping from the DAC if the supply is not the nominal value, as the output scales with the input voltage. The drawback of this architecture is the limited power-supply rejection ratio (PSRR) for the power supply noise. While a capacitor on the VCOM pin of the audio DAC will provide some filtering, it may still impact the output.

   In a VREF configuration, an internal reference is generated by the audio DAC. This will result in better PSRR performance for the system. The drawback of this design is that if the supply voltage does drop, the output could clip.

Design Steps

1. Select an LDO regulator for its current output capability, voltage-input range, and output noise. At minimum, the LDO sourcing the audio DAC must be able to supply the required current of the DAC. In addition, if there are other devices on the same bus, such as amplifiers, then the quiescent current of those devices must be taken into account. The LDO input voltage range must accommodate the main supply source, which, in this circuit, is assumed to be a 12-V battery.
2. The feedback (FB) voltage must be calculated to provide the correct output voltage. In this circuit, the resistors R_1 and R_2 can be calculated as the following shows.

   $$R_1 \quad R_2\left(\frac{V_{DD}}{V_{REF}} - 1\right)$$

   Given the design goal of +3.3V for V_{DD}, and the V_{REF} for this LDO is approximately 0.8V, use a R_1 of 35.7kΩ and R_2 of 11.5kΩ. In addition, note that the FB node has a current requirement and it is recommended that the following equation is used for guidance when selecting R2.

   $$\frac{V_{REF}}{R_2} > 5\mu A$$

3. Select the voltage supervisor for the features desired in the system. In this circuit, the selected supervisor has an enable input pin. This feature allows a user (or microcontroller) mute signal to be used to override the supervisor output. In addition, some supervisors allow multiple supply rails to be monitored, which is useful for the output amplifiers.
4. The sense voltage is calculated using the following equation.

   $$V_{SENSE} \quad V_{BATTERY} \times \frac{R_4}{R_3 + R_4}$$

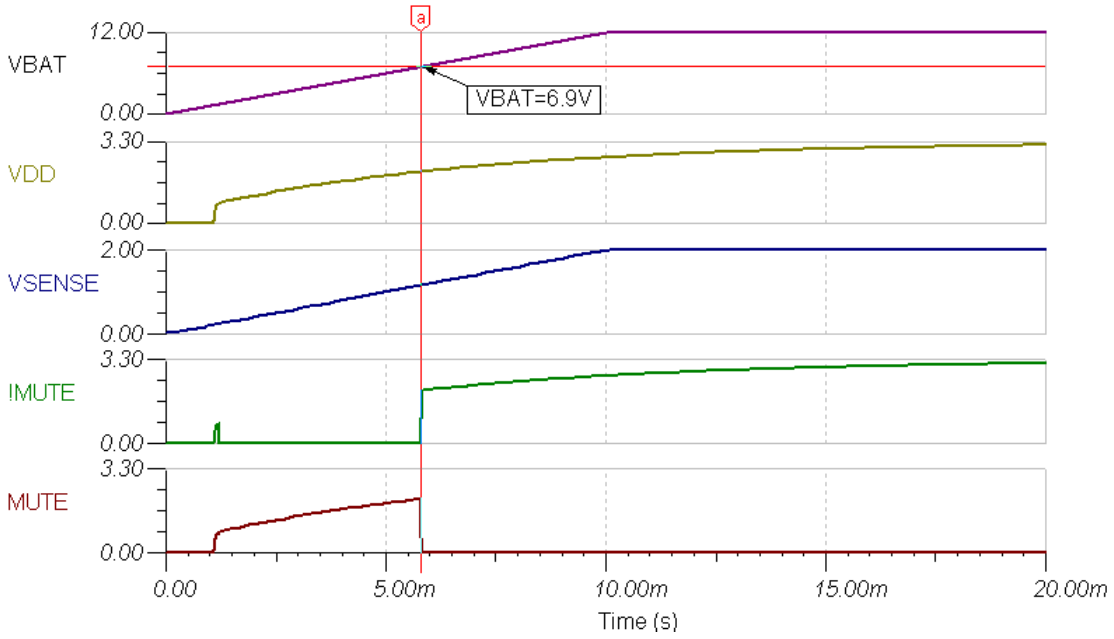
   The SNS-OUT pin is pulled low when the SNS voltage is less than the reference voltage, approximately 1.15V. Using 10kΩ for R_3 and 2kΩ for R_4, it is estimated that the device will be muted if the $V_{BATTERY}$ supply drops below approximately 6.9V.

   The capacitor $C_{NR/SS}$ is used by the LDO to reduce noise and enables the LDO soft-start function.
5. The DAC is selected based on the needs of the application. Consider the required SNR, THD+N, and supported I2S interface sample rates. While most audio DACs support rates ranging from 16kHz to 192kHz, not all support rates like 384kHz or 768kHz. Higher rates result in noise shaping that moves the out-of-band noise further from the audible range, but not all audio sources can provide them.

6. The capacitors used for the audio filter should be COG, NP0 type ceramics. COG, NP0 type capacitors have a lower voltage coefficient of capacitance, meaning that the capacitive value of the component is less impacted by the voltage bias across the device. As the capacitors are key for performance of the filter, other types of ceramic capacitors should be avoided in the signal path.
7. The capacitors used for the input and output of the LDO should have low equivalent series resistance (ESR), such as X7R-, X5R-, and COG-type capacitors.
8. The resistors used for the LDO and voltage supervisor can be thick-film, though the accuracy of the resistor dividers will impact the LDO output voltage and the supervisor threshold. For this reason, it recommended that R_1, R_2, R_3, and R_4 have a maximum tolerance of 1%.
9. Thin-film resistors are recommended for the resistive elements in the DAC output filter.

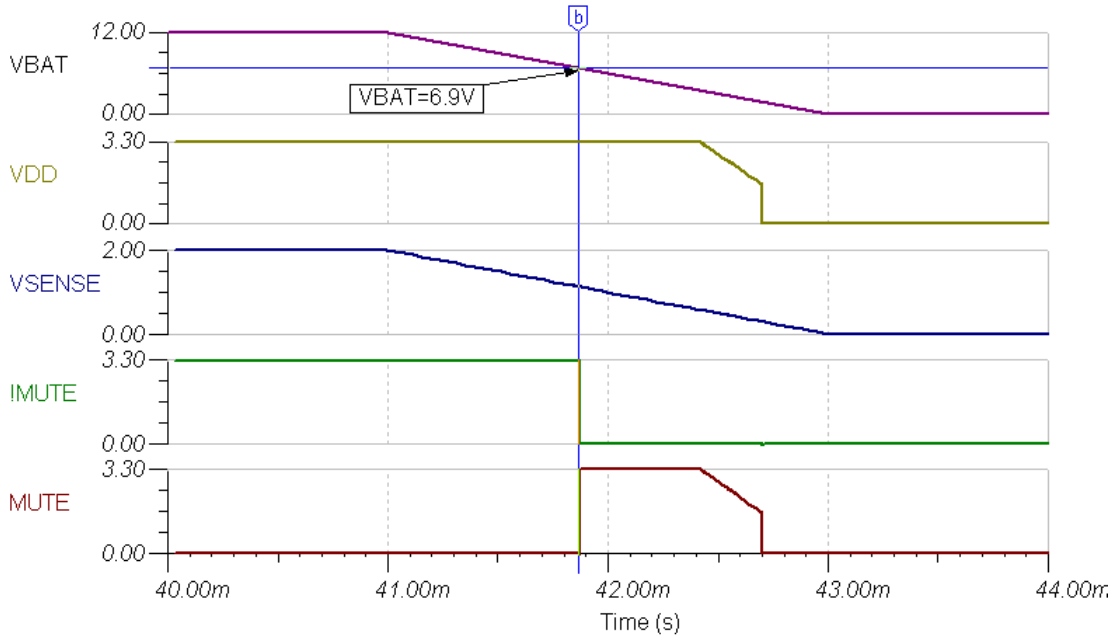
Power-Up Mute Transient

The following simulation shows the power-up transient of the circuit. It can be seen that $\overline{\text{MUTE}}$ output is not released until the VBAT input reaches approximately 6.9V.



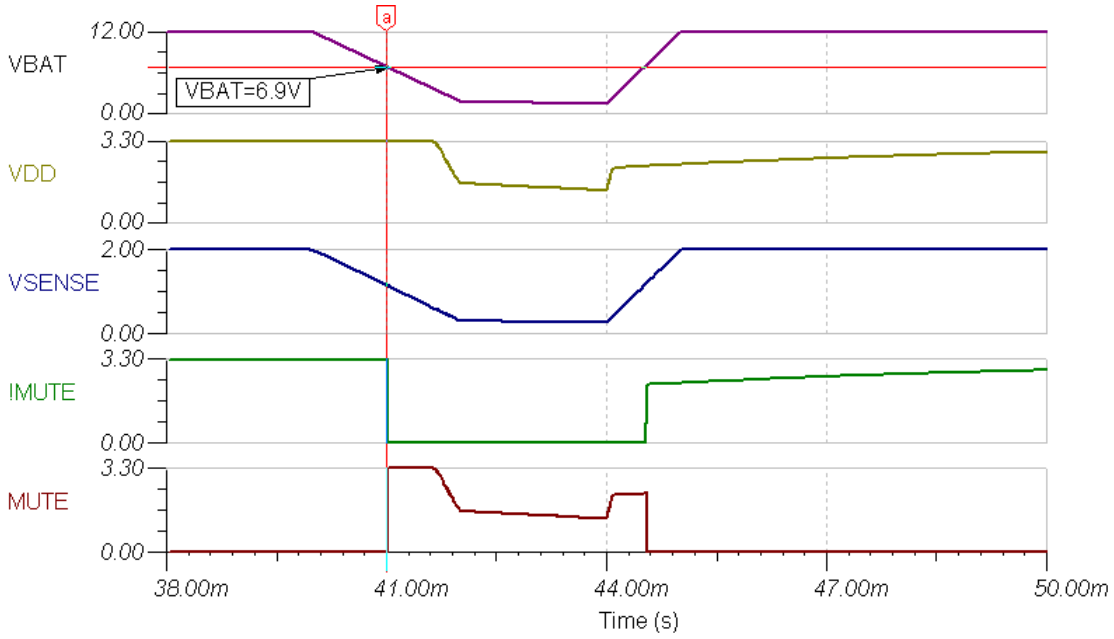
Power-Down Mute Transient

The following simulation shows that the $\overline{\text{MUTE}}$ output is asserted to low when the VBAT input drops below 6.9V.



Brown-Out Mute Transient

The following simulation demonstrates that the DAC will be in a mute condition before the VDD supply of the DAC is compromised by the brown-out event. When the VBAT voltage drops below approximately 6.9V, the $\overline{\text{MUTE}}$ signal is asserted low. Once the VBAT recovers, the $\overline{\text{MUTE}}$ signal deasserted.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
PCM5102A	2VRMS DirectPath™, 112-dB audio stereo DAC with 32-bit, 384-kHz PCM interface	2VRMS DirectPath™, 112dB Audio Stereo DAC with 32-bit, 384kHz PCM Interface	Audio DACs
TPS7A8300	2A, 6μV_{RMS}, low-noise, LDO voltage regulator	2A, low-VIN, low-2A, low-VIN, low-noise, ultra-low-dropout voltage regulator with power good wi	Linear & low-dropout (LDO) regulators
TPS389001	Low quiescent current, 1% accurate voltage supervisor with programmable delay	Low-quiescent current 1% accuracy supervisor with programmable delay	Supervisor & reset ICs
CSD13380F3	12-V N-channel FemtoFET™ MOSFET	12V, N channel NexFET™ power MOSFET, single LGA 0.6mm x 0.7mm, 76mOhm, gate ESD protection	MOSFETs

Design References

Texas Instruments, SBAM414 circuit companion simulation files, software

Other Links:

Texas Instruments, Precision DAC Learning Center, portfolio overview

Texas Instruments, Audio DACs, portfolio overview

Trademarks

All trademarks are the property of their respective owners.

Analog Engineer's Circuit

Current-to-Voltage Converter Circuit for Audio DACs

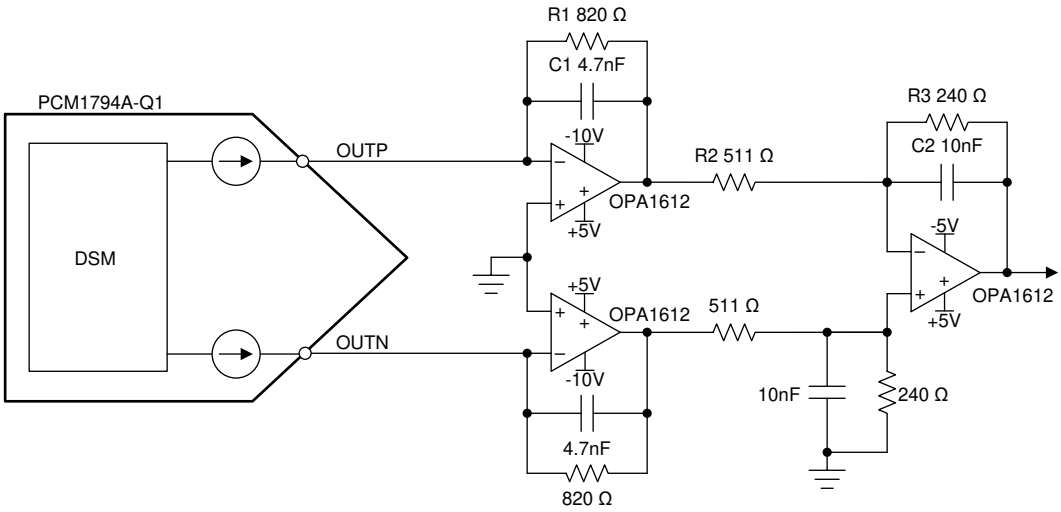
Paul Frost

Design Goals

DAC I_{OUT} Amplitude	DAC I_{OUT} Common Mode Current	V_{OUT} Amplitude
$7.8mA_{P-P}$	–6.2mA	$2.1V_{RMS}$

Design Description

Many high-performance audio digital-to-analog converters (DACs) feature a current output that must be converted into a voltage output for use with audio amplifiers. In premium automotive audio applications, for example, it is critical that the DAC signal-to-noise ratio (SNR) and total harmonic distortion plus noise (THD+N) performance is not compromised by the current-to-voltage (I-V) output stage.



Design Notes

1. The first stage of the circuit converts the current output to a voltage output by providing a virtual ground potential to the OUTP and OUTN nodes of the DAC. The current flowing from the DAC then creates a voltage across the resistor, R1, in the feedback loop. Note that current-output audio DACs have a common-mode current that creates an offset to confirm that the DAC is always sourcing current. This common-mode current also results in the output of the first stage always being a negative value. The supplies of the amplifiers of the circuit are not required to be symmetrical.
2. The second stage of the circuit is a differential amplifier that converts the differential voltage of the first stage into a single-ended output voltage.

Design Steps

1. The DAC is selected based on the needs of the application. Consider the required SNR, THD+N, and supported I2S interface sample rates. While most audio DACs support rates ranging from 16kHz to 192kHz, not all support rates like 384kHz or 768kHz. Higher rates result in noise shaping that moves the out-of-band

noise further from the audible range, but not all audio sources can provide them. Also note that not all current-output audio DACs have the same amplitude and common-mode current.

2. Select the amplifier based on its noise and THD performance. These amplifiers must not gate the SNR performance of the DAC. A JFET or bipolar-input amplifier is recommended for its low voltage-noise. The higher current-noise is not an issue as the resistance values of the circuit are low.
3. The gain of the circuit is calculated with the following equation. Using R1 = 820Ω, R2 = 511Ω, and R3 = 240Ω, the output voltage will be approximately $6V_{P-P}$ or $2.1V_{RMS}$. For this circuit, preferable noise performance is achieved by having the first stage have a large gain, and the second stage actually attenuate the signal.

$$V_{OUT}(I_{IN}) \quad I_{IN} \times R1 \times \left(\frac{R3}{R2}\right)$$

4. The cutoff frequency (f_C) of the first stage can be calculated with the following equation:

$$f_{C-FIRSTSTAGE} = \frac{1}{2 \times \pi \times R1 \times C1}$$

The f_C of the second stage is calculated with the following equation:

$$f_{C-SECONDSTAGE} = \frac{1}{2 \times \pi \times R3 \times C2}$$

Using C1 = 4.7nF and C2 = 10nF, the f_C of the first stage is approximately 44.2kHz and the f_C of the second stage is approximately 66.3kHz.

5. The capacitors used for the filter should be COG/NP0 type ceramics. COG/NP0 type capacitors have a lower voltage coefficient of capacitance, meaning that the capacitive value of the component is less impacted by the voltage bias across the device. As the capacitors are key for performance of the filter, other types of ceramic capacitors should be avoided in the signal path.
6. Thin-film resistors are recommended for the resistive elements in the circuits. All resistors feature voltage noise, which is well understood to be dependent on resistance and temperature, as shown in the first equation that follows. But resistors also have a current-noise, which is dependent on the voltage across the resistor, frequency, and a constant, *C*, that is dependent on the material of which the resistor is composed, as shown in the second following equation:

$$S_T = 4kRT,$$

where

- k is Boltzmann's constant
- R is resistance
- T is temperature

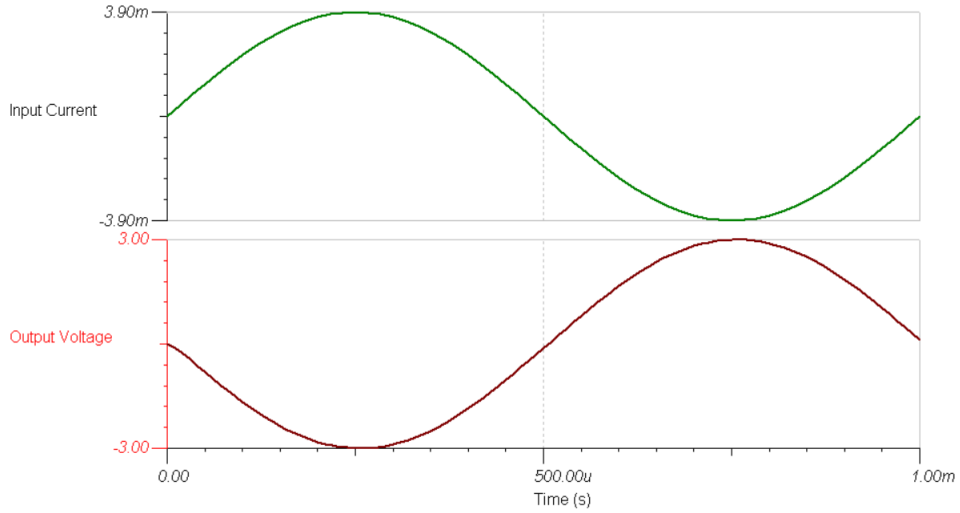
$$S_E = (C \times U^2) \div f$$

where

- C is a constant derived from the resistor material
- U is the differential voltage across the resistor
- f is the frequency

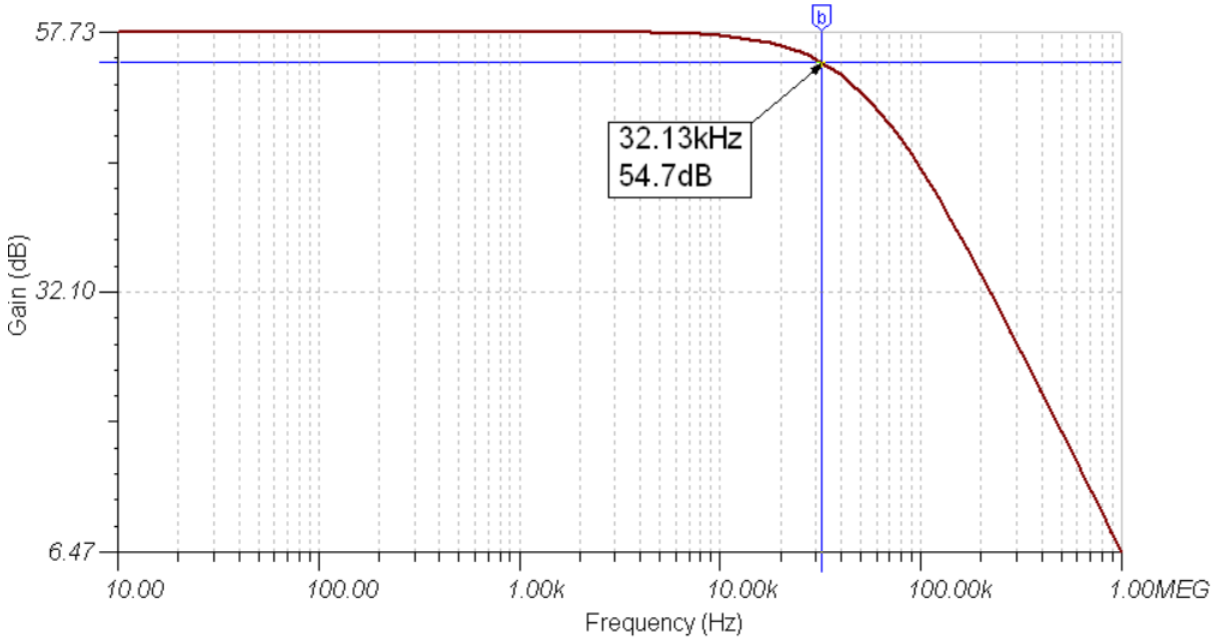
DC Transfer Characteristics

The simulation shows that the 7.8mA$_{P-P}$ differential input current results in an approximately 6V$_{P-P}$ output, or 2.1V$_{RMS}$.



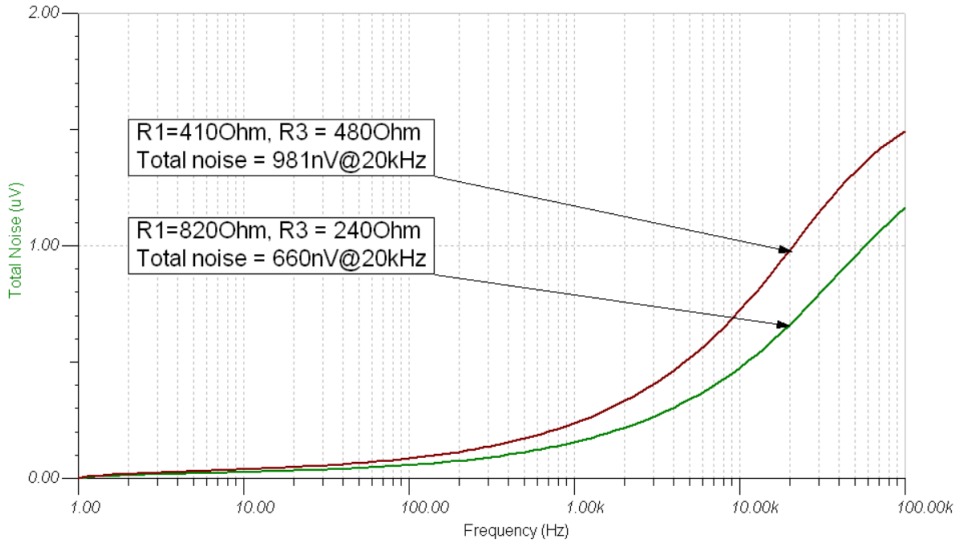
Filter Characteristics

The filters created by the two amplifier stages have a –3dB corner frequency of approximately 32.1kHz. This attenuates out-of-band noise from the output, while not affecting the audible range (20Hz to 22kHz).



Noise Simulation

The following simulation shows the benefit of having the majority of the gain of the circuit in the first stage. The two curves were generated by the same circuit with different resistor values, but resulting in the same total gain. The green line has a higher gain in the first stage, but lower total noise.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
PCM1794A-Q1	24-bit, 192-kHz sampling, advanced segment, audio stereo digital-to-analog converter	132dB, 24-bit, 192-kHz advanced Segment, Audio Stereo Digital-to-Analog Converter	Audio DACs
OPA1612	Ultra-low noise, ultra-low distortion, high-performance, bipolar-input audio operational amplifier	SoundPlus™ Audio Operational Amplifier with 1.1nV/√Hz Noise, Low THD and Precision	Audio Op-Amps

Design References

Texas Instruments, *HiFi Audio circuit design*, application report

Texas Instruments, SBAM413 circuit, simulation files

Other Links:

Texas Instruments, Precision DAC Learning Center, portfolio overview

Texas Instruments, Audio DACs, portfolio overview

Trademarks

All trademarks are the property of their respective owners.

Analog Engineer's Circuit

Circuit for Offset Adjustment of Input Signals Using Precision DAC for Measurement Equipment

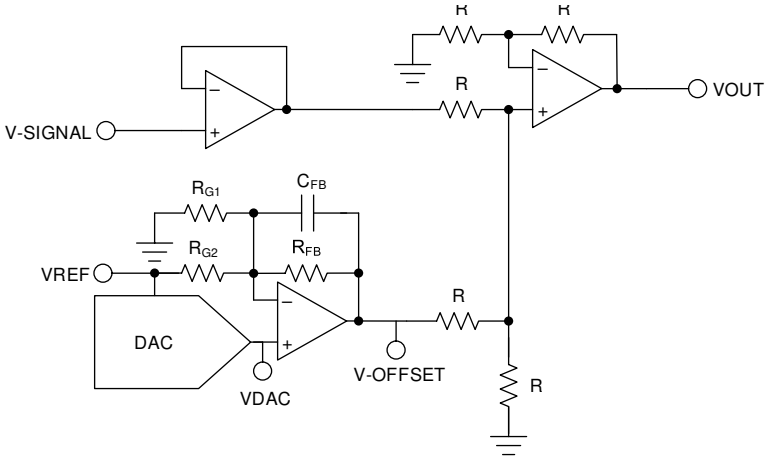
Uttama Kumar Sahu

Design Goals

Power Supply	DAC Output	Voltage Output	Current Output
VCC: 24V, VSS: –5V, VDD: 5V	0V to 2.5V	0V to 5V	0A to 10A

Design Description

Signal-measurement equipment like the *oscilloscope (DSO)* and *data aquisition (DAQ)* must manage input signals that are not within the input range of the measurement analog-to-digital converter (ADC). To bring the unknown input signal in the measurement range of the ADC, the first operation needed is offset control. A programmable offset control circuit providing both positive and negative offset, performs this function. This circuit uses a precision digital-to-analog converter (DAC), followed by a unipolar-to-bipolar conversion circuit using an op amp. The output of this circuit is fed to a summing amplifier that adds this DC output to the input signal.



Design Notes

1. Choose a DAC with the required resolution and output range
2. Choose an op amp with low offset and low drift to minimize error. Thermal noise can be an additional requirement in some applications
3. Choose R_{G1}, R_{G2}, and R_{FB} such that the desired output offset is met
4. Choose the compensation capacitor C_{FB} such that it is larger than the input capacitance of the op-amp inputs

Design Steps

1. Select the DAC80504 device: a 16-bit, 4-channel buffered voltage output DAC with 2.5V internal reference. Devices with an external reference option or devices with accessible internal references are desirable in this application as the reference is used to create an offset. The DAC selection in this design should primarily be based on DC error contributions, typically described by offset-error, gain-error, and integrated non-linearity (INL) error.

2. Select an op amp such as the OPA227 operational amplifier that combines low noise and wide bandwidth with high precision to make it the optimal choice for applications requiring both AC and precision DC performance. Amplifier input offset voltage (V_{OS}) is a key consideration for this design. V_{OS} of an operational amplifier is a typical data sheet specification, but in-circuit performance is also impacted by drift overtemperature, the common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR); therefore, give consideration to these parameters as well.
3. The DC transfer function of the offset voltage is given by:

$$V_{OFFSET} = V_{DAC}\left(1+\frac{R_{FB}}{R_{G2}}+\frac{R_{FB}}{R_{G1}}\right)-V_{REF}\left(\frac{R_{FB}}{R_{G2}}\right)$$

   - First, using the previous transfer function, consider the negative full-scale output case when V_{DAC} is equal to 0V, V_{REF} is equal to 2.5V, and V_{OFFSET} is equal to –5V. This case is used to calculate the ratio of R_{FB} to R_{G2} and is shown in the following equation:

$$-5\,V = -\frac{R_{FB}}{R_{G2}}(2.5V)$$

     That gives, $R_{FB} = 2 \times R_{G2}$.
   - Second, consider the positive full-scale output case when V_{DAC} is equal to 2.5 V, V_{REF} is equal to 2.5V, and V_{OUT} is equal to 5V. This case is used to calculate the ratio of R_{FB} to R_{G1} and is shown in the following equation:

$$5V = \left(1+\frac{R_{FB}}{R_{G2}}+\frac{R_{FB}}{R_{G1}}\right)(2.5\,V)-\left(\frac{R_{FB}}{R_{G2}}\right)(2.5\,V)$$

     This means, $R_{G1} = R_{FB}$.
   - Finally, select a value of R_{G2} to calculate the ideal values of R_{FB} and R_{G1}. The key considerations for seeding the value of R_{G2} should be the drive strength of the reference source as well as choosing small resistor values to minimize noise contributed by the resistor network. For this design, R_{G2} was chosen to be 8kΩ, which will limit the peak current draw from the reference source to approximately 312µA, under nominal conditions. The 312µA is well within the 5-mA limit of the DAC80504 device. By putting the value of R_{G2} in previous equations, R_{G1} and R_{FB} is calculated as $R_{G1} = R_{FB} = 16k\Omega$.
4. In general, the compensation capacitor C_{FB} is not set by fixed equations, but rather by choosing values while observing the output small-signal step response. Through simulation in this example, select $C_{FB} \geq 22pF$.

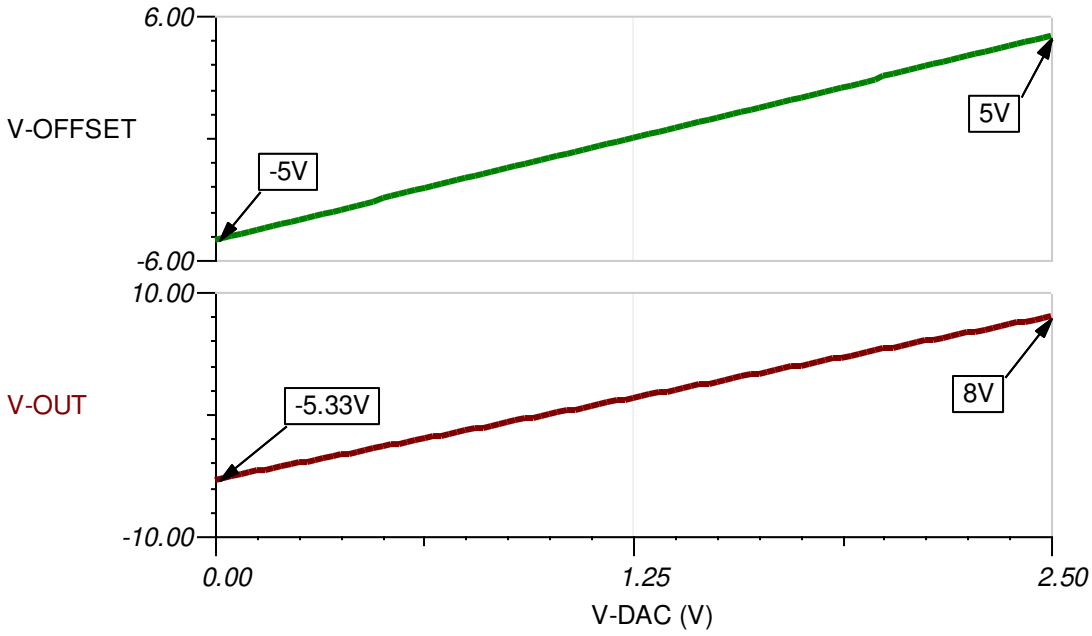


Figure 1-1. DC Transfer Characteristics

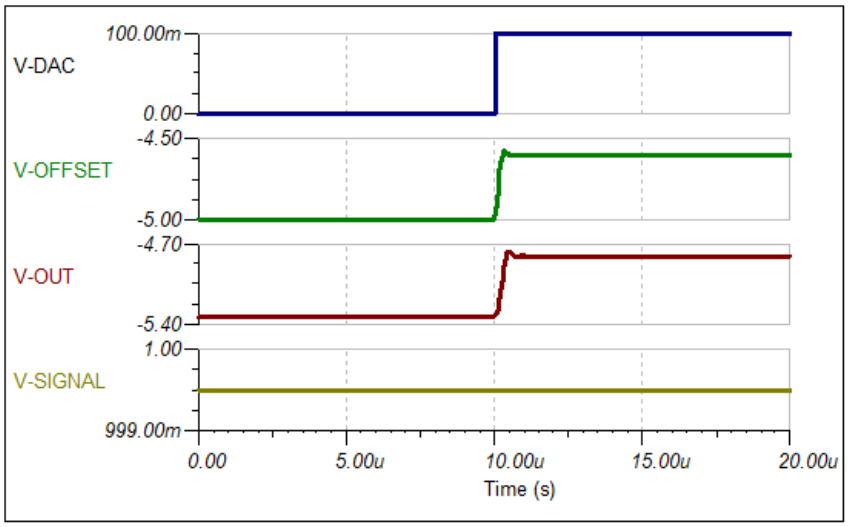


Figure 1-2. Small-Signal Step Response Without Compensation

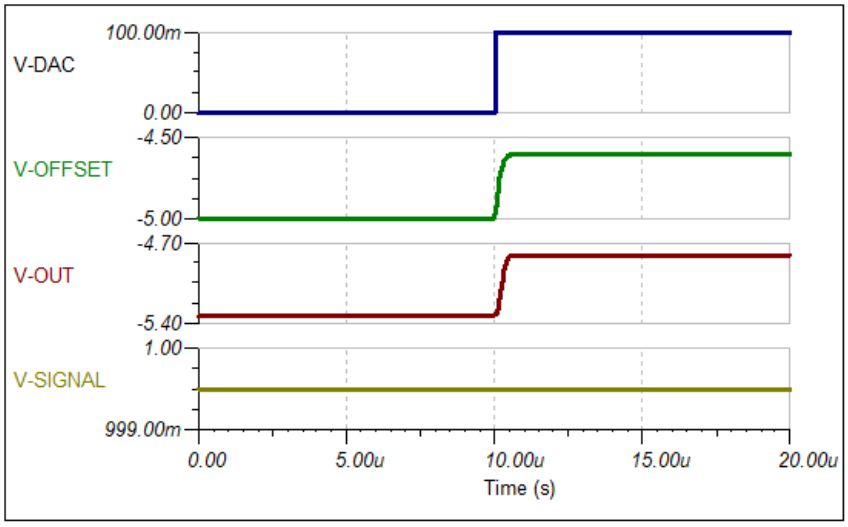


Figure 1-3. Small-Signal Step Response With C_{FB} = 22pF

Design Featured Devices and Alternative Parts

Device	Key Features	Link
DAC80504	4-channel, true 16-bit, SPI, voltage-output DAC with precision internal reference	True 16-bit, 4-channel, SPI, voltage-output DAC in QFN package with precision internal reference
DAC80508	8-channel, true 16-bit, SPI, voltage-output DAC with precision internal reference	16-Bit, Ultralow Glitch, Voltage Output, Digital to Analog Converter
DAC80004	Ultra-small, true 16-bit quad voltage output DAC with 1LSB INL/DNL	Ultra-Small, true 16-bit quad voltage output DAC with 1LSB INL/DNL
DAC8560	16-bit, single-channel, low-power, ultra-low glitch, voltage output DAC with 2.5V, 2ppm/°C reference	16-bit, single-channel, low-power, ultra-low glitch, voltage output DAC with 2.5V,2ppm/°C reference
OPA227	High precision, low noise operational amplifiers	High Precision, Low Noise Operational Amplifiers
OPA188	Precision, low-noise, rail-to-rail output, 36-V zero-drift operational amplifier	Precision, Low-Noise, Rail-to-Rail Output, 36V Zero-Drift Operational Amplifier

Trademarks

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Analog Engineer's Circuit

DAC Force and Sense Reference Drive Circuit

Paul Frost

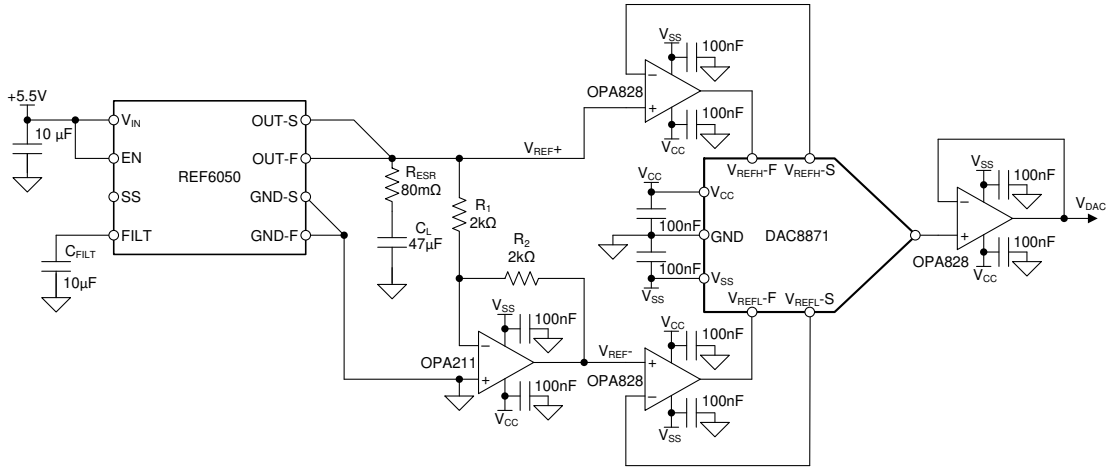
Design Goals

DAC Output Range	DAC $V_{REF}H$ Input Voltage	DAC $V_{REF}L$ Input Voltage
–5V to 5V	5V	–5V

Design Description

High-precision digital-to-analog converters (DACs) used in applications like *magnetic resonance imaging (MRI) machines* and *arbitrary waveform generators (AWG)* generally require a high-precision voltage reference. A cause of common issues with these systems is the undesired series resistance on the reference input of the DAC. The resistance will induce a DAC input-code dependent voltage potential across them as the input current of the R-2R ladder changes based on the code. The end result is that the reference voltage will seem to change based on the DAC code, which will cause a bow shaped integrated non-linearity error curve.

To remedy this issue, high-precision DACs often feature a reference force and sense pin for each of the reference inputs ($V_{REF}H$ and $V_{REF}L$). While these pins are essentially just two parallel connections with individual series resistance to the reference input nodes of the R-2R ladder, the addition of an external unity-gain reference buffer will allow the voltage at the node to be compensated by the amplifier. The small bias current flowing into the op amp inverting input will generate a minimum voltage across the series resistance of the sense input, while output of the op amp can source the current required by the R-2R ladder.



Design Notes

1. The reference selected only has a positive 5-V output, necessitating an inverting amplifier to generate the V_{REF}- value. The resistors R_1 and R_2 also create a current path from the reference output to a –5V potential. This current is provided by the voltage reference. The current can be limited by increasing the values of R_1 and R_2, at the expense of additional noise being created by the circuit. The current noise of the amplifier and the thermal noise of the resistors contribute to the total noise of the circuit.
2. The noise of the reference is reduced by adding C_{FILT}, which filters the noise generated by the band gap of the internal reference. The output of the reference also requires a capacitor (C_L) with a minimum equivalent

series resistance (ESR). It is possible to create this resistance on the PCB with an extended trace, shown as R_{ESR}.

3. The noise of the DAC is primarily created by the thermal noise of the resistor ladder. Thermal noise is calculated using the following the equation, where K_b is Boltzmann's constant, T is the temperature in kelvin, R is the resistance of the ladder, and F is the frequency range.

$$V_{NOISE} = \sqrt{4 \cdot K_b \cdot T \cdot R \cdot \Delta F}$$

The DAC8871 typical output impedance of approximately 6.25kΩ, and assuming room temperature operation, has a thermal noise that can be calculated as shown in the following equation:

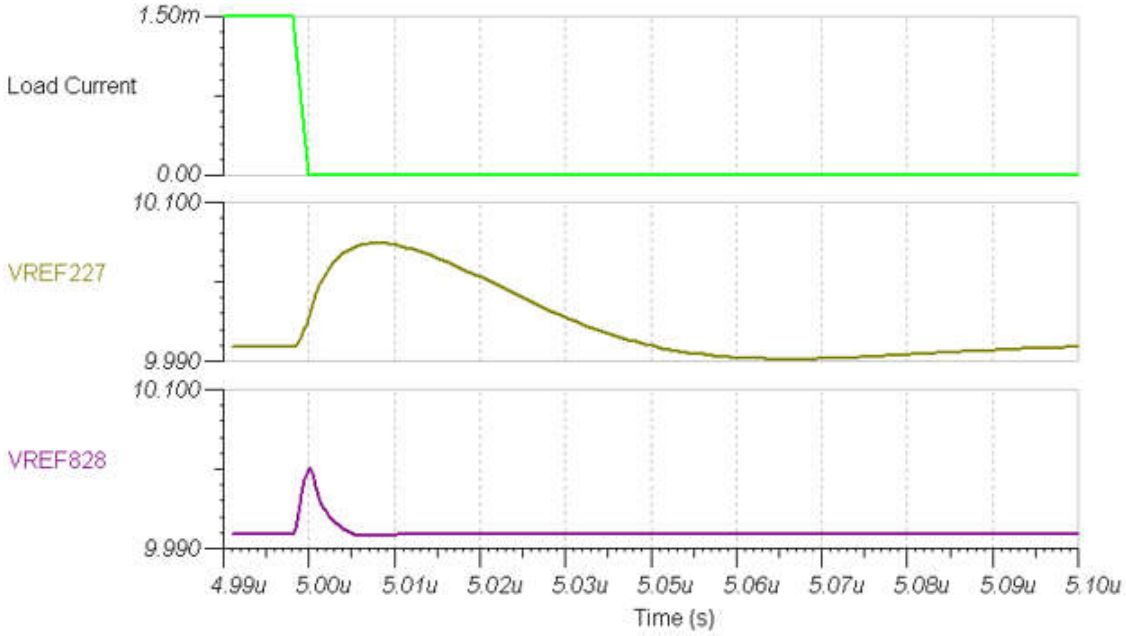
$$V_{NOISE} = \sqrt{4 \cdot 1.38 \cdot 10^{-23}\,J/K \cdot 300K \cdot 6.25k\Omega \cdot 1Hz} = 10.17nV/\sqrt{Hz}$$

Design Steps

1. The DAC is selected for its resolution, accuracy, and noise performance. The resolution may be dependent on the application, but it is common to see 16-bit or greater resolution in this circuit. Errors in the output of the DAC are considered non-linearity errors. Non-linearity errors are expressed as integrated non-linearity error (INL) and differential non-linearity error (DNL). Assuming an ideal reference on the input of the DAC, the INL and DNL errors of the system will be caused by resistor inaccuracies of the R-2R ladder.
2. The reference is selected based on the accuracy, thermal drift, and noise requirements of the application. The output voltage accuracy is generally specified as a percentage. The thermal drift is specified in units of ppm/°C (parts-per-million). The noise of the circuit has two specification: the low-frequency noise, usually specified in $V_{PEAK-PEAK}$ over a limited frequency domain (0.1Hz to 10Hz), and the total integrated noise, specified in V_{RMS}.
3. The op amp used to invert the reference voltage should be selected on its noise performance. The amplifier will contribute noise to the system in two ways, its voltage noise and current noise. The contribution from the voltage-noise can be minimized by selecting a bipolar input amplifier, which generally have a low voltage noise. Bipolar input amplifiers also have higher current noise than CMOS input amplifiers, but the current noise is converted to voltage noise via the resistors R_1 and R_2 of the circuit. By minimizing the resistance of those components, the current noise contribution of the amplifier can be minimized.
4. The amplifiers selected to drive the force and sense inputs of the DAC should be selected according to fast settling and bandwidth. When the DAC is updated with a new input code, the switches in the R-2R resistor ladder will cause a sudden change in current that is being demanded from the reference inputs. This results in a transient on the reference inputs that will also be conveyed on the DAC output. If the reference buffer amplifiers can settle quickly, the error on the output will be minimized. In addition, the voltage noise of these amplifiers will contribute to the total noise of the system. For this reason a bipolar or JFET input amplifier should be selected.
5. Select an output buffer if the circuit is desired to drive a load. The DAC8871 is an unbuffered device, meaning that the output of the DAC is a node on the resistor ladder. This amplifier is selected based on the requirements of the load: such as current output capability, capacitive load stability, slew-rate, and voltage range.
6. The capacitors C_{FILT} and C_L are low-ESR, ceramic type capacitors. The voltage rating of the capacitors needs to be compliant with the 5-V reference output.

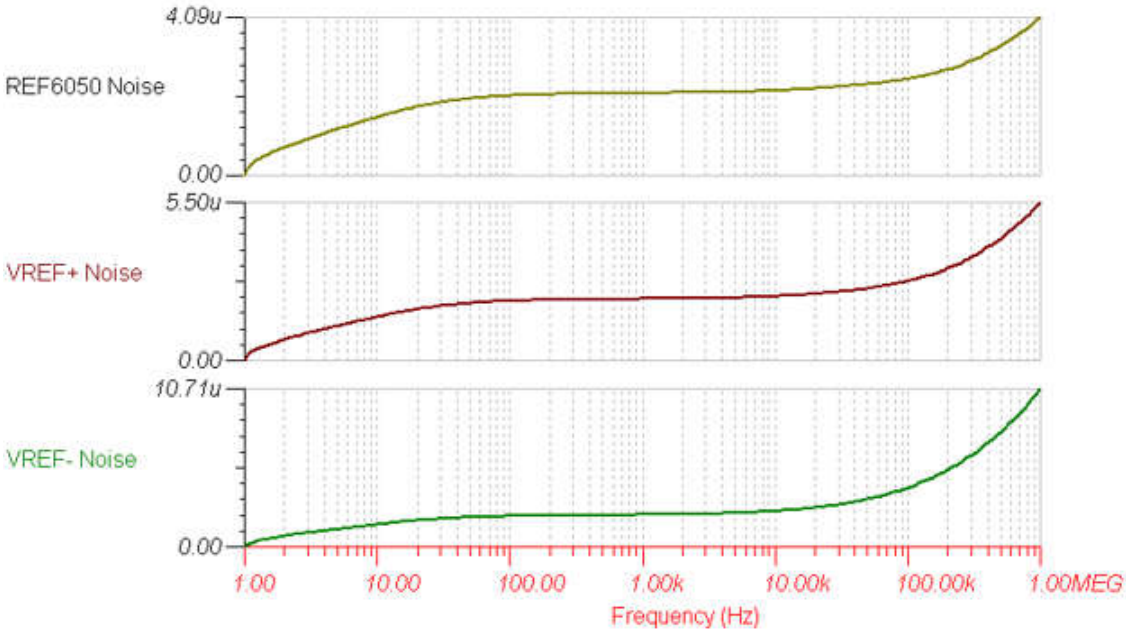
Reference Buffer Load Transient

The reference buffer must be able to quickly source transient currents necessary for the R-2R ladder when the DAC changes codes. Given the architecture of the DAC8871, the maximum transient current would occur when the DAC transitions from zero- or full-scale code to the mid-scale. This transient is simulated with a current source between the $V_{REF}H$ and $V_{REF}L$ inputs. The following simulation shows the differential reference voltage during the current transient, simulated with the OPA828 and OPA227. This shows that the reference error magnitude and duration is reduced with the OPA828.



Reference Buffer Total Noise

The total noise generated by the circuit is shown in the following simulation. The reference, inverting amplifier, and reference buffers each contribute to the noise. Note that the V_{REF}- input has greater noise due to the contribution of the inverting amplifier and the discrete resistors in its feedback network.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
DAC8871	16-bit, single-channel, serial-interface, high-voltage, bipolar-output DAC	16-Bit Single Channel, Serial Interface, ±18V (High Voltage Bipolar) Output DAC	Precision DACs (≤10 MSPS)
OPA828	Low-offset, low-drift, low-noise, 45-MHz bandwidth, JFET-input operational amplifier	High-speed (45MHz and 150V/µs), 36V, low-noise (4nV/√Hz) RRO JFET operational amplifier	Precision op amps (Vos < 1mV)
OPA221	Low-power, 1.1nV/√Hz noise, high-performance operation amplifier	1.1nV/rtHz Noise, Low-Power, Precision Operational Amplifier	Precision op amps (Vos < 1mV)
REF6050	Low-noise, high-precision, 5-V output voltage reference	5V, 5ppm/°C high-precision voltage reference with integrated buffer and enable pin	Series voltage references

Trademarks

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Analog Engineer's Circuit

Power-Supply Margining Circuit for LDOs Using a Precision DAC

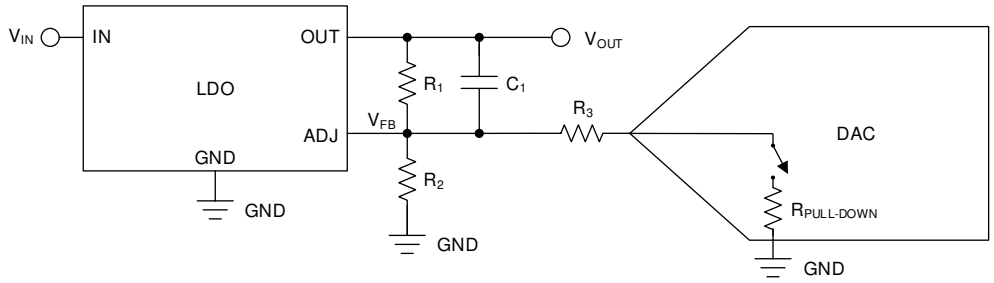
Uttama Kumar Sahu

Design Goals

Power Supply (VDD)	Nominal Output	Margin High	Margin Low
5V	3.3V	3.3V + 10%	3.3V – 10%

Design Description

A power-supply margining circuit is used for tuning the output of a power converter. This is done either to adjust the offset and drift of the power supply output or to program a desired value at the output. Adjustable power supplies like Low-Dropout Regulators (LDOs) and DC/DC converters provide a feedback or adjust input that is used to set the desired output. A precision voltage output digital-to-analog converter (DAC) is designed for controlling the power-supply output linearly. The following image shows an example power-supply margining circuit. Typical applications of power-supply margining is in test and measurement, communications equipment, and power delivery.



Design Notes

1. Choose a DAC with the required resolution, pulldown resistor value, and output range.
2. Derive the relationship of the DAC output to V_{OUT}.
3. Choose R_1 based on typical current through the feedback circuit.
4. Calculate the start-up or nominal value of V_{DAC} considering the power-down and power-up conditions of the DAC.
5. Select R_2, and R_3 such that the desired start-up output voltage is met along with the DAC output voltage range for the desired tuning range.
6. Calculate the margin low and margin high DAC outputs.
7. Choose a compensation capacitor to achieve the desired step response.

Design Steps

1. Select the LDO TPS79501 device for the calculations. The DAC53608 device is an ultra-low cost, 10-bit, 8-channel, unipolar output DAC designed for such applications
2. The output voltage of the power supply is given by:

$V_{OUT} \quad V_{REF} + I_1 R_1 \quad V_{REF} + (I_2 + I_3) R_1$

where

- I_1 is the current flowing through R_1
- I_2 is the current flowing through R_2
- I_3 is the current flowing through R_3

DACs in this application typically include power-down mode, which includes an internal pulldown resistor at the voltage output. Hence, replacing the values of the currents in the previous equation yields:

- When the DAC is in *Power Down* mode:

$$V_{OUT} = V_{REF} + \left(\left(\frac{V_{REF}}{R_2} \right) + \left(\frac{V_{REF}}{R_3 + R_{PULL\text{-}DOWN}} \right) \right) R_1$$

- When the DAC output is powered-up:

$$V_{OUT} = V_{REF} + \left(\left(\frac{V_{REF}}{R_2} \right) + \left(\frac{V_{REF} - V_{DAC}}{R_3} \right) \right) R_1$$

For DAC53608, $R_{PULL\text{-}DOWN}$ is 10kΩ. For the LDO part number TPS79501, the value of V_{REF} is 1.225V.

3. R_1 can be calculated by the following method.
   The current through the FB pin of TPS79501 is 1µA. To make this current negligible, I_1 should be >> I_{FB}. Choose I_1 to be 50µA. Calculate R_1 as follows:

$$R_1 = \frac{V_{OUT} - V_{REF}}{I_1} = 41.5\ k\Omega$$

The nominal value of I_1 can be given by:

- When the DAC is in *Power Down* mode

$$I_{1\text{–}Nom} = \left(\frac{V_{REF}}{R_2} \right) + \left(\frac{V_{REF}}{R_3 + 10\ k\Omega} \right)$$

- When the DAC output is powered-up

$$I_{1\text{–}Nom} = \left(\frac{V_{REF}}{R_2} \right) + \left(\frac{V_{REF} - V_{DAC}}{R_3} \right)$$

The values of I_1 at *Margin High* and *Margin Low* outputs are given by:

$$I_{1\text{-}HIGH} = \frac{V_{OUT\text{-}HIGH} - V_{REF}}{R_1} = 57.95\ \mu A$$

$$I_{1\text{-}LOW} = \frac{V_{OUT\text{-}LOW} - V_{REF}}{R_1} = 42.05\ \mu A$$

$$I_{1\text{-}HIGH} - I_{1\text{-}Nom} = I_{1\text{-}Nom} - I_{1\text{-}LOW} = 7.65\ \mu A$$

4. The nominal or startup value of V_{DAC} can be calculated using the following method:

   To make sure the 10-kΩ resistor does not impact when the DAC is transitioning from power-down to power-up, the power-up value for the DAC voltage can be calculated with:

$$\frac{V_{REF}}{R_3 + 10\ k\Omega} = \frac{V_{REF} - V_{DAC}}{R_3}$$

The previous equation can be further simplified to:

$$V_{DAC} = V_{REF}\left(\frac{10\ k\Omega}{R3 + 10\ k\Omega}\right)$$

5. The values of R_2 and R_3 can be calculated as follows:

   If the power-up or nominal value of V_{DAC} is kept at one-third of V_{REF}, that is, 408.3mV, then R_3 is 2 × 10kΩ = 20kΩ. R_2 can be calculated as:

$$\frac{V_{REF}}{R_2} + \frac{V_{REF}}{R_3 + 10k\Omega} = 50\mu A$$

   Replacing the value of R_3, R_2 can be calculated to equal 133kΩ.

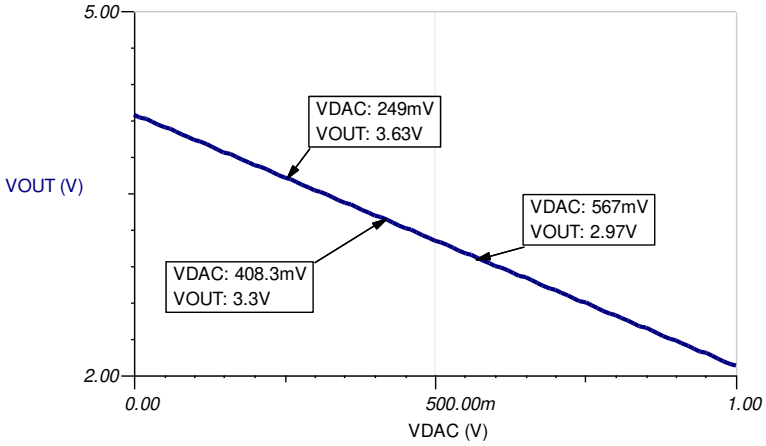
6. Subtracting the *Margin High* and *Nominal* values of I_1 and the corresponding equations, we get

$$\frac{V_{REF} - V_{DAC}}{R_3} - \frac{V_{REF}}{R_3 + 10\ k\Omega} = 7.95\ \mu A$$

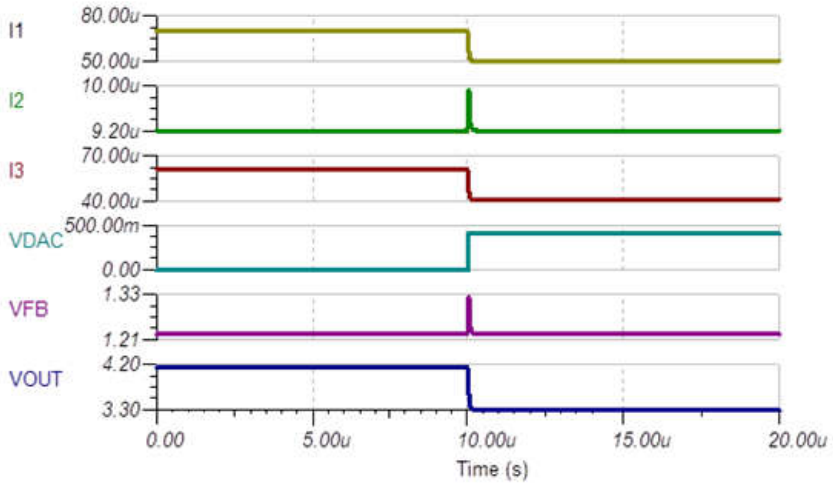
   So, the *Margin High* value of V_{DAC} is 249mV and similarly, the *Margin Low* value can be calculated as 567mV from the following equation:

$$\frac{V_{REF}}{R_3 + 10\ k\Omega} - \frac{V_{REF} - V_{DAC}}{R_3} = 7.95\ \mu A$$

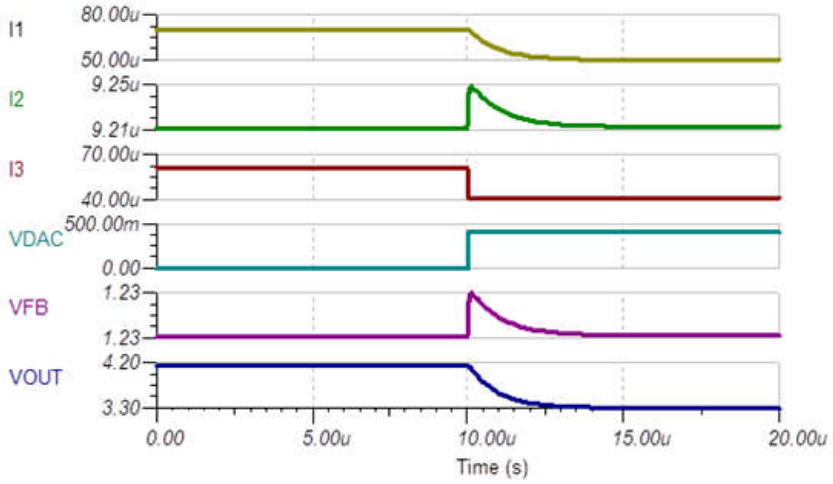
7. The step response of this circuit without a compensation capacitor has some overshoot and ringing as shown in the following curves. This kind of transient response can cause errors at the load circuits. To minimize this, use a compensation capacitor C_1. The value of this capacitance is usually obtained through simulation. A comparative output shows the waveforms with a compensation capacitor of 22pF.



DC Transfer Characteristics



Small Signal Step Response Without Compensation



Small-Signal Step Response With C_1= 22pF

Design Featured Devices and Alternative Parts

Device	Key Features	Link
DAC53608	8-channel 10-bit, I2C interface, buffered-voltage-output DAC	10-Bit, 8-channel, I2C, voltage output DAC in tiny QFN package
DAC60508	8-channel, true 12-bit, SPI, voltage-output DAC with precision internal reference	True 12-Bit, 8-channel, SPI, Vout DAC in tiny WCSP package with precision internal reference
DAC60501	12-bit, 1-LSB INL, DAC with precision internal reference	True 12-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference
DAC8831	16-bit, ultra-low power, voltage output DAC	16-Bit, Ultra-Low Power, Voltage Output Digital to Analog Converter
TPS79501-Q1	Automotive catalog single output LDO, 500mA, adj.(1.2 to 5.5V), low-noise, high PSRR	Automotive 500mA, adjustable low-dropout voltage regulator with enable

Design References

Texas Instruments, SBAM415 TINA source files, software support

Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (January 2019) to Revision A (September 2019)	Page
• Updated circuit image and equation	1

Analog Engineer's Circuit

Power-Supply Margining Circuit for SMPS Using a Precision DAC

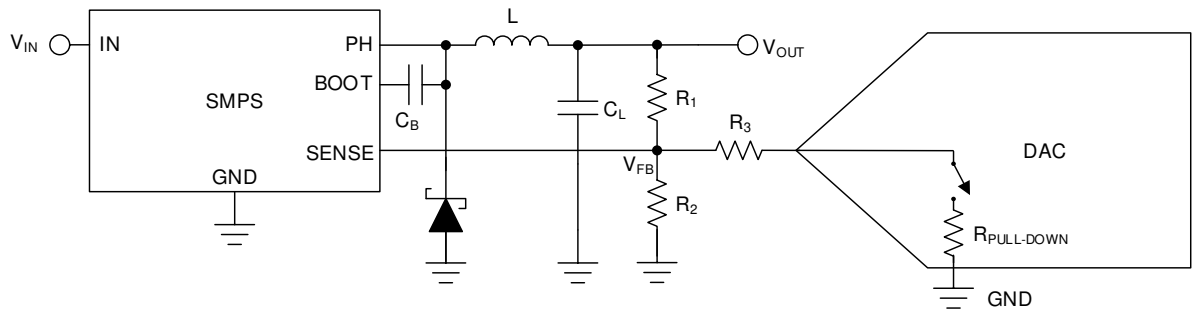
Uttama Kumar Sahu

Design Goals

Power Supply (DAC VDD)	Nominal Output	Margin High	Margin Low
5V	5V	5V + 10%	5V – 10%

Design Description

A power-supply margining circuit is used for tuning the output of a power converter. This is done either to adjust the offset and drift of the power-supply output or to program a desired value at the output. Adjustable power supplies like LDOs and DC/DC converters provide a feedback or adjust input that is used to set the desired output. A precision voltage output DAC is designed for controlling the power-supply output linearly. An example power-supply margining circuit is shown in the following figure. Typical applications of power-supply margining are in *test and measurement*, *communications equipment*, and *general purpose power supply modules*.



Design Notes

1. Choose a DAC with required resolution, pulldown resistor value, and output range
2. Derive the relationship of the DAC output to V_{OUT}
3. Choose R_1 based on typical current through the feedback circuit
4. Calculate the start-up or nominal value of V_{DAC}, considering the power-down and power-up conditions of the DAC
5. Select R_2, and R_3 such that the desired start-up output voltage is met along with the DAC output voltage range for the desired tuning range
6. Calculate the margin low and margin high DAC outputs
7. Choose a compensation capacitor to get the desired step response

Design Steps

1. Select the switching DC/DC converter TPS5450 for the calculations. The DAC53608 device is an ultra-low cost, 10-bit, 8-channel unipolar output DAC designed for such applications
2. The output voltage of the power supply is given by

$$V_{OUT} = V_{REF} + I_1 R_1 = V_{REF} + \left(I_2 + I_3\right) R_1$$

where

- I_1 is the current flowing through R_1
- I_2 is the current flowing through R_2
- I_3 is the current flowing through R_3

DACs in this application typically include power-down mode, which includes an internal pulldown resistor at the voltage output. Hence, replacing the values of the currents in the previous equation yields:

- When DAC is in power-down mode:

$$V_{OUT} = V_{REF} + \left(\left(\frac{V_{REF}}{R_2}\right) + \left(\frac{V_{REF}}{R_3 + R_{PULL-DOWN}}\right)\right) R_1$$

- When DAC output is powered-up:

$$V_{OUT} = V_{REF} + \left(\left(\frac{V_{REF}}{R_2}\right) + \left(\frac{V_{REF} - V_{DAC}}{R_3}\right)\right) R_1$$

For DAC53608, $R_{PULLDOWN}$ is 10kΩ. For the LDO device TPS5450, the value of V_{REF} is 1.221V.

3. R_1 can be calculated with the following method:
   The current through the FB pin of the TPS5450 device is negligible. Select I_1 to be 50µA. So, R_1 is calculated as follows:

$$R_1 = \frac{V_{OUT} - V_{REF}}{I_1} = 75.6\ k\Omega$$

The nominal value of I_1 is given by:

- When DAC is in power-down mode:

$$I_{1-Nom} = \left(\frac{V_{REF}}{R_2}\right) + \left(\frac{V_{REF}}{R_3 + 10\ k\Omega}\right)$$

- When DAC output is powered-up:

$$I_{1-Nom} = \left(\frac{V_{REF}}{R_2}\right) + \left(\frac{V_{REF} - V_{DAC}}{R_3}\right)$$

The values of I_1 at margin high and margin low outputs are given by:

$$I_{1-HIGH} = \frac{V_{OUT-HIGH} - V_{REF}}{R_1} = 56.6\mu A$$

$$I_{1-LOW} = \frac{V_{OUT-LOW} - V_{REF}}{R_1} = 43.4$$

$$I_{1-LOW} = \frac{V_{OUT-LOW} - V_{REF}}{R_1} = 43.4$$

4. The nominal, or start-up value of V_{DAC} is calculated by the following method:

   To make sure the 10-kΩ resistor does not impact when the DAC is transitioning from power-down to power-up, the power-up value for the DAC voltage is calculated with:

$$\frac{V_{REF}}{R_3 + 10\ k\Omega} = \frac{V_{REF} - V_{DAC}}{R_3}$$

The previous equation is further simplified to:

$$V_{DAC} = V_{REF}\left(\frac{10\ k\Omega}{R_3 + 10\ k\Omega}\right)$$

5. The values of R_2 and R_3 are calculated as follows:

   If the power-up or nominal value of V_{DAC} is kept at 1/3 of V_{REF}, that is, 407mV, then R_3 is 2 × 10kΩ = 20kΩ. And, R_2 can be calculated as:

$$\frac{V_{REF}}{R_2} + \frac{V_{REF}}{R_3 + 10k\Omega} = 50\mu A$$

   Replacing the value of R_3, calculate R_2 = 131.3kΩ.

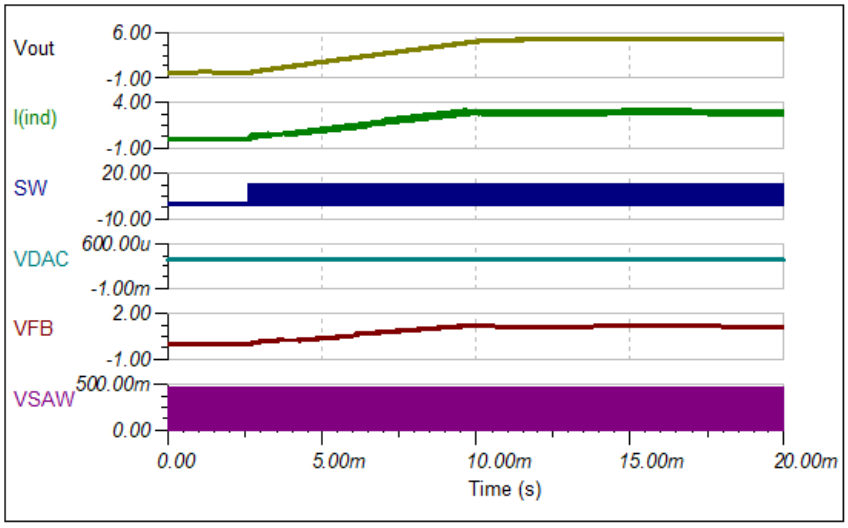
6. Subtracting the margin high and nominal values of I_1 and the corresponding equations yields:

$$\frac{V_{REF} - V_{DAC}}{R_3} - \frac{V_{REF}}{R_3 + 10\ k\Omega} = 6.6\mu A$$

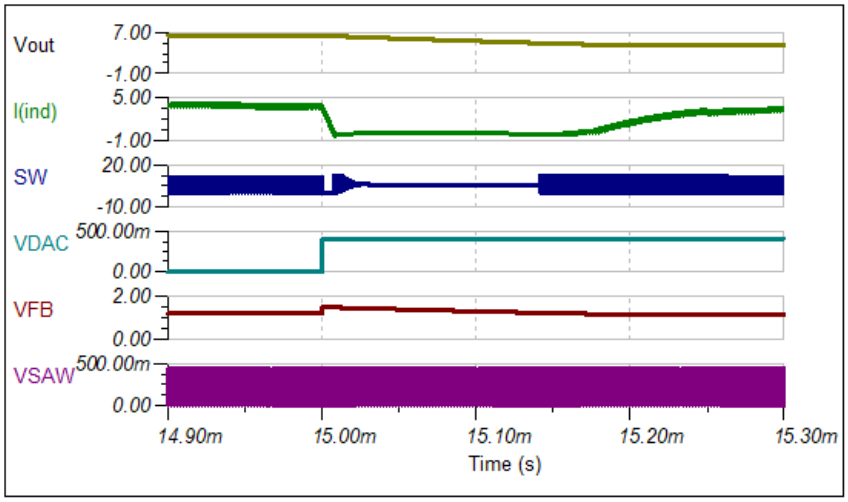
   The margin high value of V_{DAC} is 275mV and similarly, the margin low value is calculated as 539mV using the following equation:

$$\frac{V_{REF}}{R_3 + 10\ k\Omega} - \frac{V_{REF} - V_{DAC}}{R_3} - \ = 6.6\mu A$$

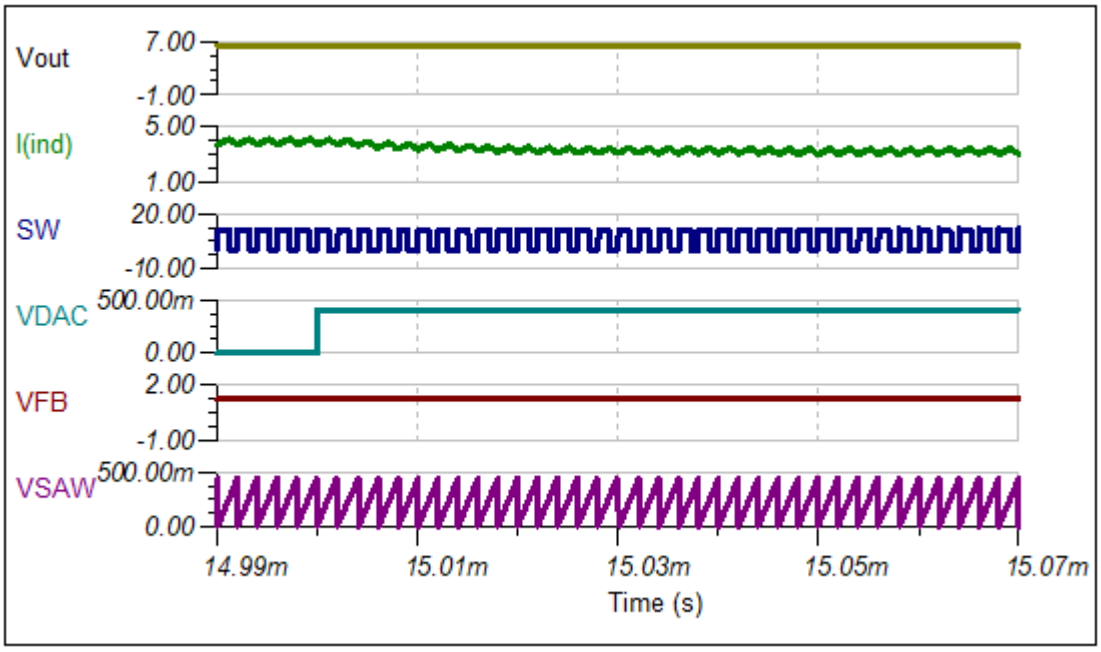
7. The step response of this circuit without a compensation capacitor causes the inductor current to reach its limit as shown in the following figure. This kind of surge can take the inductor into saturation. To minimize the surge, a compensation capacitor C_1 is used as the circuit diagram shows. The value of this capacitance is usually obtained through simulation. A comparative output shows the waveforms with a compensation capacitor of 10nF.



Output With DAC in Power Down Mode



Small-Signal Step Response Without Compensation



Small-Signal Step Response With C_1 = 10nF

Design Featured Devices and Alternative Parts

Device	Key Features	Link
DAC53608	8-channel 10-bit, I2C interface, buffered-voltage-output digital-to-analog converter (DAC)	10-Bit, 8-channel, I2C, voltage output DAC in tiny QFN package
DAC60508	8-channel, true 12-bit, SPI, voltage-output DAC With precision internal reference	True 12-Bit, 8-channel, SPI, Vout DAC in tiny WCSP package with precision internal reference
DAC60501	12-bit, 1-LSB INL, digital-to-analog converter (DAC) with precision internal reference	True 12-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference
DAC8831	16-bit, ultra-low power, voltage output digital to analog converter	16-Bit, Ultra-Low Power, Voltage Output Digital to Analog Converter
TPS5450	5.5V to 36V input, 5A, 500-kHz step-down converter	5.5V to 36V Input, 5A, 500kHz Step Down Converter

Link to Key Files

Texas Instruments, SBAM416 source files, support software

Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (January 2019) to Revision A (September 2019)	Page
• Updated the circuit image	1

Analog Engineer's Circuit

Voltage Margining and Scaling Circuit with a Voltage Output Smart DAC

Smart DAC *Katlynne Jones*

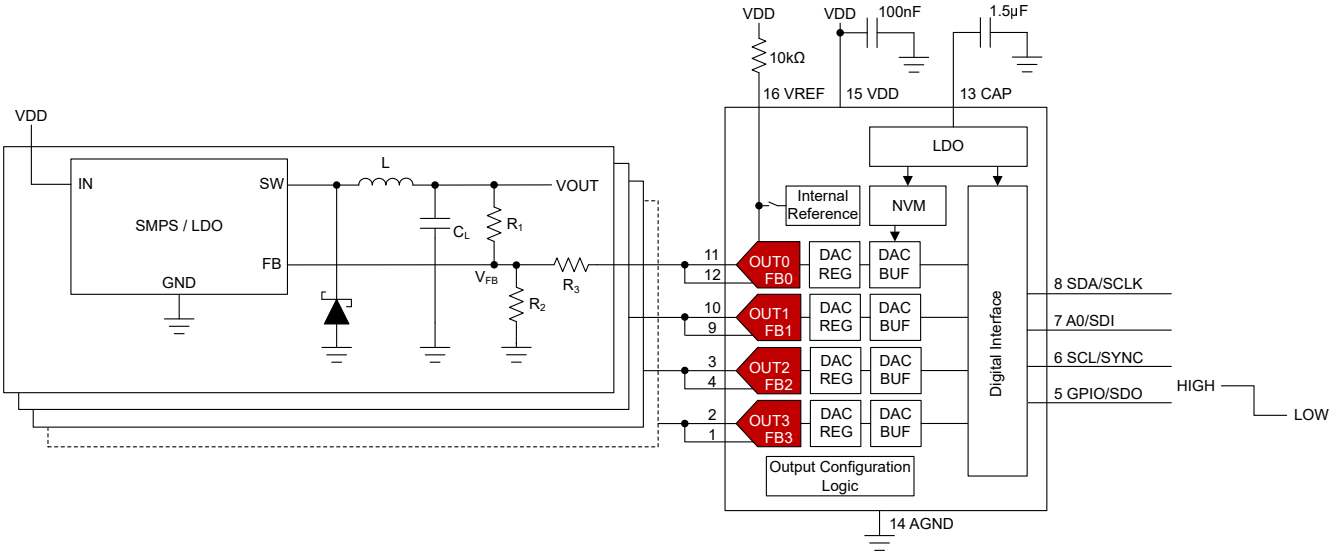
Design Objective

Key Input Parameter	Key Output Signal	Recommended Device
SPI or I^2C communication	0V to 1.2V analog DAC output, 3.3V ±10% SMPS output	DAC53204, DAC63204, DAC43204, DAC53004

Objective: *Provide a margin voltage for an SMPS output of ±10% the nominal value*

Design Description

This circuit uses a four-channel buffered voltage output DAC to voltage margin a switch-mode power supply (SMPS). A voltage margining circuit is used to trim, scale, or test the output of a power converter. Adjustable power supplies, such as low dropout regulators (LDOs), DC/DC converters, or SMPS provide a feedback (FB) input that is used to control the desired output. A precision smart DAC, such as the DAC53204 or DAC53004, provides linear control of the power supply output when the DAC is supplied and the output is powered on. Most DACs include an internal pull-down resistor at the voltage output when the DAC is supplied but the output is in power down mode. Also, when most DACs are completely powered off, the ESD cells on the output pin conduct current if the output is pulled away from ground which is the case in voltage margining circuits. The DAC53204 or DAC53004 provides a high impedance (Hi-Z) output when the DAC is powered off or when the output channel is in power down mode, meaning that the DACs draw very little current through the FB pin of the SMPS and the output is set at the nominal voltage. The DAC53204 and DAC53004 have a general-purpose input (GPI) pin that allows the DAC output to be toggled between a high and low voltage output. This allows the SMPS to be toggled within ±10% of the nominal output value. All register settings can be saved using the non-volatile memory (NVM) on the DAC53204 and DAC53004 meaning that the devices can be used without a processor, even after a power cycle. This circuit can be used in applications such as Communications Equipment, Enterprise Systems, Test and Measurement, and general-purpose power-supply modules.



Design Notes

1. The *DACx3204 12-Bit, 10-Bit, and 8-Bit, Quad Voltage and Current Output Smart DACs With Auto-Detected I2C, PMBus™, or SPI Interface Data Sheet* recommends using a 100nF decoupling capacitor for the VDD pin and a 1.5µF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal LDO. Place these capacitors close to the device pins.
2. There are three reference options for the DAC53204:
   a. An external reference of 1.7V to V_{DD} can be applied to the VREF pin of the device. Connect a 100nF capacitor between the VREF pin and the AGND pin when using the external reference. Use a pullup resistor to V_{DD} when the external reference is not used.
   b. There is a precision 1.21V reference with ×1.5, ×2, ×3, and ×4 gain options.
   c. V_{DD} can be used as a reference.
3. The nominal voltage of the SMPS is set by resistors R_1 and R_2. The SMPS uses an internal 600mV reference voltage at the FB pin to determine the voltage at the output. Calculate R_1 and R_2 using the following equations:

$$R_1 = \frac{V_{NOMINAL} - V_{FB}}{I_{NOMINAL}}$$

$$R_2 = \frac{R_1 \times V_{FB}}{V_{NOMINAL} - V_{FB}}$$

   A nominal current of 100µA through R_1 and R_2 and 3.3V nominal output voltage is used. With these values the equations become:

$$R_1 = \frac{3.3V - 0.6V}{100\mu A} = 27k\Omega$$

$$R_2 = \frac{27k\Omega \times 0.6V}{3.3V - 0.6V} = 6k\Omega$$

4. To achieve the desired margin, the DAC53204 must sink or source additional current through R_1. This current (I_{MARGIN}) is calculated by:

$$I_{MARGIN} = \left(\frac{V_{NOMINAL} \times (1 + MARGIN) - V_{FB}}{R_1}\right) - I_{NOMINAL}$$

   For a ±10% margin, the equation becomes:

$$I_{MARGIN} = \left(\frac{3.3V \times (1 + 0.10) - 0.6V}{27k\Omega}\right) - 100\mu A = 12\mu A$$

5. The voltage output of the DAC53204 is turned into a current through the series resistor R_3. R_3 is calculated by:

$$R_3 = \frac{V_{DAC} - V_{FB}}{I_{MARGIN}}$$

   Avoid DAC codes near zero- and full-scale when determining the DAC output voltage range to avoid the zero- and full-scale errors at these codes. This design uses the internal 1.21V reference with a gain of ×1.5 giving a full-scale voltage of 1.82V. The DAC53204 has a max zero-code error of 15mV, so a 20mV minimum output is a safe choice. I_{MARGIN} is considered positive and is being sourced from the DAC when $V_{DAC} > V_{FB}$. I_{MARGIN} is considered negative and is being sunk by the DAC53204 when $V_{DAC} < V_{FB}$. R_3 is calculated to be 48.3kΩ:

$$R_3 = \frac{20mV - 0.6V}{-12\mu A} = 48.3k\Omega$$

   The maximum output becomes:

$$V_{DAC,\,MAX} = (R_3 \times I_{MARGIN}) + V_{FB}$$

$$V_{DAC,\,MAX} = (48.3k\Omega \times 12\mu A) + 0.6V = 1.18V$$

6. The DAC codes for $V_{DAC,MAX}$ and $V_{DAC,MIN}$ are stored in the DAC-MARGIN-HIGH and DAC-MARGIN-LOW registers. The codes programmed to these registers, in decimal, is calculated using:

$$\text{DAC\_MARGIN\_HIGH} = \frac{V_{DAC,\,MAX}}{V_{REF} \times \text{GAIN}} \times 1024$$

$$\text{DAC\_MARGIN\_LOW} = \frac{V_{DAC,\,MIN}}{V_{REF} \times \text{GAIN}} \times 1024$$

The equations become:

$$\text{DAC\_MARGIN\_HIGH} = \frac{1.18\text{V}}{1.21\text{V} \times 1.5} \times 1024 = 665.7\text{d}$$

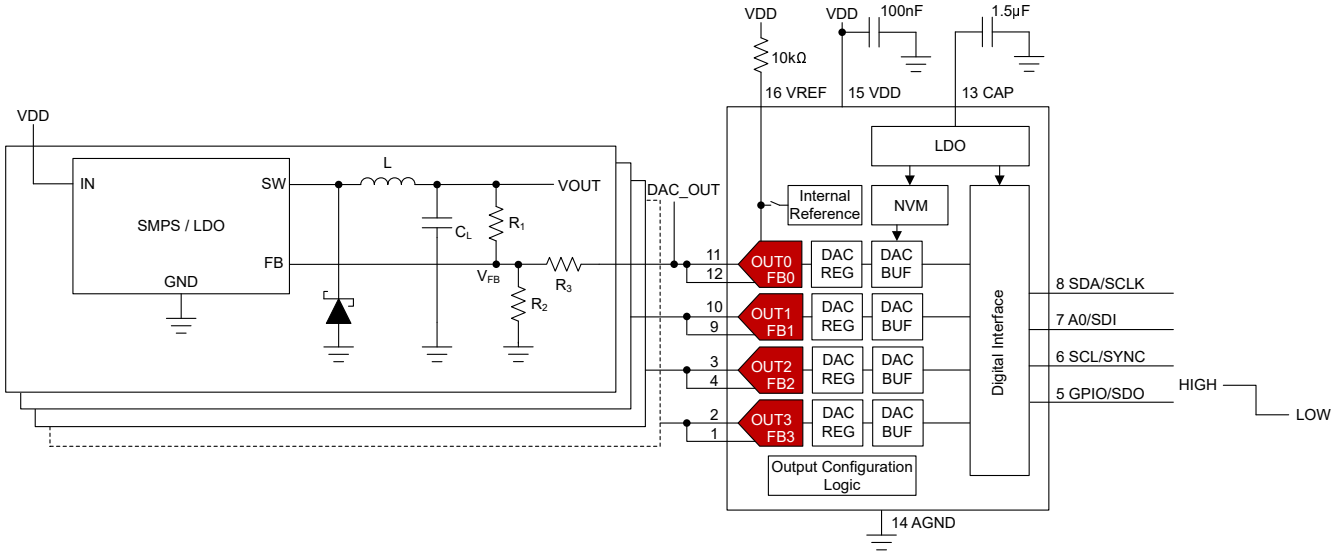
$$\text{DAC\_MARGIN\_LOW} = \frac{20\text{mV}}{1.21\text{V} \times 1.5} \times 1024 = 11.2\text{d}$$

This is rounded to 666d and 11d to give a $V_{DAC,MAX}$ of 1.18V and a $V_{DAC,MIN}$ of 19.5mV.

7. Using a 1.21V reference with a ×1.5 gain and the 10-bit DAC53204, the LSB size, or step size between each code, is about 1.8mV. Using lower reference voltages decreases the LSB size and thus increases the resolution of $V_{DAC,MAX}$ and $V_{DAC,MIN}$.
8. In this design, GPI is used for Margin High, Low function. A high on GPI sets the DAC output to $V_{DAC,MAX}$ and the SMPS V_{OUT} to margin low, or 2.97V. A low on GPI sets the DAC output to $V_{DAC,MIN}$ and the SMPS V_{OUT} to margin high, or 3.63V.
9. The DAC53204 can be programmed with the initial register settings described in the Register Settings section using I^2C or SPI. The initial register settings can be saved in the NVM by writing a 1 to the NVM-PROG field of the COMMON-TRIGGER register. After programming the NVM, the device loads all registers with the values stored in the NVM after a reset or a power cycle.

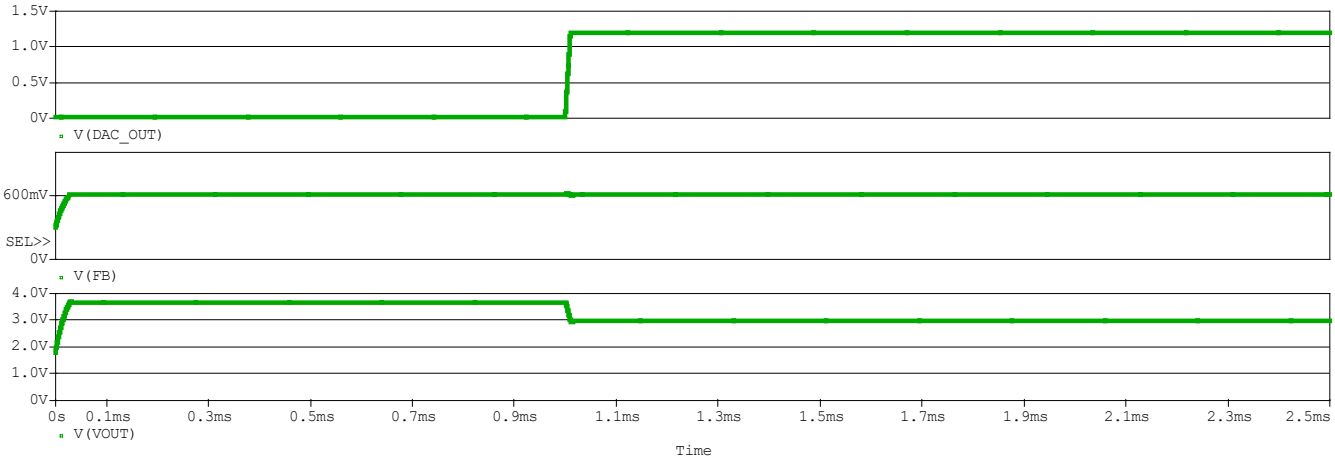
Design Simulations

This schematic is used for the following simulation of the DAC53204.



Transient Simulation Results

The simulation shows the SMPS output (V_{OUT}) responding to the changes on the DAC53204 output (DAC_OUT). When DAC_OUT is at $V_{DAC,MAX}$ the SMPS V_{OUT} goes to margin low, or 2.97V. When DAC_OUT is at $V_{DAC,MIN}$ the SMPS V_{OUT} goes to margin high, or 3.63V.



Register Settings

Register Settings for DAC53204 Voltage Margining

Register Address	Register Name	Setting	Description
0x1F	COMMON-CONFIG	0x1249	[15] 0b0: Write 0b1 to set window-comparator output to a latching output
			[14] 0b0: Write 0b1 to lock device. Unlock by writing 0b0101 to DEV-UNLOCK field in the COMMON-TRIGGER register
			[13] 0b0: Write 0b1 to set fault-dump read enable at address 0x01
			[12] 0b1: Enables the internal reference
			[11:10] 0b00: Powers-up VOUT3
			[9] 0b1: Powers-down IOUT3
			[8:7] 0b00: Powers-up VOUT2
			[6] 0b1: Powers-down IOUT2
			[5:4] 0b00: Powers-up VOUT1
			[3] 0b1: Powers-down IOUT1
			[2:1] 0b00: Powers-up VOUT0
			[0] 0b1: Powers-down IOUT0
0x24	GPIO-CONFIG	0x01F5	[15] 0b0: Write 0b1 to enable glitch filter on GPI
			[14] 0b0: Don't care
			[13] 0b0: Write 0b1 to enable output mode on GPIO pin
			[12:9] 0b0000: Selects the STATUS function setting mapped to GPIO as output
			[8:5] 0b1111: Enables GPI function on all channels
			[4:1] 0b1010: Selects GPI to trigger margin-high, margin-low
			[0] 0b1: Enables input mode for GPIO pin
0x20	COMMON-TRIGGER	0x0002	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11:8] 0b0000: Write 0b1010 to trigger a POR reset
			[7] 0b0: Write 0b1 to trigger LDAC operation if the respective SYNC-CONFIG-X bit in the DAC-X-FUNC-CONFIG register is 1
			[6] 0b0: Write 0b1 to set the DAC registers and outputs to zero-code or mid-code based on the respective CLR-SEL-X bit in the DAC-X-FUNC-CONFIG register
			[5] 0b0: Don't care
			[4] 0b0: Write 0b1 to trigger fault-dump sequence
			[3] 0b0: Write 0b1 to trigger PROTECT function
			[2] 0b0: Write 0b1 to read one row of NVM for fault-dump
			[1] 0b1: Write 0b1 to store applicable register settings to the NVM
			[0] 0b0: Write 0b1 to reload applicable registers with existing NVM settings
0x01, 0x07, 0x0D, 0x13	DAC-X-MARGIN-HIGH	0xA680	[15:6] 0x29A: 10-bit data updates the MARGIN-HIGH code
			[5:0] 0b000000: Don't care
0x02, 0x08, 0x0E, 0x14	DAC-X-MARGIN-LOW	0x02C0	[15:6] 0x00B: 10-bit data updates the MARGIN-LOW code
			[5:0] 0b000000: Don't care

Pseudo Code Example

The following shows a pseudo code sequence to program the initial register values to the NVM of the DAC53204. The values given here are for the design choices made in the Design Notes.

Pseudo Code Example

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up voltage output on all channels, enables internal reference
WRITE COMMON-CONFIG(0x1F), 0x12, 0x49
//Configure GPI for Margin-High, Low function
WRITE GPIO-CONFIG(0x24), 0x01, 0xF5
//Write DAC margin high code (repeat for all channels)
WRITE DAC-0-MARGIN-HIGH(0x01), 0xA6, 0x80
//Write DAC margin low code (repeat for all channels)
WRITE DAC-0-MARGIN-LOW(0x02), 0x02, 0xC0
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

Design Featured Devices

Device	Key Features	Link
DAC53204	4-channel, 10-bit, VOUT and IOUT smart DAC with I^2C, SPI and Hi-Z out during power off	www.ti.com/product/DAC53204
DAC63204	4-channel, 12-bit, VOUT and IOUT smart DAC with I^2C, SPI and Hi-Z out during power off	www.ti.com/product/DAC63204
DAC43204	4-channel, 8-bit, VOUT and IOUT smart DAC with I^2C, SPI and Hi-Z out during power off	www.ti.com/product/DAC43204
DAC53004	Ultra-low-power, 4-channel, 10-bit, VOUT and IOUT smart DAC with I2C, SPI and Hi-Z out during power off	www.ti.com/product/DAC53004

Find other possible devices using the Parametric search tool.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, Smart DAC Python Examples
- Texas Instruments, DAC63204 Evaluation Module
- Texas Instruments, DAC63204 EVM User's Guide
- Texas Instruments, Precision Labs - DACs

For direct support from TI Engineers, use the E2E™ forums:

e2e.ti.com

Analog Engineer's Circuit

Voltage Margining and Scaling Circuit With Current Output Smart DAC

Smart DAC

Katlynne Jones

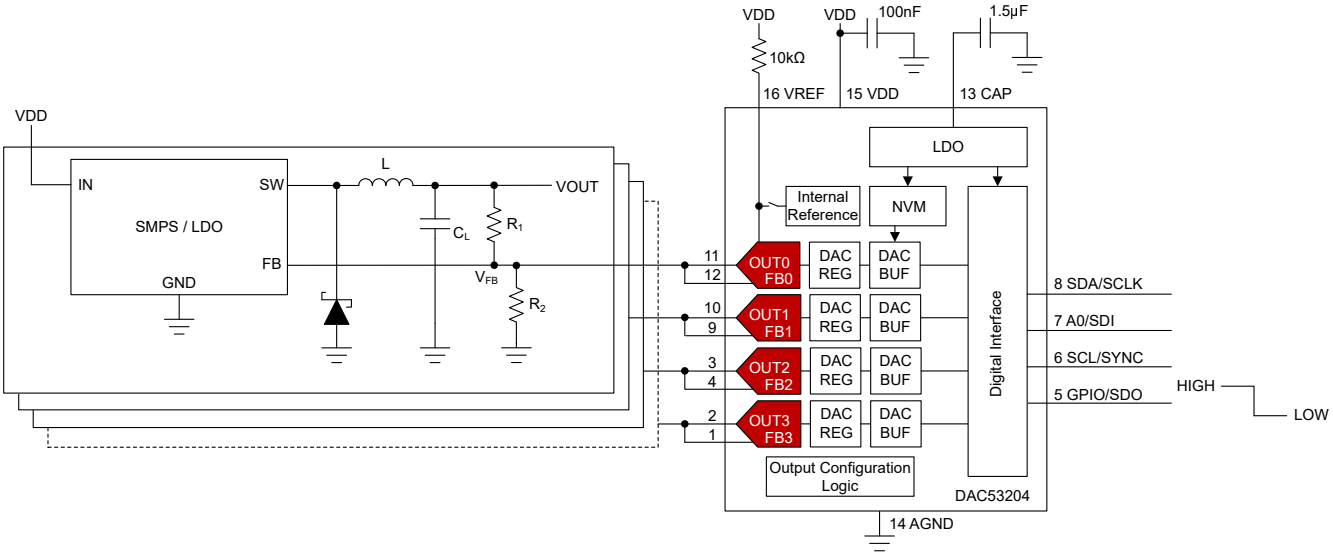
Design Objective

Key Input Parameter	Key Output Signal	Recommended Device
SPI or I^2C communication	±12µA analog DAC output, 3.3V ±10% SMPS output	DAC43204, DAC53204, DAC53004

Objective: *Provide a margin voltage for an SMPS output of ±10% the nominal value.*

Design Description

This circuit uses a four-channel buffered current output DAC to voltage margin a switch-mode power supply (SMPS). A voltage margining circuit is used to trim, scale, or test the output of a power converter. Adjustable power supplies, such as low dropout regulators (LDOs), DC/DC converters, or SMPS provide a feedback (FB) input that is used to control the desired output. A precision smart DAC, such as the DAC43204, provides linear control of the power supply output when the DAC is supplied and the output is powered on. Most DACs include an internal pulldown resistor at the voltage output when the DAC is supplied but the output is in power down mode. Also, when most DACs are completely powered off, the ESD cells on the output pin conduct current if the output is pulled away from ground which is the case in voltage margining circuits. The DAC43204 provides a high-impedance (Hi-Z) output when the DAC is powered off or when the output channel is in power down mode, meaning that the DAC draws very little current through the FB pin of the SMPS and the output is set at the nominal voltage. The DAC43204 has a general-purpose input (GPI) pin that allows the DAC output to be toggled between a high- and low-current output. This allows the SMPS to be toggled within ±10% of the nominal output value. All register settings can be saved using the non-volatile memory (NVM) on the DAC43204 meaning that the device can be used without a processor, even after a power cycle. This circuit can be used in applications such as communications equipment, enterprise systems, test and measurement, and general-purpose power-supply modules.



Design Notes

1. The *DACx3204 12-Bit, 10-Bit, and 8-Bit, Quad Voltage and Current Output Smart DACs With Auto-Detected I2C, PMBus™, or SPI Interface Data Sheet* recommends using a 100nF decoupling capacitor for the VDD pin and a 1.5µF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal LDO. Place these capacitors close to the device pins.
2. The nominal voltage of the SMPS is set by resistors R_1 and R_2. The SMPS uses an internal 600mV reference voltage at the FB pin to determine the voltage at the output. Calculate R_1 and R_2 using the following equations:

$$R_1 = \frac{V_{NOMINAL} - V_{FB}}{I_{NOMINAL}}$$

$$R_2 = \frac{R_1 \times V_{FB}}{V_{NOMINAL} - V_{FB}}$$

   A nominal current of 100µA through R_1 and R_2 and 3.3V nominal output voltage is used. With these values the equations become:

$$R_1 = \frac{3.3V - 0.6V}{100\mu A} = 27k\Omega$$

$$R_2 = \frac{27k\Omega \times 0.6V}{3.3V - 0.6V} = 6k\Omega$$

3. To achieve the desired margin, the DAC43204 must sink or source additional current through R_1. This current (I_{MARGIN}) is calculated by:

$$I_{MARGIN} = \frac{V_{NOMINAL} \times (1 + MARGIN) - V_{FB}}{R_1} - I_{NOMINAL}$$

   For a ±10% margin, the equation becomes:

$$I_{MARGIN} = \frac{3.3V \times (1 + 0.10) - 0.6V}{27k\Omega} - 100\mu A = 12\mu A$$

4. The DAC codes for $\pm I_{MARGIN}$ are stored in the DAC-MARGIN-HIGH and DAC-MARGIN-LOW registers. The codes programmed to these registers, in decimal, is calculated using:

$$DAC\_MARGIN\_HIGH = \frac{I_{DAC,MAX} - I_{MIN}}{I_{MAX} - I_{MIN}} \times 256$$

$$DAC\_MARGIN\_LOW = \frac{I_{DAC,MIN} - I_{MIN}}{I_{MAX} - I_{MIN}} \times 256$$

   Using an I_{OUT} range of ±25µA, the equation becomes:

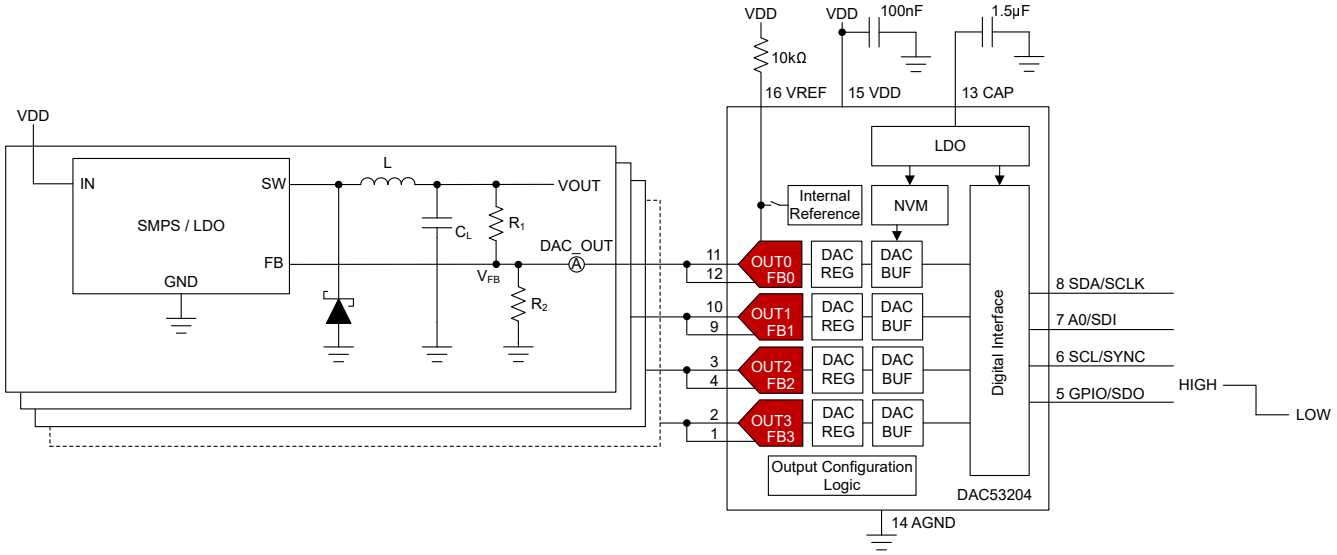
$$DAC\_MARGIN\_HIGH = \frac{12\mu A - (-25\mu A)}{25\mu A - (-25\mu A)} \times 256 = 189.44d$$

$$DAC\_MARGIN\_LOW = \frac{-12\mu A - (-25\mu A)}{25\mu A - (-25\mu A)} \times 256 = 66.56d$$

   This is rounded to 189d and 67d to give a $I_{DAC,MAX}$ of 11.9µA and a $I_{DAC,MIN}$ of –11.9µA.
5. In this design, GPI is used for Margin High, Low function. A high on GPI sets the DAC output to $I_{DAC,MAX}$ and the SMPS V_{OUT} to margin low, or 2.97V. A low on GPI sets the DAC output to $I_{DAC,MIN}$ and the SMPS V_{OUT} to margin high, or 3.63V.
6. The DAC43204 can be programmed with the initial register settings described in the Register Settings section using I^2C or SPI. Save the initial register settings in the NVM by writing a 1 to the NVM-PROG field of the COMMON-TRIGGER register. After programming the NVM, the device loads all registers with the values stored in the NVM after a reset or a power cycle.

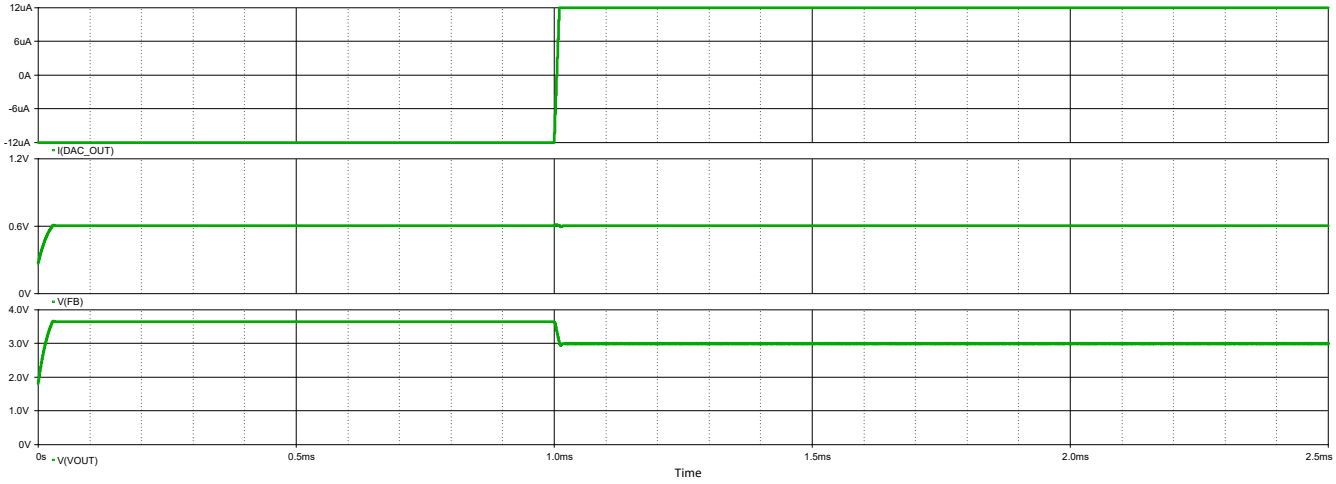
Design Simulations

This schematic is used for the following simulation of the DAC43204.



Transient Simulation Results

The simulation shows the SMPS output (V_{OUT}) responding to the changes on the DAC43204 output (DAC_OUT). When DAC_OUT is at $I_{DAC,MIN}$ the SMPS V_{OUT} goes to margin high, or 3.63V. When DAC_OUT is at $I_{DAC,MAX}$ the SMPS V_{OUT} goes to margin low, or 2.97V.



Register Settings

Register Settings for DAC43204 Voltage Margining

Register Address	Register Name	Setting	Description
0x1F	COMMON-CONFIG	0x1DB6	[15] 0b0: Write 0b1 to set window-comparator output to a latching output
			[14] 0b0: Write 0b1 to lock device. Unlock by writing 0b0101 to DEV-UNLOCK field in the COMMON-TRIGGER register
			[13] 0b0: Write 0b1 to set fault-dump read enable at address 0x01
			[12] 0b1: Enables the internal reference
			[11:10] 0b11: Powers-down VOUT3
			[9] 0b0: Powers-up IOUT3
			[8:7] 0b11: Powers-down VOUT2
			[6] 0b0: Powers-up IOUT2
			[5:4] 0b11: Powers-down VOUT1
			[3] 0b0: Powers-up IOUT1
			[2:1] 0b11: Powers-down VOUT0
			[0] 0b0: Powers-up IOUT0
0x24	GPIO-CONFIG	0x01F5	[15] 0b0: Write 0b1 to enable glitch filter on GPI
			[14] 0b0: Don't care
			[13] 0b0: Write 0b1 to enable output mode on GPIO pin
			[12:9] 0b0000: Selects the STATUS function setting mapped to GPIO as output
			[8:5] 0b1111: Enables GPI function on all channels
			[4:1] 0b1010: Selects GPI to trigger margin-high, margin-low
			[0] 0b1: Enables input mode for GPIO pin
0x20	COMMON-TRIGGER	0x0002	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11:8] 0b0000: Write 0b1010 to trigger a POR reset
			[7] 0b0: Write 0b1 to trigger LDAC operation if the respective SYNC-CONFIG-X bit in the DAC-X-FUNC-CONFIG register is 1
			[6] 0b0: Write 0b1 to set the DAC registers and outputs to zero-code or mid-code based on the respective CLR-SEL-X bit in the DAC-X-FUNC-CONFIG register
			[5] 0b0: Don't care
			[4] 0b0: Write 0b1 to trigger fault-dump sequence
			[3] 0b0: Write 0b1 to trigger PROTECT function
			[2] 0b0: Write 0b1 to read one row of NVM for fault-dump
			[1] 0b1: Write 0b1 to store applicable register settings to the NVM
			[0] 0b0: Write 0b1 to reload applicable registers with existing NVM settings
0x01, 0x07, 0x0D, 0x13	DAC-X-MARGIN-HIGH	0xBD00	[15:8] 0xBD: 8-bit data updates the MARGIN-HIGH code
			[7:0] 0x00: Don't care
0x02, 0x08, 0x0E, 0x14	DAC-X-MARGIN-LOW	0x4300	[15:8] 0x43: 8-bit data updates the MARGIN-LOW code
			[5:0] 0x00: Don't care

Pseudo Code Example

The following shows a pseudo code sequence to program the initial register values to the NVM of the DAC43204. The values given here are for the design choices made in the Design Notes.

Pseudo Code Example for GPI to PWM

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up current output on all channels, enables internal reference
WRITE COMMON-CONFIG(0x1F), 0x1D, 0xB6
//Configure GPI for Margin-High, Low function
WRITE GPIO-CONFIG(0x24), 0x01, 0xF5
//Write DAC margin high code (repeat for all channels)
WRITE DAC-0-MARGIN-HIGH(0x01), 0xBD, 0x00
//Write DAC margin low code (repeat for all channels)
WRITE DAC-0-MARGIN-LOW(0x02), 0x43, 0x00
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

Design Featured Devices

Device	Key Features	Link
DAC43204	4-channel, 8-bit, VOUT and IOUT smart DAC with I^2C, SPI and Hi-Z out during power off	www.ti.com/product/DAC43204
DAC53204	4-channel, 10-bit, VOUT and IOUT smart DAC with I^2C, SPI and Hi-Z out during power off	www.ti.com/product/DAC53204
DAC53004	Ultra-low-power, 4-channel, 10-bit, VOUT and IOUT smart DAC with I^2C, SPI and Hi-Z out during power off	www.ti.com/product/DAC53004

Find other possible devices using the Parametric search tool.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, Smart DAC Python Examples
- Texas Instruments, DAC63204 Evaluation Module
- Texas Instruments, DAC63204 EVM User's Guide
- Texas Instruments, Precision Labs - DACs

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Analog Engineer's Circuit

Negative Voltage Margining and Scaling Circuit With Voltage Output Smart DAC

Smart DAC

Katlynne Jones

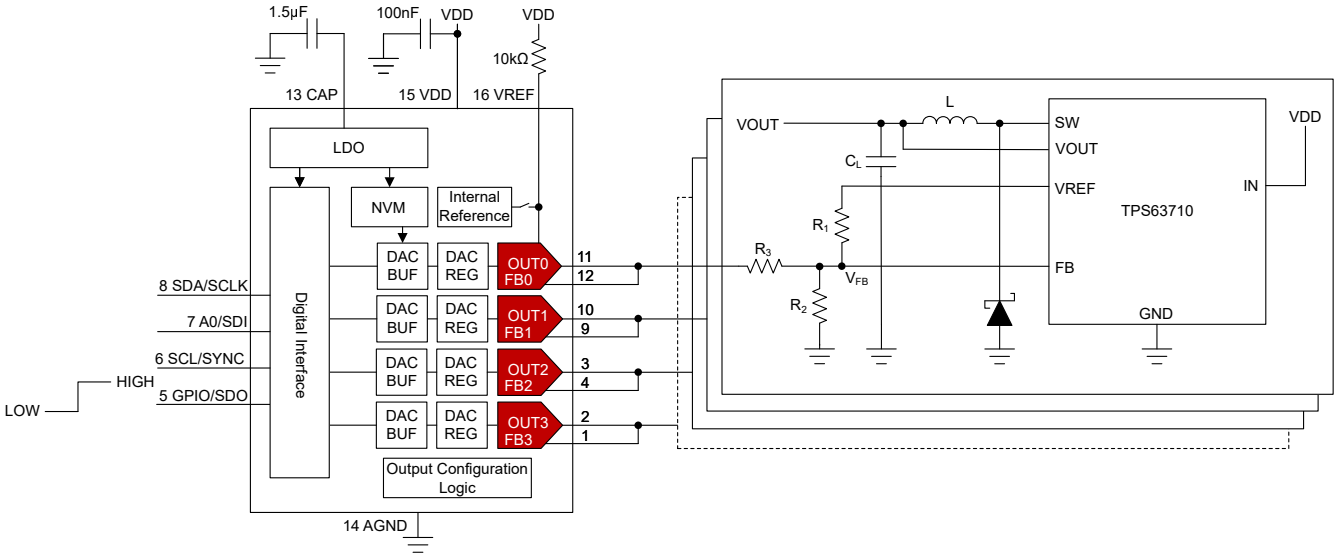
Design Objective

Key Input Parameter	Key Output Signal	Recommended Device
SPI or I^2C communication to control DAC voltage output	0-V to 1.2-V programmable current sink, –3.45 V ±26% DC/DC output	DAC63204W, DAC53204W, DAC63004W, DAC53004W, DAC63204, DAC53204, DAC43204, TPS63710

Objective: Margin a DC/DC output to ±26% the nominal value.

Design Description

This circuit uses a four-channel buffered voltage output DAC to margin an inverting step-down DC/DC converter. A voltage margining circuit is used to trim, scale, or test the output of a power converter. Adjustable power supplies, such as low dropout regulators (LDOs), DC/DC converters, or switch-mode power supplies (SMPS) provide a feedback (FB) pin that is used, along with a resistive voltage divider, to control the desired output. A precision smart DAC, such as the DAC63204W or DAC53204W (DACx3204W), provides linear control of the power supply output by using a series resistor to inject current into the voltage divider. The DACx3204 have a general-purpose input (GPI) pin that allows the DAC output to be toggled between a high and low voltage output. This allows the DC/DC to be toggled within ±26% of the nominal output value. All register settings are saved using the integrated non-volatile memory (NVM), enabling the device to be used without runtime software, even after a power cycle or reset. This circuit can be used in applications such as LIDAR, virtual reality headsets, and OLED TVs.



Design Notes

1. The *DACx3204W 12-Bit and 10-Bit, Quad Voltage and Current Output Smart DACs With Auto-Detected I2C, SPI, or PMBus® Interface in DSBGA Package* data sheet recommends using a 100-nF decoupling capacitor for the VDD pin and a 1.5-µF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal LDO. Place these capacitors close to the device pins.
2. Connect a 100-nF capacitor from the VREF pin to GND if the external reference is used. Ramp up the external reference after VDD. Connect a pullup resistor from the VREF pin to VDD if the external reference is not used. This example uses the internal reference and the VREF pin is pulled up to VDD with a 10-kΩ resistor.
3. The output voltage (V_{OUT}) of the TPS63710 when the DAC63204W is not connected or the current through the series resistor, R_3, is 0 A set by resistors R_1 and R_2. The TPS63710 uses an internal –700-mV reference voltage (V_{FB}) at the FB pin to determine V_{OUT}. The current through R_3 is 0 A when the DAC63204W output voltage (V_{DAC}) equals V_{FB}. The DAC63204W cannot output a negative voltage, so this design assumes that the DAC63204W output is always positive, and the TPS63710 is at the nominal output voltage when the DAC63204W is at midscale.
4. Choose R_3 so that V_{DAC} **>** –0.3 V when the DAC63204W is set to power-down mode. When the DAC63204W is configured in 10 kΩ to GND power-down mode, the 10-kΩ resistance creates a resistor divider with R_3. R_3 is chosen to be 200 kΩ in this example, making V_{DAC} equal to –0.038 V when in 10 kΩ to GND power down. Do not use Hi-z power-down mode when a negative voltage is connected to V_{DAC}.
5. Choose the current through R_2 (I_{R2}) so that the bias current into the FB pin of the TPS63710 is negligible. R_2 is calculated using:

$$R_2 = \frac{V_{FB}}{I_{R2}}$$

I_{R2} is chosen to be 5.2 µA. The TPS63701 has an internal gain factor of 1/0.9 which makes the effective V_{FB} –778 mV. R_2 is calculated to be:

$$R_2 = \frac{|-778\ \text{mV}|}{5.2\ \mu\text{A}} = 150\ \text{k}\Omega$$

6. The nominal TPS63710 V_{OUT} is chosen to be –3.45 V when V_{DAC} is at midscale, or 0.91 V. The current sourced from the DAC63204W output is calculated by:

$$I_{DAC} = \frac{V_{DAC} - V_{FB}}{R_3}$$

$$I_{DAC} = \frac{910\ \text{mV} + 778\ \text{mV}}{200\ \text{k}\Omega} = 8.44\ \mu\text{A}$$

R_1 can be calculated to achieve the desired nominal V_{OUT} using:

$$R_1 = \frac{V_{FB} - V_{OUT}}{I_{R2} - I_{DAC}}$$

$$R_1 = \frac{-0.778\ \text{V} + 3.45\ \text{V}}{5.2\ \mu\text{A} + 8.44\ \mu\text{A}} = 196\ \text{k}\Omega$$

7. The DAC63204W sinks or sources additional current through R_1 by adjusting V_{DAC} to achieve the desired margin. V_{DAC} is calculated by:

$$V_{DAC} = \left(I_{R2} - \frac{V_{OUT} - V_{FB}}{R_1}\right) \times R_3 + V_{FB}$$

$V_{DAC,MAX}$ and $V_{DAC,MIN}$ are configured to margin V_{OUT} by 26%. V_{OUT} low is –4.34 V and V_{OUT} high is –2.55 V

$$V_{DAC,\,MAX} = \left(-5.2\ \mu\text{A} - \frac{-4.34\ \text{V} + 0.778\ \text{V}}{196\ \text{k}\Omega}\right) \times 200\ \text{k}\Omega - 0.778\ \text{V} = 1.82\ \text{V}$$

$$V_{DAC,\,MIN} = \left(-5.2\ \mu\text{A} - \frac{-2.55\ \text{V} + 0.778\ \text{V}}{196\ \text{k}\Omega}\right) \times 200\ \text{k}\Omega - 0.778\ \text{V} = 0\ \text{V}$$

8. The DAC codes for $V_{DAC,MAX}$ and $V_{DAC,MIN}$ are stored in the DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers. $V_{DAC,NOM}$ is stored in the DAC-X-DATA register. The codes programmed to these registers, in decimal, is calculated using:

$$\text{DAC\_CODE} = \frac{V_{DAC} \times 2^{12}}{V_{REF}}$$

This design uses the internal 1.21-V reference with a gain of ×1.5 giving a full-scale voltage of 1.82 V. The equations become:

$$\text{DAC\_MARGIN\_HIGH} = \frac{1.82\ \text{V} \times 2^{12}}{1.82\ \text{V}} = 4096\text{d}$$

$$\text{DAC\_DATA} = \frac{0.91\ \text{V} \times 2^{12}}{1.82\ \text{V}} = 2048\text{d}$$

$$\text{DAC\_MARGIN\_LOW} = \frac{0\ \text{V} \times 2^{12}}{1.82\ \text{V}} = 0\text{d}$$

The maximum output code for a 12-bit device is 4095 so the $V_{DAC,MAX}$ becomes 1.819 V.

9. The TPS63710 requires that $V_{IN} \geq |V_{OUT}| / 0.7$. The max V_{OUT} for this application is –4.34 V, so the minimum V_{IN} is 6.2 V. 10 V is used in this design.
10. Using a 1.21-V reference with a ×1.5 gain and the 12-bit DAC63204W, the LSB size, or step size between each code, is about 443 µV. Using the lowest reference voltage possible decreases the LSB size and thus maximizes the resolution of $V_{DAC,MAX}$ and $V_{DAC,MIN}$.
11. The DAC63204W has a programmable slew-rate feature. The programmable slew is configured with the CODE-STEP-X and SLEW-RATE-X fields in the DAC-X-FUNC-CONFIG register. The programmable slew is only available when toggling between two values stored in the DAC-X-MARGIN-HIGH and DAC-X-MARGIN-LOW registers.

    CODE-STEP-X defines the number of LSB steps used to transition from the starting code to the final output code. SLEW-RATE-X defines the time-period for each code step. The slew time is calculated by:

$$t_{SLEW} = \text{SLEW\_RATE} \times \text{CEILING}\left(\frac{\text{MARGIN\_HIGH\_CODE} - \text{MARGIN\_LOW\_CODE}}{\text{CODE\_STEP}} + 1\right)$$

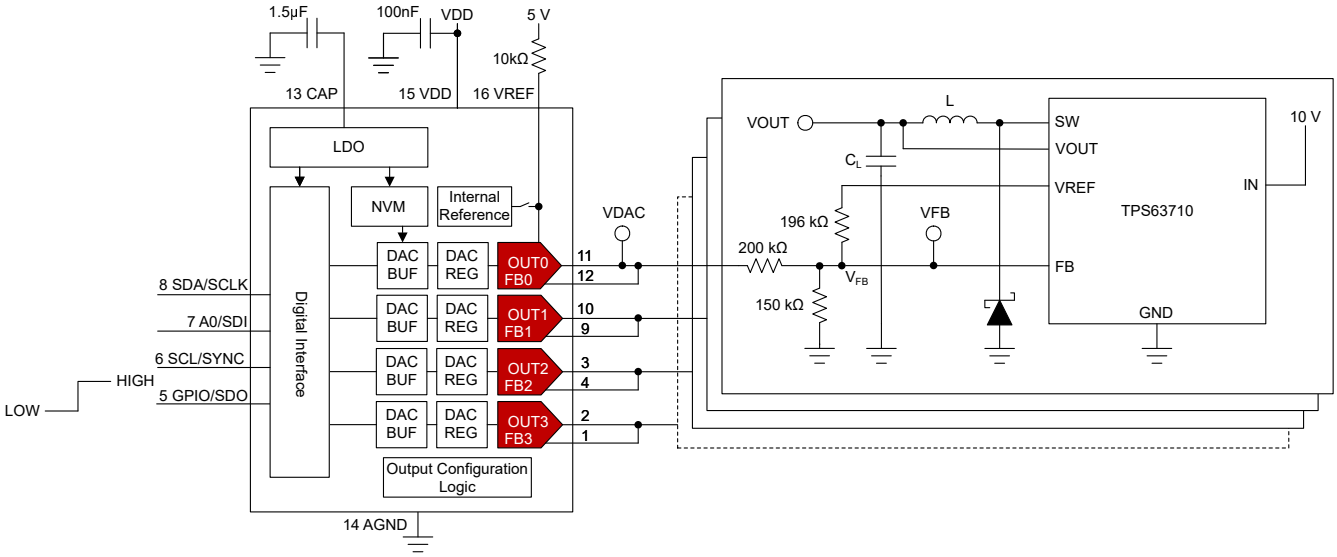
    This application uses a margin high code of 4095, margin low code of 0, SLEW-RATE of 1282 µs/LSB and a CODE-STEP of 1 LSB to achieve a 5.25-s slew time:

$$t_{SLEW} = 1282\ \left(\mu\text{s/LSB}\right) \times \text{CEILING}\left(\frac{4095 - 0}{1\ \text{LSB}} + 1\right) = 5.25\ \text{s}$$

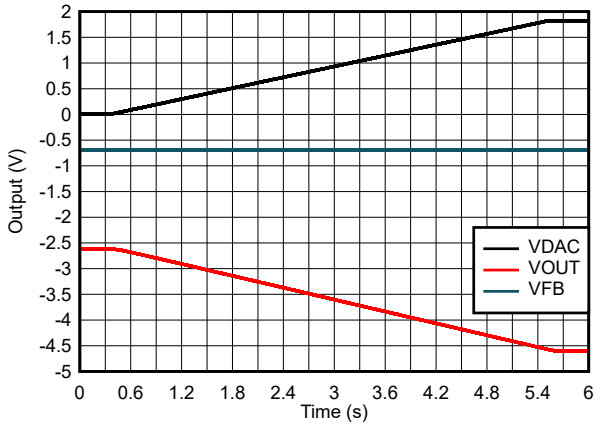
12. The GPIO pin can be configured as a digital input to switch the DAC63204W output between the margin high and margin low outputs with a programmable slew. The GPI-EN bit in the GPIO-CONFIG register enables the GPIO pin as an input. The GPI-CH-SEL field selects which channels are controlled by the GPI. The GPI-CONFIG field selects the GPI function. Write 0b1010 to the GPI-CONFIG field to configure the GPIO pin to trigger margin-high or margin-low functions.
    - A high on GPI sets the DAC output to $V_{DAC,MAX}$ and the TPS63710 V_{OUT} to low, or –4.34 V. A low on GPI sets the DAC output to $V_{DAC,MIN}$ and the TPS63710 V_{OUT} to high, or –2.55 V.
13. The DAC63204W can be programmed with the initial register settings described in the Register Settings section using I^2C or SPI. Save the initial register settings in the NVM by writing a 1 to the NVM-PROG field of the COMMON-TRIGGER register. After programming the NVM, the device loads all registers with the values stored in the NVM after a reset or a power cycle.

Design Results

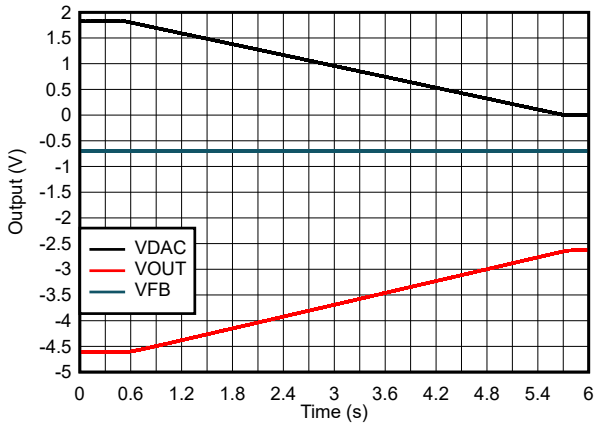
This schematic is used for the following design results of the DAC63204W. The V_{DAC}, V_{OUT}, and V_{FB} signals are measured on an oscilloscope at the test points marked on the schematic.



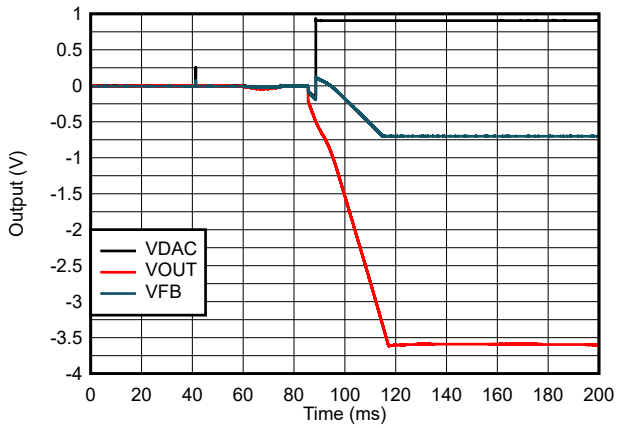
This plot shows the low-to-high transition of the DAC63204W output with the 5.25-s slew configured using the settings discussed in the Design Notes. The V_{DAC} output voltage slews from 0 V to 1.82 V which causes the TPS63710 V_{OUT} voltage to slew from –2.55 V to –4.34 V.



This plot shows the low-to-high transition of the DAC63204W output with the 5.25-s slew. The V_{DAC} output voltage slews from 1.82 V to 0 V which causes the TPS63710 V_{OUT} voltage to slew from –4.34 V to –2.55 V.



This plot shows the start-up behavior of the circuit. The 10-V TPS63710 supply and 5-V DAC63204W supply are switched on at the same time. The V_{DAC} output starts up to the nominal voltage of 910 mV. The TPS63710 V_{OUT} ramps to the nominal output of –3.45 V as the V_{FB} reference voltage starts up.



Register Settings

The following table shows an example register map for this application. The values given here are for the design choices made in the Design Notes section.

Register Settings for DAC63204W

Register Address	Register Name	Setting	Description
0x1F	COMMON-CONFIG	0x1249	[15] 0b0: Write 0b0 to set the window-comparator output to a non-latching output
			[14] 0b0: Device not locked
			[13] 0b0: Fault-dump read enable at address 0x00
			[12] 0b1: Enables the internal reference
			[11:10] 0b00: Powers up VOUT3
			[9] 0b1: Powers down IOUT3
			[8:7] 0b00: Powers up VOUT2
			[6] 0b1: Powers down IOUT2
			[5:4] 0b00: Powers up VOUT1
			[3] 0b1: Powers down IOUT1
			[2:1] 0b00: Powers up VOUT0
			[0] 0b1: Powers down IOUT0
0x24	GPIO-CONFIG	0x01F5	[15] 0b0: Glitch filter disabled for GP input
			[14] 0b0: Don't care
			[13] 0b0: Disable output mode for GPIO pin
			[12:9] 0b0000: Selects the STATUS function setting mapped to GPIO as output
			[8:5] 0b1111: Enables GPI function on all channels
			[4:1] 0b1010: GP input configured to trigger margin high or low
			[0] 0b1: Enables input mode for GPIO pin

Register Settings for DAC63204W (continued)

Register Address	Register Name	Setting	Description
0x20	COMMON-TRIGGER	0x0002	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11:8] 0b0000: Write 0b1010 to trigger a POR reset
			[7] 0b0: LDAC is not triggered
			[6] 0b0: DAC clear is not triggered
			[5] 0b0: Don't care
			[4] 0b0: Fault-dump is not triggered
			[3] 0b0: PROTECT function not triggered
			[2] 0b0: Fault-dump read not triggered
			[1] 0b1: Write 0b1 to store applicable register settings to the NVM
			[0] 0b0: NVM reload not triggered. Write 0b1 to reload applicable registers with existing NVM settings
0x03, 0x09, 0x0F, 0x15	DAC-X-VOUT-CMP-CONFIG	0x0800	[15:13] 0b000: Don't care
			[12:10] 0b010: Selects internal reference with ×1.5 gain
			[9:5] 0x00: Don't care
			[4] 0b0: Set OUTx pins as push-pull in comparator mode
			[3] 0b0: Comparator output consumed internally
			[2] 0b0: FBx input has high-impedance in comparator mode
			[1] 0b0: Comparator output not inverted
			[0] 0b0: Disable comparator mode
0x06, 0x0C, 0x12, 0x18	DAC-X-FUNC-CONFIG	0x000D	[15] 0b0: DAC-X clear mode set to zero-scale
			[14] 0b0: DAC-X output updates immediately after a write command
			[13] 0b0: Do not update DAC-X with broadcast command
			[12:11] 0b00: Phase set to 0°
			[10:8] 0b000: Selects sine wave mode
			[7] 0b0: Enable linear slew
			[6:4] 0b000: Selects 8 LSB CODE-STEP
			[3:0] 0xD: Selects 8 µs/step SLEW-RATE
0x01, 0x07, 0x0D, 0x13	DAC-X-MARGIN-HIGH	0xFFF0	[15:4] 0xFFF: 12-bit margin high code
			[3:0] 0x0: Don't care
0x02, 0x08, 0x0E, 0x14	DAC-X-MARGIN-LOW	0x0000	[15:4] 0x000: 12-bit margin low code
			[3:0] 0x0: Don't care

Pseudocode Example

The following shows a pseudocode sequence to program the initial register values to the NVM of the DAC63204W. The values given here are for the design choices made in the Design Notes section.

Pseudocode Example for DAC63204W

```
1:  //SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
2:  //Set gain setting to 1.5x internal reference (1.8 V) (repeat for all channels)
3:  WRITE DAC-0-VOUT-CMP-CONFIG(0x3), 0x08, 0x00
4:  //Power-up voltage output on all channels and enable the internal reference
5:  WRITE COMMON-CONFIG(0x1F),0x12, 0x49
6:  //Configure GPI for Margin-High, Low trigger for all channels
7:  WRITE GPIO-CONFIG(0x24), 0x01, 0xF5
8:  //Set slew rate and code step (repeat for all channels)
9:  //CODE_STEP: 1 LSB, SLEW_RATE: 1282 µs/step
10: WRITE DAC-0-FUNC-CONFIG(0x06), 0x00, 0x0D
11: //Write nominal DAC code (repeat for all channels)
12: //For a 1.8-V output range, the 12-bit hex code for 0.9 V is 0x800. With 16-bit left alignment,
13: this becomes 0x8000
14: WRITE DAC-0-DATA(0x19), 0x80, 0x00
15: //Write DAC margin high code (repeat for all channels)
16: //For a 1.8-V output range, the 12-bit hex code for 1.8 V is 0xFFF. With 16-bit left alignment,
17: this becomes 0xFFF0
18: WRITE DAC-0-MARGIN-HIGH(0x01), 0xFF, 0xF0
19: //Write DAC margin low code (repeat for all channels)
20: //The 12-bit hex code for 0 V is 0x000. With 16-bit left alignment, this becomes 0x0000
21: WRITE DAC-0-MARGIN-LOW(0x02), 0x00, 0x00
21: //Save settings to NVM
22: WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

Design Featured Devices

Device	Key Features	Link
DAC63204W	4-channel, 12-bit, VOUT and IOUT smart DAC with I^2C, SPI, and Hi-Z out during power off in DSBGA package	DAC63204W
DAC53204W	4-channel, 10-bit, VOUT and IOUT smart DAC with I^2C, SPI, and Hi-Z out during power off in DSBGA package	DAC53204W
DAC63004W	4-channel, 12-bit, VOUT and IOUT smart DAC with I^2C, SPI, and Hi-Z out during power off in DSBGA package	DAC63004W
DAC53004W	4-channel, 10-bit, VOUT and IOUT smart DAC with I^2C, SPI, and Hi-Z out during power off in DSBGA package	DAC53004W
TPS63710	Low Noise, 1 A Synchronous Inverting Buck Converter in 3x3 WSON Package	TPS63710

Find other possible devices using the Parametric search tool.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, *DAC63004WCSP-Evaluation Module*
- Texas Instruments, *DAC63004WCSP-EVM User's Guide*
- Texas Instruments, Precision Labs - DACs
- Texas Instruments, *TPS63710EVM-811*

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Analog Engineer's Circuit

High-Voltage Gain Stage Design Circuit for DAC81401

Design Goals

DAC V_{OUT}			Gain Stage		External Supply	
Range	MIN	MAX	MIN	MAX	HV+	HV–
0 V–20 V	0 V	20 V	0 V	80 V	0 V	82 V
±10 V	–10 V	+10 V	–40 V	+40 V	–41 V	+41 V

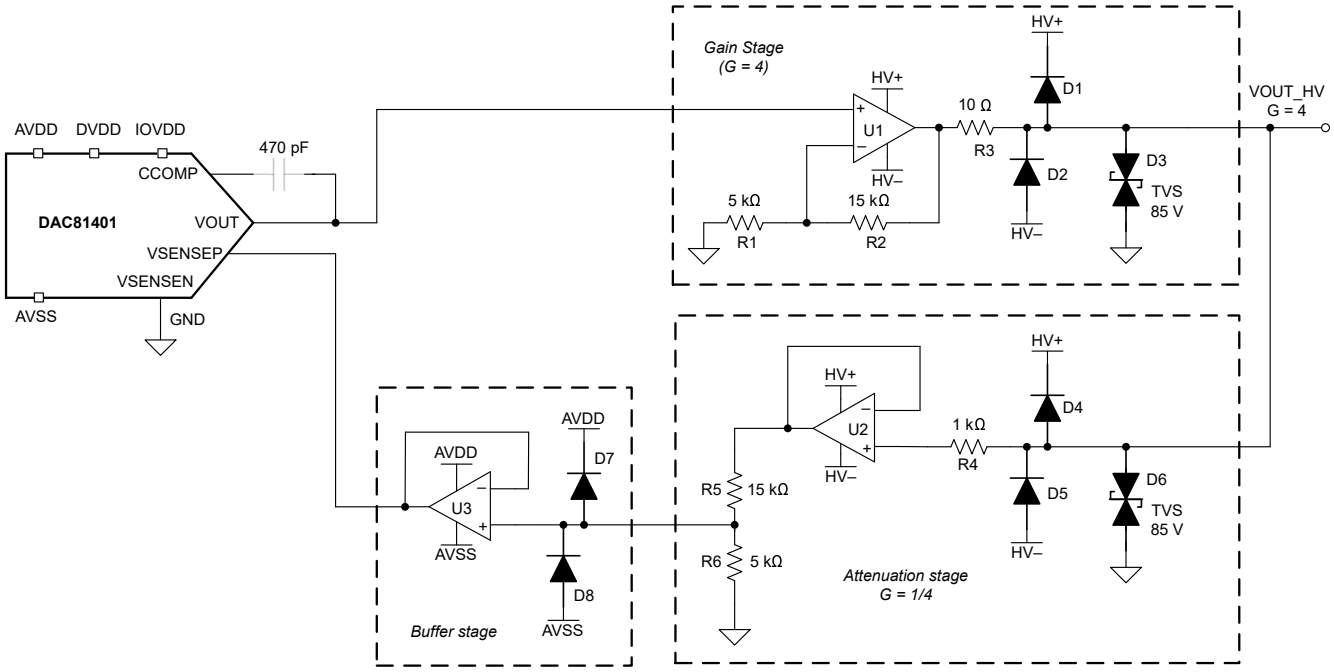
Objective: Design a high-voltage gain (4 ×) stage in a closed loop system for the DAC81401.

Design Description

This high-voltage gain stage design circuit for the DAC81401 is capable of providing output voltage ±40 V or 0 V to 80 V. This system design consists of four blocks as listed below and shown in *High-Voltage Gain Stage Circuit Block Diagram*.

- DAC81401 output stage
- High-voltage gain (4 ×) stage with protection diodes and TVS
- Attenuation stage
- Buffer stage with protection diodes

The DAC81401 output voltage is amplified by the gain stage by a factor of 4. The gain stage output is attenuated by the attenuation stage by a factor of 4. This attenuated output voltage is buffered and connected to the VSENSEP pin of the DAC81401 to close the loop.



High-Voltage Gain Stage Circuit Block Diagram

Key Components

- U1,U2 – OPA593: 85-V, low offset, low noise, 10 MHz, 250-mA output current precision operational amplifier
- U3 – OPA189: 36-V, low offset, low drift, low noise, 14-MHz precision operational amplifier
- D1, D2, D4, D5, D7, D8 – Schottky diode 100 V, 150 mA, 0.7-V forward voltage, fast switching
- D3, D6 – 85-V standoff voltage, high current, bidirectional TVS
- R1, R2 – low temperature coefficient and high accuracy (< 0.01%) thin film resistors
- R5, R6 – low temperature coefficient and high accuracy (< 0.01%) thin film resistors
- R3, R4 – normal thin film resistor

DAC81401 Output Stage

The DAC81401 output (V_{OUT}) is capable of providing from –20 V to +40 V. However, some applications (test and measurement, factory automation and control) requires even higher voltages. The high-voltage gain stage design is useful in these applications.

V_{OUT} is expressed by using the next two equations.

For unipolar mode:

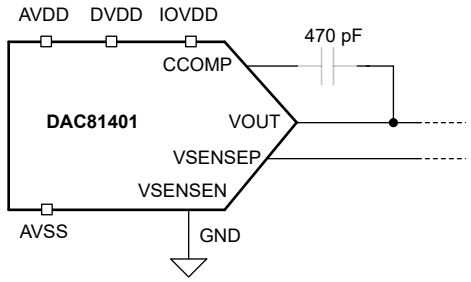
$$V_{OUT} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N}$$

For bipolar mode:

$$V_{OUT} = V_{REFIO} \times GAIN \times \frac{CODE}{2^N} - GAIN \times \frac{V_{REFIO}}{2^N}$$

where:

- CODE is the decimal equivalent of the code loaded to the DAC register
- N is the bits of resolution; 16-bits for DAC81401
- V_{REFIO} = 2.5 V is the reference voltage (internal or external)
- GAIN is the gain factor for each of the DAC814101 output voltage range, GAIN = 8 is recommended for this design



DAC81401 Output Stage Block Diagram

Compensation Capacitor

A 470-pF compensation capacitor is optional and the CCOMP pin can be left floating. This compensation capacitor is only needed if the load capacitor at the DAC81401 VOUT node is greater than 2 nF.

Adding the compensation capacitor increases the output settling time and slows the output voltage transient.

Gain Stage

The gain stage amplifies the DAC output voltage by 4 ×. This gain stage utilizes the OPA593 (U1) which supports an output voltage range of 85 V for single supply or ±42.5 V for bipolar supply. At the gain stage output (VOUT_HV), 0 V to 80 V or ±40 V can be obtained by programming the DAC output range to, 0 V to 20 V or ±10 V, respectively. For a given gain stage output (VOUT_HV), the DAC output can be calculated with the next two equations.

For unipolar mode:

$$\text{CODE} = \frac{\left(\frac{\text{VOUT\_HV}}{4}\right) \times 2^{\text{N}}}{\text{V}_{\text{REFIO}} \times \text{GAIN}}$$

For bipolar mode:

$$\text{CODE} = \frac{\left(\frac{\text{VOUT\_HV}}{4} + \text{GAIN} \times \frac{\text{V}_{\text{REFIO}}}{2^{\text{N}}}\right) \times 2^{\text{N}}}{\text{V}_{\text{REFIO}} \times \text{GAIN}}$$

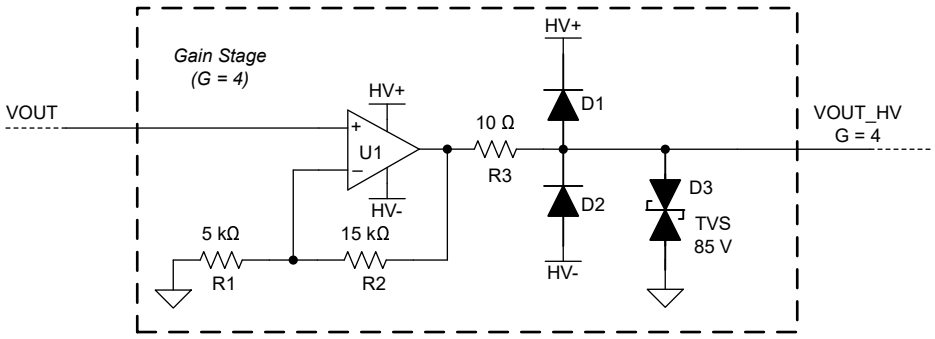
And for a given DC code, the gain stage output voltage can be calculated with the following equations.

For unipolar mode:

$$\text{VOUT\_HV} = 4 \times \left(\text{V}_{\text{REFIO}} \times \text{GAIN} \times \frac{\text{CODE}}{2^{\text{N}}}\right)$$

For bipolar mode:

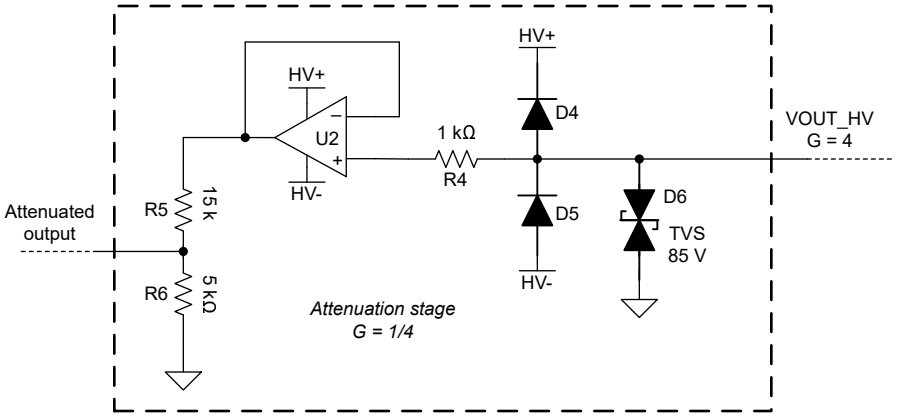
$$\text{VOUT\_HV} = 4 \times \left(\text{V}_{\text{REFIO}} \times \text{GAIN} \times \frac{\text{CODE}}{2^{\text{N}}} - \text{GAIN} \times \frac{\text{V}_{\text{REFIO}}}{2^{\text{N}}}\right)$$



Gain Stage Block Diagram

Attenuation Stage

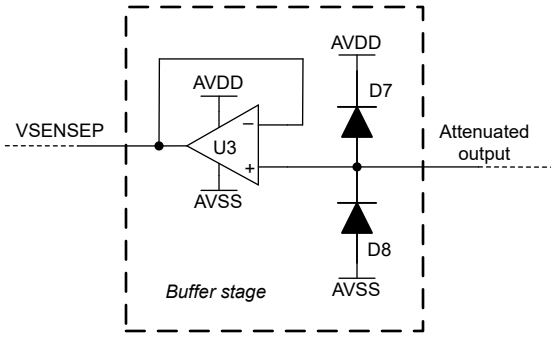
To avoid any unintended voltage drop due to load current (IR drop), VOUT and VSENSEP are connected close to the load, and the voltage value for the VSENSEP and VOUT is same. To remove the IR drop, the gain stage output voltage is – first buffered (U2) and then attenuated by a factor of 4 with resistor divider R5 and R6.



Attenuation Stage Block Diagram

Buffer Stage

The VSENSEP pin has an input impedance of about 50 kΩ and the resistor divider voltage cannot be connected directly or loading causes a voltage error. This voltage output is first buffered (U3) and then connected to the VSENSEP pin of DAC81401 to close the internal feedback loop with VOUT.



Buffer Stage Block Diagram

Design Accuracy

The gain stage output has an error contributed by mostly from:

- Offset voltage of U1 (OPA593): ±100 µV offset voltage of OPA593 has a small error contribution to the static device performance. The error contribution from offset voltage is calculated to be 0.00025 %FSR using the following equation, considering a 40-V span for the gain stage output.

$$\text{error (\%FSR)} = \frac{\text{offset voltage}}{\text{gain stage voltage span}} \times 100$$

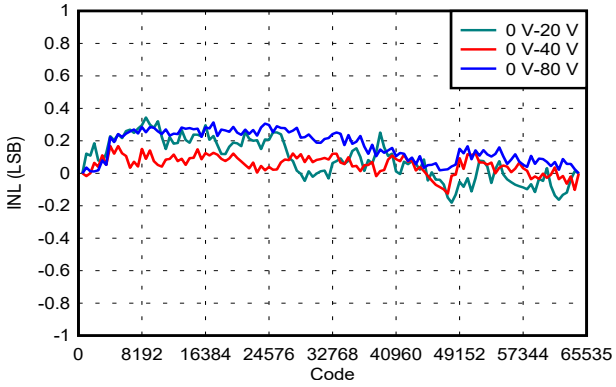
- Gain resistors R1 and R2 : Mismatch in ratio of R1 and R2 causes a gain error at the gain stage output. The error contribution due to mismatch in the ratio R1 and R2, is calculated to be 0.02 %FSR using the following equation.

$$\text{error (\%FSR)} = \left(1 - \frac{(1 \pm \Delta R2)}{(1 \pm \Delta R1)}\right) \times 100$$

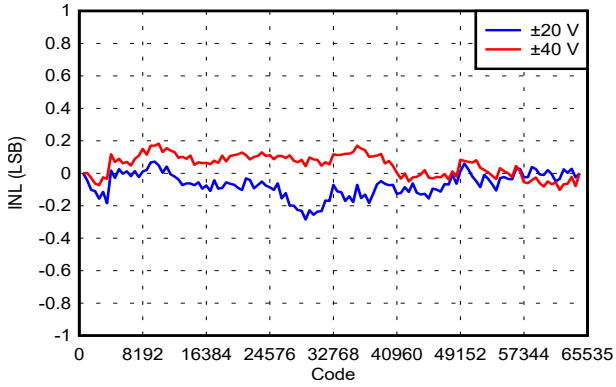
The calculated error contributions from U1, R1, and R3 show that the final gain stage output is just as accurate as the DAC81401.

Measurement Result

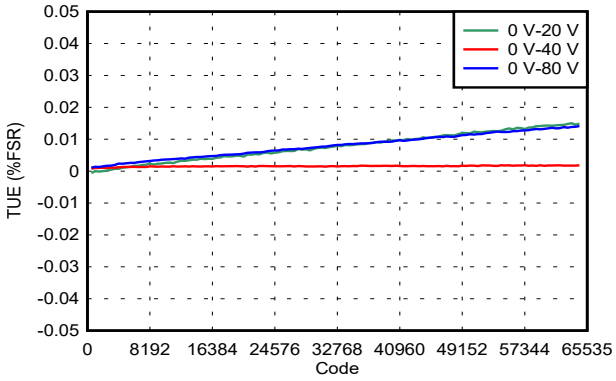
Integral nonlinearity (INL) and total unadjusted error (TUE) at the gain stage output were measured for different output voltage ranges. The INL and TUE plots from the next four images are measured for linear codes spans from code 512 to code 65024.



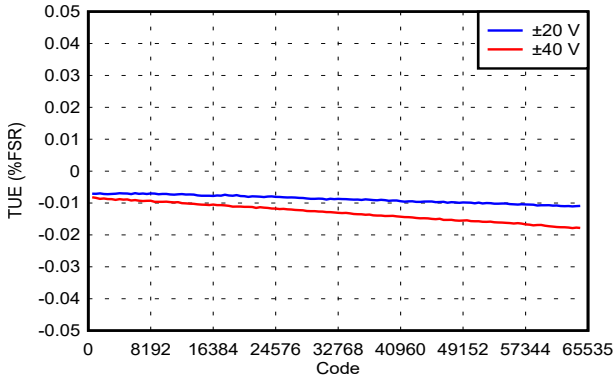
Integral Nonlinearity vs Digital Input Code – Unipolar Mode



Integral Nonlinearity vs Digital Input Code – Bipolar Mode



TUE vs Digital Input Code – Unipolar Mode



TUE vs Digital Input Code – Bipolar Mode

The DAC81401 voltage output range and corresponding gain stage voltage output range are listed in the following table.

DAC81401 VOUT Range	Gain Stage Voltage Range
0 V–5 V	0 V–20 V
0 V–10 V	0 V–40 V
0 V–20 V	0 V–80 V
±5 V	±20 V
±10 V	±40 V

Power Supply Requirement

An external high-voltage power supply is needed for the OPA593 in the gain stage (U1) and the attenuation stage (U2). The supplies also need to meet the headroom and footroom requirements as per the *OPA593 85-V, 250-mA Output Current, Precision, Power Op Amp* data sheet. These external power supplies need to be provided from a high-voltage supply source. Typical values used for HV+ and HV– are +41 V and −41 V or 81 V and 0 V, respectively.

$$\text{HV}- = \min\left(\text{VOUT}_{\text{HV}}\right) - \text{footroom}\left(\text{OPA593}\right)$$

$$\text{HV}+ = \max\left(\text{VOUT\_HV}\right) + \text{headroom}\left(\text{OPA593}\right)$$

Where VOUT_HV is output of the gain stage (U1) in the block diagram shown in *High-Voltage Gain Stage Circuit Block Diagram*.

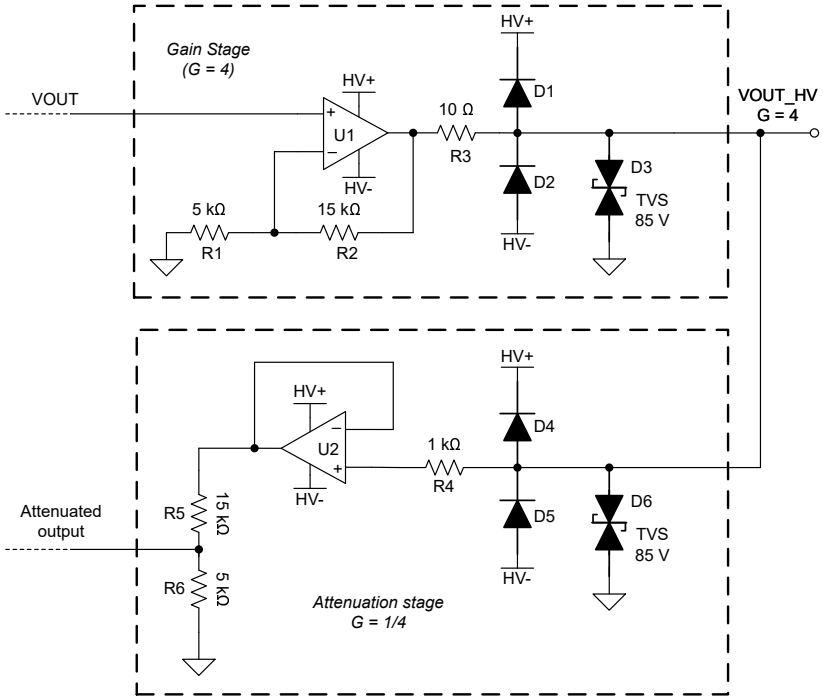
Set the DAC81401 power supply as recommended by the *DACx1401 Single-Channel, 16-Bit and 12-Bit, High-Voltage Output DACs With Precision Internal Reference* data sheet. AVDD and AVSS of the DAC81401 can be used for the V+ and V– power supply of the buffer stage operational amplifier (U3).

Overvoltage Stress (OVS) Protection Design

If the OPA593 (U1 and U2) output pins are exposed to industrial transient testing without external protection components, the internal diode structures of the DAC81401 becomes forward biased and conducts current. If the conducted current is large, as is common in high-voltage industrial transient tests, the structures can get permanently damaged and impact the device functionality.

The gain stage output and attenuation stage input includes an external electrical overstress protection circuit for short-circuit events. Protection is achieved by using the transient voltage suppressor (TVS) diodes D3 and D6 and clamp-to-rail diodes D1, D2, D4, and D5.

The combined protection from the TVS and clamp-to-rail diodes limits the current flowing into the device internal diode structures to prevent permanent damage. Considering R1 = 10 Ω and diode forward biased voltage is 0.7 V, the peak current entering to the device (U1 and U2) is 80 mA when the Schottky diode clamps VOUT to ±1.5 V from the rail. It is also important to connect the TVS diodes D3 and D6 to the gain stage output and attenuation stage input nodes to provide a discharge path for the energy sent to these nodes through diodes D3, D6, and the internal diode structures. R1 helps to limit the peak transient current or steady state current in case of incorrect bias voltage.



Protection Stage Block Diagram

Pseudocode Example

The following pseudocode sequence example:

- Powers up the DAC81401
- Enables the internal reference
- Enables the DAC channel
- Configures the voltage output range
- And sets the VOUT_HV output voltage

```
//Write these SPI commands after the device power supply is power configured

//Device power up
WRITE 0x0A04 to SPI_CONFIG register (0x03)
//Internal reference power up
WRITE 0x0000 to GEN_CONFIG register (0x04)
//DAC channel power up
WRITE 0xFFFE to DAC_PWDWN register (0x09)

//Configure the gain stage voltage output, default voltage range is 0 V to 20 V
//For 20 V span
WRITE 0x0000 to DACRANGE register (0x0A)
//For 5 V
WRITE 0x3FFF to DAC register (0x10)
//For 10 V
WRITE 0x7FFF to DAC register (0x10)
//For 15 V
WRITE 0xBFFF to DAC register (0x10)
//For 20 V
WRITE 0xFFFF to DAC register (0x10)
```

Design Featured Devices

Device	Key Features	Link
OPA593	85-V, Low offset, Low noise, 10 MHz, 250 mA output current precision operational Amplifier	OPA593
OPA189	36-V, Low offset, Low drift, Low noise, 14 MHz precision operational amplifier	OPA189

Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, DAC81401 Evaluation Module product page
- Texas Instruments, DAC81401 product page
- Texas Instruments, DAC81401 EVM User's Guide

For direct support from TI Engineers, use the E2E™ community:

e2e.ti.com

Analog Engineer's Circuit

Loop-Powered 4mA to 20mA Transmitter Circuit

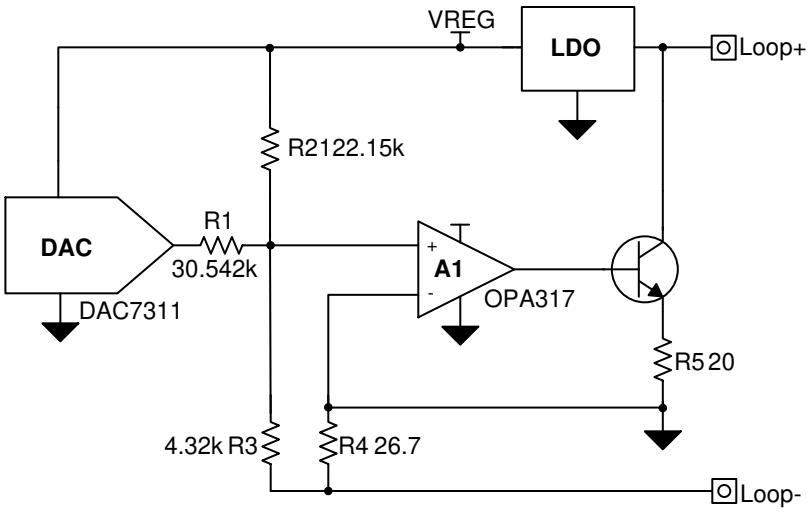
Garrett Satterfield

Design Goals

Loop Supply Voltage	DAC Output Voltage	Output Current	Error
12V–36V	0V–3V	4mA–20mA	<1% FSR

Design Description

The loop powered current transmitter regulates the current in series loop consisting of the power supply, transmitter, and load resistance. The active circuitry in the transmitter derives power from the loop current, meaning the current consumption of all devices must be less than the zero-scale current, which can be as low as 3.5mA in some applications. A regulator steps down the loop voltage to supply the DAC, op amp and additional circuitry. The op amp biases the transistor to regulate the current flowing from Loop+ to Loop-. The circuit is commonly used in 2-wire field sensor-transmitters such as Flow Transmitters, Level Transmitters, Pressure Transmitters, and Temperature Transmitters.



Design Notes

1. Select a single channel DAC with the required resolution and accuracy for the application. Use an op amp with low offset and low drift to minimize error.
2. Select a low power DAC, op amp, and voltage regulator to establish a total sensor-transmitter quiescent current of less than 4mA.
3. Minimize current flow through R1, R2, and R3 by selecting a large ratio of R3/R4 to minimize thermal drift of the resistors.
4. Use precision low drift resistors for R1-R4, R7-R8 to minimize error.
5. Use a voltage regulator with a wide input voltage range and low dropout voltage to allow for a wide range of loop supply voltages.

Design Steps

The output current transfer function is:

$$I_{OUT} = \left(\frac{V_{DAC}}{R1} + \frac{V_{REG}}{R2}\right)\left(\frac{R3}{R4} + 1\right)$$

1. Select a large ratio of R3/R4:

$$\frac{R3}{R4} = \frac{4.32k\Omega}{26.7\Omega}$$

2. Calculate R2 based on the zero-scale current (4mA), regulator voltage, and gain ratio (R3/R4).

$$R2 = \frac{V_{REG}}{I_{OUT,ZS}}\left(\frac{R3}{R4} + 1\right) = \frac{3V}{4mA}\left(\frac{4.32k\Omega}{26.7\Omega} + 1\right) = 122.10k\Omega$$

3. Calculate R1 to set the full-scale current based on the full-scale DAC voltage and current span of 16mA.

$$R1 = \frac{V_{DAC,FS}}{I_{OUT,SPAN}}\left(\frac{R3}{R4} + 1\right) = \frac{3V}{16mA}\left(\frac{4.32k\Omega}{26.7\Omega} + 1\right) = 30.524k\Omega$$

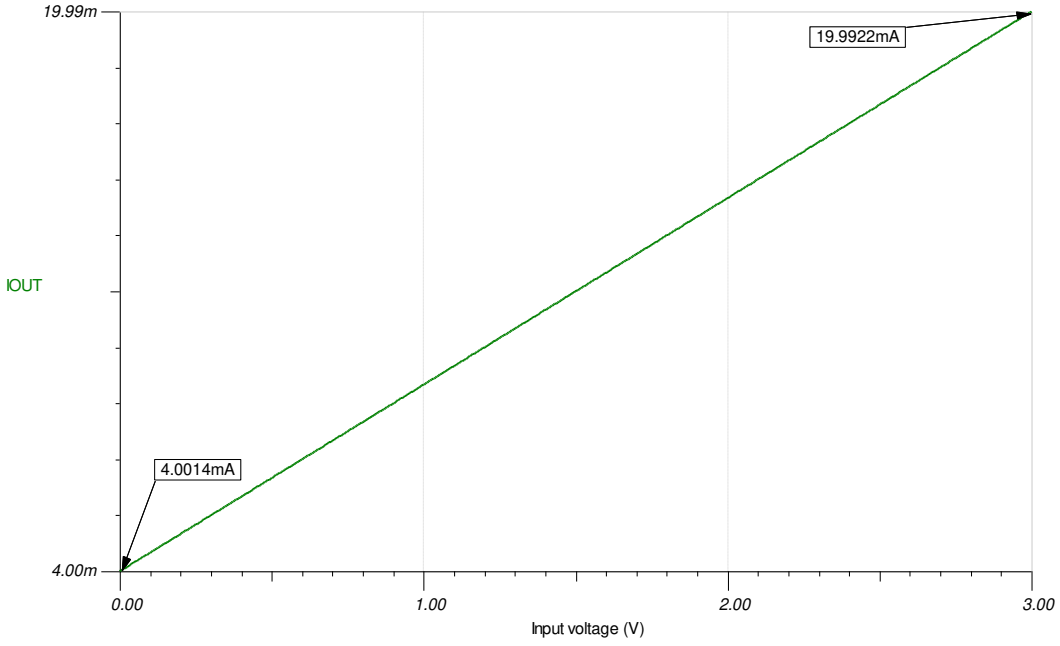
4. Calculate the zero-scale output current based on the chosen resistance values.

$$I_{OUT,ZS} = \frac{V_{REG}}{R2}\left(\frac{R3}{R4} + 1\right) = \frac{3V}{122.15k\Omega}\left(\frac{4.32k\Omega}{26.7\Omega} + 1\right) = 3.9983mA$$

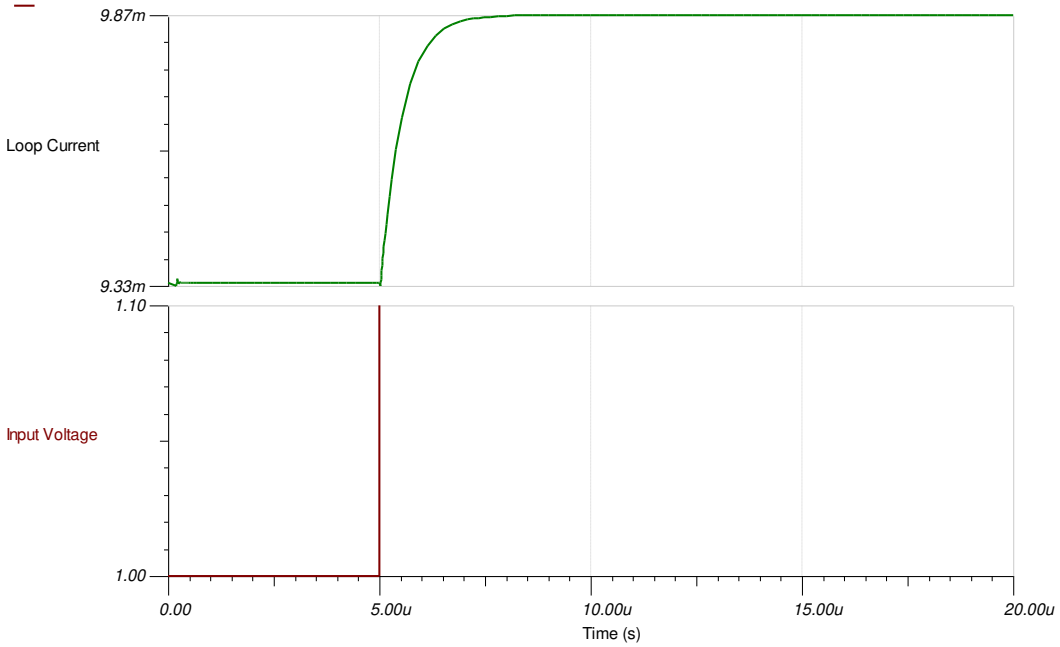
5. Calculate the full-scale current based on the chosen resistor values.

$$I_{OUT,FS} = \left(\frac{V_{DAC}}{R1} + \frac{V_{REG}}{R2}\right)\left(\frac{R3}{R4} + 1\right) = \left(\frac{3V}{30.542k\Omega} + \frac{3V}{122.15k\Omega}\right)\left(\frac{4.32k\Omega}{26.7\Omega} + 1\right) = 19.9891mA$$

DC Transfer Characteristic



Small Signal Step Response



Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC7311	12-bit resolution, single channel, ultra-low power, 1 LSB INL, SPI, 2V to 5.5V supply	12-bit, single-channel, ultra-low power DAC in 6-pin SC70 package for battery powered applications	Precision DACs (≤10 MSPS)
DAC8560	16-bit resolution, single channel, internal reference, low power, 4 LSB INL, SPI, 2V to 5.5V supply	16bit, Single Channel, 80uA, 2.0V-5.5V DAC in SC70 Package	Precision DACs (≤10 MSPS)
DAC8830	16-bit resolution, single channel, ultra-low power, unbuffered output, 1 LSB INL, SPI, 2.7V to 5.5V supply	16-bit, single-channel, ultra-low power, voltage output DAC	Precision DACs (≤10 MSPS)
DAC161S997	16-bit, 4-20mA current output, 100uA supply current, SPI, 2.7V to 3.3V supply	16-Bit Precision DAC With Internal Reference and 4mA-to-20mA Current Loop Drive	Precision DACs (≤10 MSPS)
Amplifiers			
TLV9001	Low-Power, 0.4mV Offset, Rail-to-Rail I/O, 1.8V to 5.5V supply	One-channel, 1-MHz rail-to-rail input and output 1.8-V to 5.5-V operational amplifier	Operational amplifiers (op amps)
OPA317	Zero-Drift, Low-Offset, Rail-to-Rail I/O, 35uA supply current max, 2.5V to 5.5V supply	Low Offset, Rail-to-Rail I/O Operational Amplifier	Operational amplifiers (op amps)
OPA333	microPower, Zero-Drift, Low Offset, Rail-to-Rail I/O, 1.8V to 5.5V supply	Micropower, 1.8-V, 17-µA zero-drift CMOS precision operational amplifier	Operational amplifiers (op amps)

Links to Key Files

Texas Instruments, *Low Cost Loop-Powered 4-20mA Transmitter EMC/EMI Tested*, TIPD158 reference design

Texas Instruments, *4-20mA Current Loop Transmitter*, TIDA-00648 reference design

Texas Instruments, *Highly-Accurate, Loop-Powered, 4mA to 20mA Field Transmitter with HART® Modem*, TIDA-01504 reference design

Texas Instruments, source files for SLAA866, SLAC782 software support

Trademarks

All trademarks are the property of their respective owners.

Analog Engineer's Circuit

Programmable Low-Side Current Sink Circuit

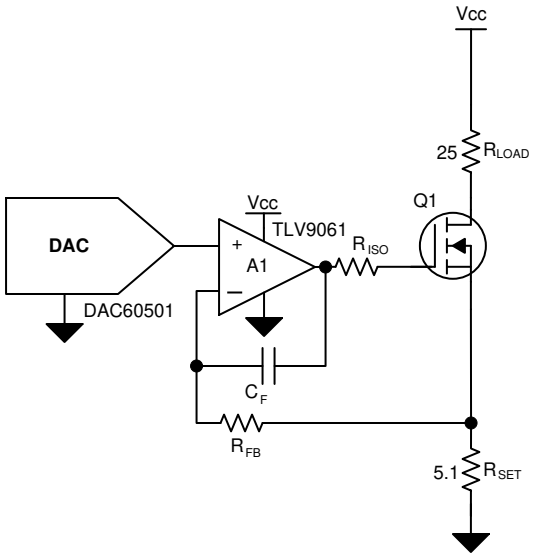
Garrett Satterfield

Design Goals

VCC	DAC Output Voltage	Output Current	Error	Maximum Resistive Load
5V	0mV – 510mV	0mA – 100mA	<0.25% FSR	44.9Ω

Design Description

The programmable low-side current sink sets the current through a load based on the DAC output voltage. The current is sensed through R_{SET} and the op amp biases a transistor regulate the current through the load. Components C_F, R_{ISO}, and R_{FB} provide compensation to verify the stability of the circuit.



Design Notes

1. Choose a DAC with low offset error, gain error, and drift. Use RRIO op amps to reduce error near the rails and maximize resistive load drive. Choose an op amp with low offset voltage to minimize error.
2. Use a high-precision, low-drift resistor for R_{SET} for accurate current regulation.
3. R_{SET} should be minimized for efficiency and power dissipation. Most of the power dissipation should occur through R_{LOAD}
4. To drive large R_{LOAD}, use a separate high voltage supply for driving the current to the load.

Design Steps

1. Calculate the R_{SET} value for the maximum DAC output voltage and desired maximum output current.

$$R_{SET} = \frac{V_{DAC,max}}{I_{OUT,max}} = \frac{510mV}{100mA} = 5.1\Omega$$

2. The maximum resistive load is given by:

$$R_{LOAD,max} = \frac{Vcc - I_{SET,max}R_{SET}}{I_{SET,max}} = \frac{5V - 100mA \times 5.1}{100mA} = 44.9\Omega$$

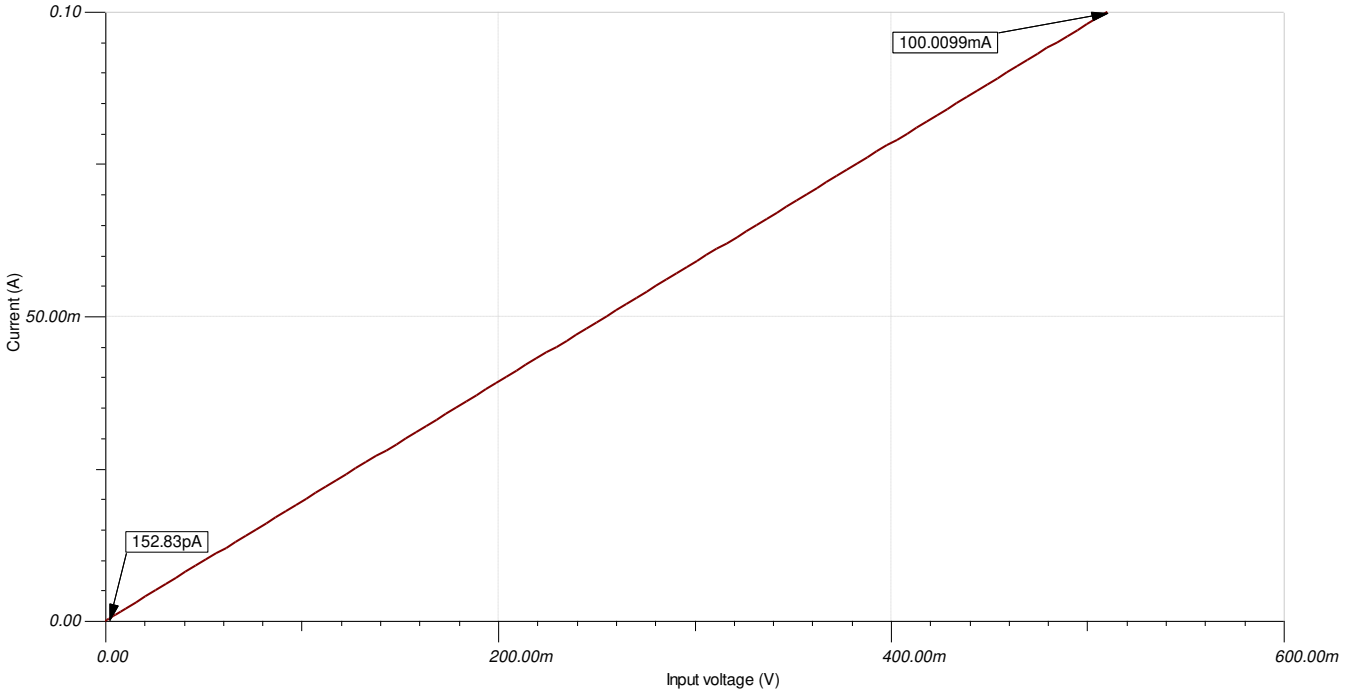
3. Verify that Q1 is rated for the power dissipation at maximum current.

$$P_{Diss,Q2} = Vcc \times I_{SET,max} - I_{SET,max}^2 \times (R_{LOAD} + R_{SET}) = 5V \times 100mA - 100mA^2 \times (25\Omega + 5.1\Omega) = 0.2W$$

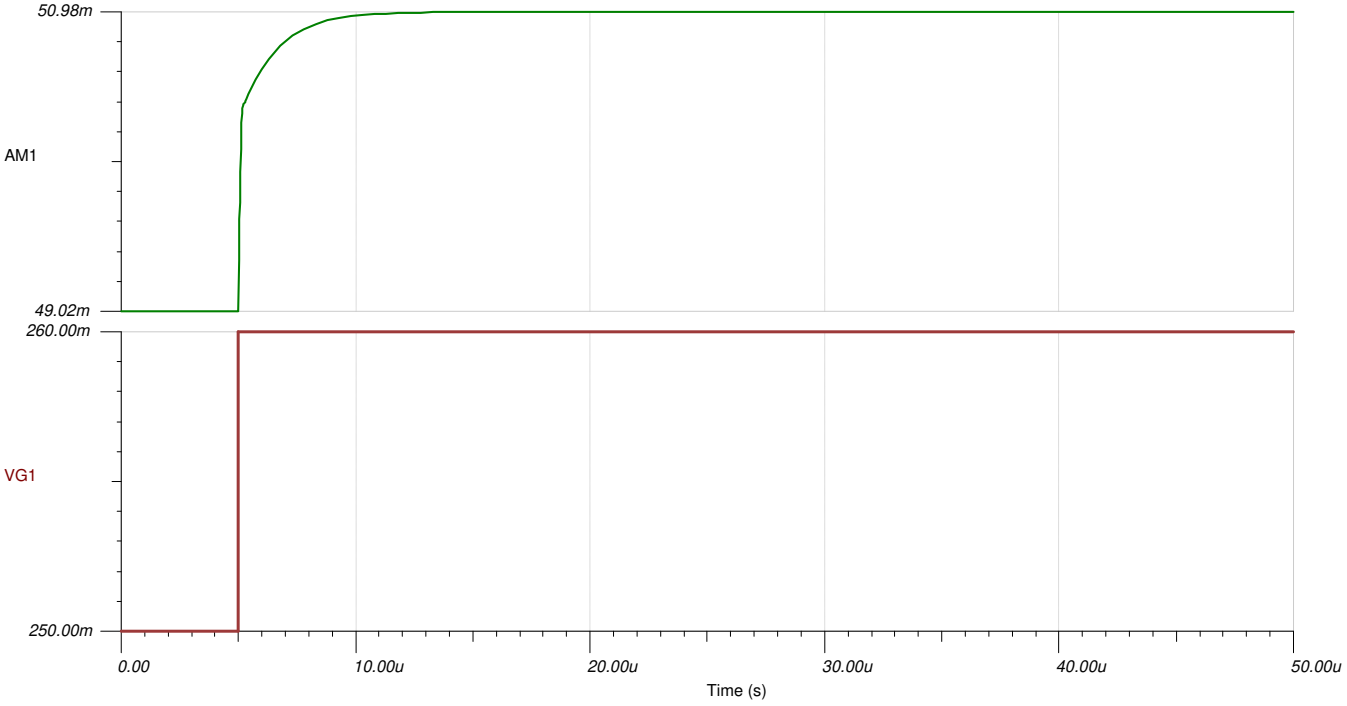
4. The output error can be approximated based on DAC TUE, amplifier offset voltage, resistor tolerance, and reference initial accuracy using root sum square (RSS) analysis.

$$\text{Output TUE(\%FSR)} = \sqrt{TUE_{DAC}^2 + \left(\frac{V_{OS,Amplifier}}{FSR} \times 100\right)^2 + Tol_{R_{SET}}^2 + Accuracy_{Ref}^2} = \sqrt{0.1^2 + \left(\frac{0.3mV}{510mV} \times 100\right)^2 + 0.1^2 + 0.1^2} = 0.183\% \text{ FSR}$$

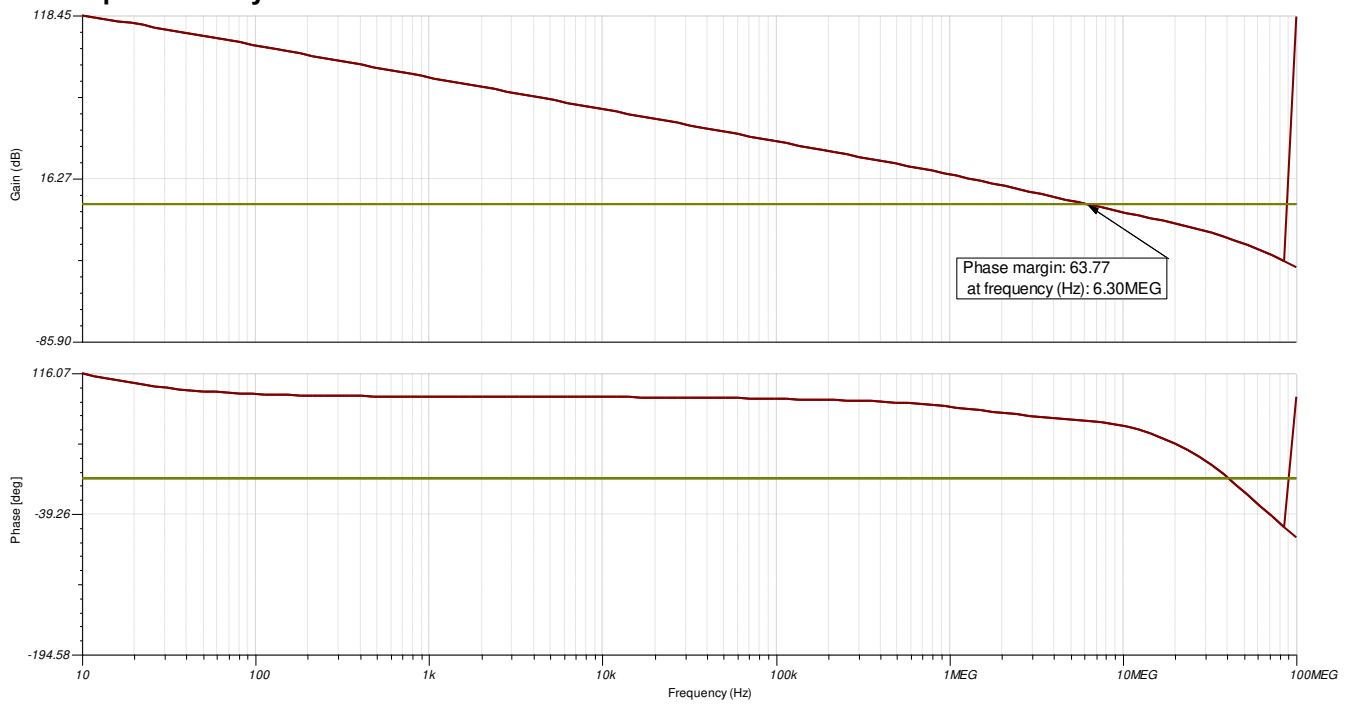
DC Transfer Characteristic



Small Signal Step Response



AC Loop Gain Analysis



Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC60501	12-bit resolution, 1LSB INL, Single-Channel, Voltage Output DAC with 5ppm/°C Internal Reference	True 12-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Precision DACs (≤10 MSPS)
DAC80501	16-bit resolution, 1LSB INL, Single-Channel, Voltage Output DAC with 5ppm/°C Internal Reference	True 16-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Precision DACs (≤10 MSPS)
DAC8830	16-bit resolution, single channel, ultra-low power, unbuffered output, 1 LSB INL, SPI, 2.7V to 5.5V supply	16-bit, single-channel, ultra-low power, voltage output DAC	Precision DACs (≤10 MSPS)
Amplifiers			
TLV9061	Ultra-Small, 0.3-mV Offset, Rail-to-Rail I/O, 1.8V to 5.5V supply	Single, 5.5V, 10MHz, RRIO operational amplifier for cost-optimized applications	Operational amplifiers (op amps)
OPA317	Zero-Drift, Low-Offset, Rail-to-Rail I/O, 35-µA supply current max, 2.5V to 5.5V supply	Low Offset, Rail-to-Rail I/O Operational Amplifier	Operational amplifiers (op amps)
OPA388	Precision, Zero-Drift, Zero-Crossover, Low Noise Rail-to-Rail I/O, 2.5V to 5.5V supply	Single, 10MHz, CMOS, zero-drift, zero-crossover, true RRIO precision operational amplifier	Operational amplifiers (op amps)

Trademarks

All trademarks are the property of their respective owners.

Analog Engineer's Circuit

Programmable, Two-Stage, High-Side Current Source Circuit

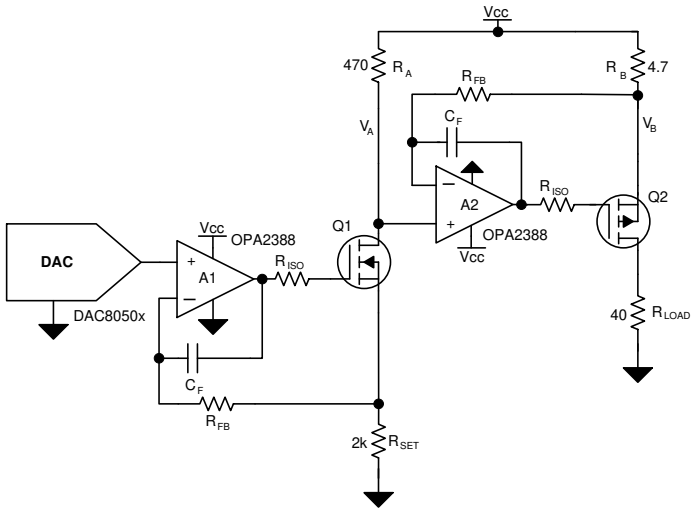
Garrett Satterfield

Design Goals

Supply Voltage (V_{CC})	DAC Output Voltage	Output Current	Error	Max Load Resistance	Compliance Voltage
5V	0V–2V	0–100mA	<1% FSR	45Ω	4.5V

Design Description

The programmable high-side current source supplies an adjustable current to a ground reference load. The first op amp stage sets a reference current based on the DAC output voltage. The second op amp stage acts as a current mirror that gains the reference current and regulates the current sourced from the output PMOS to the load. R_{SET}, RA, and RB set the output current based on the DAC voltage. Components C_{COMP}, R_{ISO}, and R_{FB} provide compensation to verify the stability of the circuit. Common end equipment that utilize this circuit include *PLC Analog Output Modules*, *Field Transmitters*, *Digital Multimeters, Printers, Optical Modules, LED Drivers,* and *EPOS.*



Design Notes

1. Choose a DAC with low offset, gain, and drift errors. Use RRIO op amps to maintain low compliance voltage and op amps with low offset should be selected.
2. Minimize the current flow through R_A, Q1, and $R_{SET}$by selecting a large ratio of R_A:R_B to maximize efficiency while also minimizing heating and drift in the first stage.
3. Use high-precision, low-drift resistors for R_{SET}, R_A, and R_B to minimize error caused by resistor mismatch and temperature drift.
4. Minimize the resistance of R_B to maximize compliance voltage.
5. Avoid placing Q2 near thermally sensitive components in layout as the power dissipation causes heating.

Design Steps

1. Set the reference current in the sink stage by selecting R_{SET} based on V_{DAC}. Minimize the reference current as it flows directly to ground and reduced efficiency. Set the reference current to 1mA and calculate R_{SET}.

$$R_{SET} = \frac{V_{DAC,max}}{I_{SET}} = \frac{2V}{1mA} = 2k\Omega$$

2. Select the required gain ratio based on the desired output current and I_{OUT}/I_{SET} = 100mA/1mA = 100, this is the required ratio of R_A:R_B.
3. Calculate the maximum value of R_B from the maximum allowable voltage drop to drive the maximum current through the maximum load.

$$R_B < \frac{V_{CC} - I_{OUT,max}R_{LOAD,max}}{I_{OUT,max}} = \frac{5V - 0.1A \times 45\Omega}{0.1A} = 5\Omega$$

4. The voltage V_A is $V_{CC} – I_{SET}xR_A$ which is equal to the voltage V_B due to the op amp feedback. Select R_A to achieve a voltage drop of <500mV to maintain the desired compliance voltage. A standard resistance of 4.7Ω is chosen.

$$V_A = V_B$$

$$R_A = \frac{V_{CC} - V_A}{I_{SET}} = \frac{470mV}{1mA} = 470\Omega$$

5. Calculate R_B based on R_A and the gain selected in step 2.

$$R_B = \frac{R_A}{100}$$

6. Verify the power dissipation of Q2. The power dissipation of Q2 based on the load is given by:

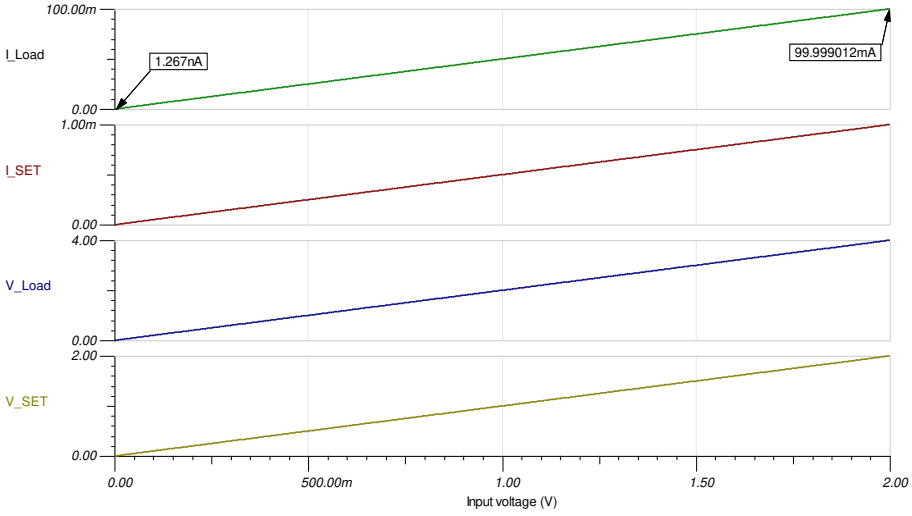
$$P_{Diss,Q2} = V_{CC} \times I_{OUT} - I_{OUT}^2 \times (R_{LOAD} + R_B) = 5V \times 0.1A - 0.1A^2 \times (40\Omega + 4.7\Omega) = 0.053W$$

The maximum power dissipation of Q2 occurs when the load resistance is zero:

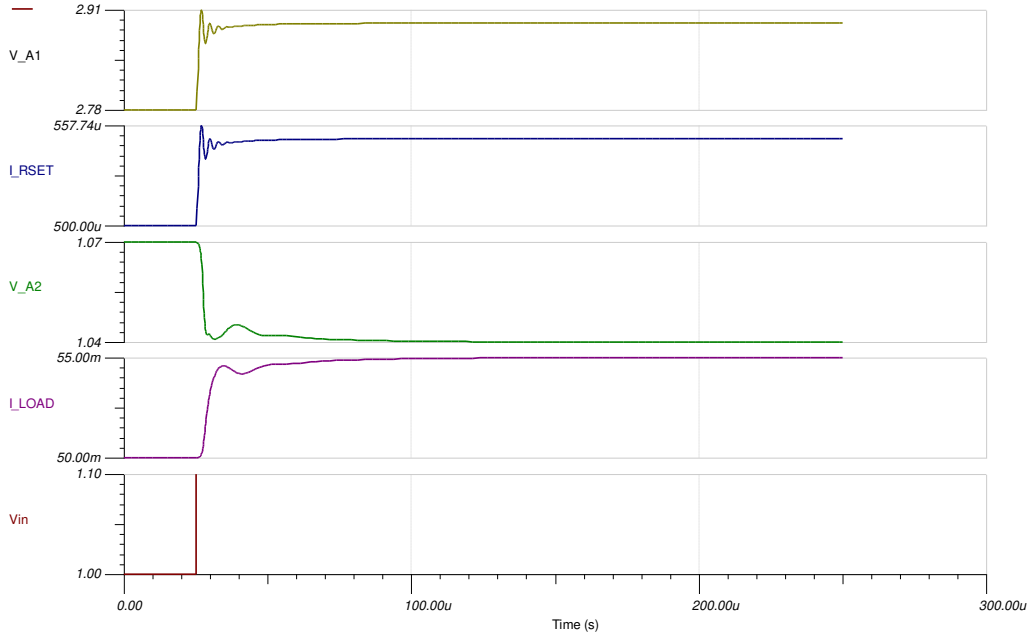
$$P_{Diss,Q2,max} = V_{CC} \times I_{OUT} - I_{OUT}^2 \times R_B = 5V \times 0.1A - 0.1A^2 \times 4.7 = 0.453W$$

Confirm that Q2 is rated for this power dissipation.

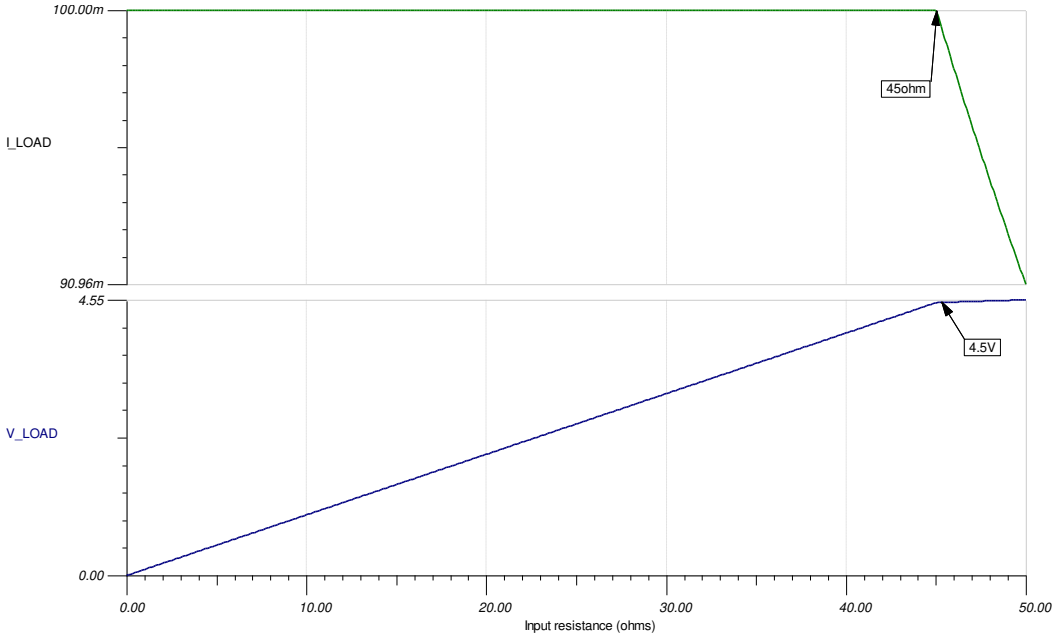
DC Transfer Characteristics



Small-Signal Step Response



Compliance Voltage



High Voltage Supply Modification

This circuit design example uses a low voltage supply for V_{CC}. Some applications, such as 4mA – 20mA current loops, require a high voltage supply to drive large resistive loads. To modify this current source for higher voltage supply, choose a high voltage, rail-to-rail input/output amplifier such as OPA192.

Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC80501	16-bit resolution, 1LSB INL, Single-Channel, Voltage Output DAC with 5ppm Internal Reference	True 16-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Precision DACs (≤10 MSPS)
DAC80508	16-bit resolution, 1LSB INL, Octal-Channel, Voltage Output DAC with 5ppm Internal Reference	True 16-bit, 8-channel, SPI, voltage-output DAC with precision internal reference	Precision DACs (≤10 MSPS)
DAC8775	16-bit resolution, Quad-Channel, ±10V, ±24mA Voltage and Current Output DAC, with Integrated DC/DC Converter	16-Bit Quad-Channel Programmable Current-Output and Voltage-Output Digital-to-Analog Converter (DAC)	Precision DACs (≤10 MSPS)
Amplifiers			
OPA388	Precision, Zero-Drift, Zero-Crossover, Rail-to-Rail Input/Output, 2.5V to 5.5V Supply	Single, 10-MHz, CMOS, zero-drift, zero-crossover, true RRIO precision operational amplifier	Operational amplifiers (op amps)
OPA192	Precision, High-Voltage, Rail-to-Rail Input/Output, 4.5V to 36V Supply	High-Voltage, Rail-to-Rail Input/Output, 5μV, 0.2μV/˚C, Precision Operational Amplifier	Operational amplifiers (op amps)
TLV170	Cost Sensitive, Rail-to-Rail Output, 2.7V to 36V Supply	Single, 36V, 1.2MHz, low-power operational amplifier for cost-sensitive applications	Operational amplifiers (op amps)

Links to Key Files

Texas Instruments, *High side V-I converter reference design from 0V to 2V and 0mA to 100mA, 1% full-scale error*, TIPD102 overview

Texas Instruments, *Less Than 1-W, Quad-Channel, Analog Output Module With Adaptive Power Management Reference Design*, TIPD215 overview

Texas Instruments, 8-channel, 16-bit, 200mA current output DAC, reference design

Texas Instruments, source files for SLAA867, software support

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Analog Engineer's Circuit

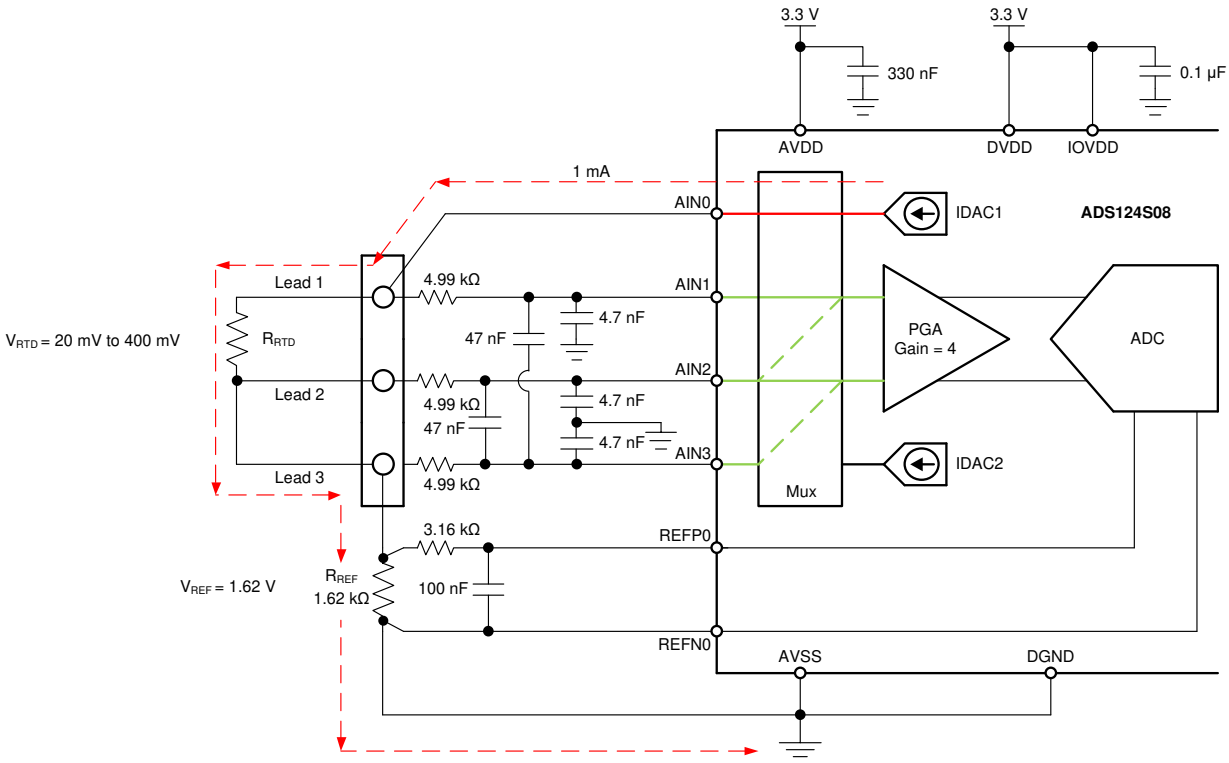
Three-Wire PT100 RTD Measurement Circuit With Low-Side Reference and One IDAC Current Source

Joseph Wu

Power Supplies		
AVDD	**AVSS, DGND**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD with a low-side reference using the ADS124S08. In comparison to a *Three-Wire PT100 RTD Measurement Circuit With Low- Side Reference and Two IDAC Current Sources* with a single measurement, this design uses a single IDAC excitation current source and a second measurement to remove the lead resistance error. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.
7. This design shows connections to four input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The three-wire RTD measurement offers more accuracy than comparable two-wire RTD measurements but also gives better immunity from the IDAC current mismatch than with a three-wire RTD measurement using matched IDAC current sources. For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   Start with a design where the excitation current is driven into lead 1 of the RTD, flowing through the RTD, and out the RTD through lead 3. At this point, ignore the lead resistance error, so that the measurement from AIN1 to AIN2 only measures the RTD resistance.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01°C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

$V_{AIN1} = I_{IDAC1} \cdot (R_{RTD} + R_{REF}) = 1mA \cdot (400\Omega + 1620\Omega) = 2.02V$

$V_{AIN2} = I_{IDAC1} \cdot R_{REF} = 1mA \cdot 1620\Omega = 1.62V$

$V_{INMAX} = 1mA \cdot 400\Omega = 400mV$

3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As shown in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the absolute input voltage must satisfy the following:

   $AVSS + 0.15V + [|V_{INMAX}| \cdot (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0V + 0.15V + [|V_{INMAX}| \cdot (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0.75V < V_{AIN1}, V_{AIN2} < 2.55 V$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02V and 1.62V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

   $0V < V_{AIN0} < 2.7V$

   With the previous result, the output compliance of the IDAC is satisfied.

4. Use two different measurements to measure the RTD resistance and cancel the lead-resistance error.

   The first measurement of the ADC is measured across AIN1 and AIN2, with the lead resistances included.

   $\text{Measurement 1} = V_{AIN1} - V_{AIN2} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})$

   Because the IDAC current does not pass through lead 2, its resistance is never part of the measurement. The input multiplexer of the ADC is then set to make a second measurement across AIN2 and AIN3. This measures the voltage drop across the resistance from lead 3.

   $\text{Measurement 2} = V_{AIN2} - V_{AIN3} = I_{IDAC1} \cdot R_{LEAD3}$

   Measurement 2 is subtracted from measurement 1 to get the following result.

   $\text{Measurement 1} - \text{Measurement 2} = [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] - (I_{IDAC1} \cdot R_{LEAD3})$

   If the lead resistances are equal, then the lead-resistance error drops out to get the final result.

   $\text{Measurement 1} - \text{Measurement 2} = I_{IDAC1} \cdot R_{RTD}$

5. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are

selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10 kΩ, to allow for proper input sampling for the ADC.

With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

$$f_{IN\_DIFF} = 1 / [2 \cdot \pi \cdot C_{IN\_DIFF} (R_{RTD} + 2 \cdot R_{IN})]$$

$$f_{IN\_CM} = 1 / [2 \cdot \pi \cdot C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$$

For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5kHz.

The bandwidth for the reference input filtering is approximated in the following equation.

$$f_{REF} = 1 / [2 \cdot \pi \cdot C_{REF} \cdot (R_{REF} + R_{IN\_REF})]$$

For the reference input filtering, R_{IN_REF} = 3.16kΩ and C_{REF_DIFF} = 100nF. This sets the reference filter bandwidth to 330Hz. Because REFN0 is set to ground, the common-mode filtering is removed. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC. First, the result from measurement 1 is shown.

$$\text{Output Code 1} = 2^{23} \cdot \text{Gain} \cdot [(V_{RTD} + V_{LEAD1}) / V_{REF}] = 2^{23} \cdot \text{Gain} \cdot [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot [(R_{RTD} + R_{LEAD1}) / R_{REF}]$$

$$R_{RTD} + R_{LEAD1} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{23})]$$

Then the result from measurement 2 is shown.

$$\text{Output Code 2} = 2^{23} \cdot \text{Gain} \cdot (V_{LEAD3} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC1} \cdot R_{LEAD3}) / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot (R_{LEAD1} / R_{REF})$$

$$R_{LEAD3} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{23})]$$

If the lead resistances are assumed to be equal, then the subtract the result of measurement 2 from measurement 1 to get the equivalent RTD resistance.

$$R_{RTD} = R_{REF} \cdot [(\text{Output Code 1} - \text{Output Code 2}) / (\text{Gain} \cdot 2^{23})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Three-Wire PT100 RTD Measurement Circuit with Low-Side Reference and One IDAC Current Source Using the ADS124S08

Register Address	Register Name	Setting	Description
02h(1)	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	12h	Positive reference buffer enabled, negative reference buffer disabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation
02h(2)	INPMUX	23h	Select AINP = AIN2 and AINN = AIN3

(1) This input multiplexer setting is for measurement 1.
(2) This input multiplexer setting is for measurement 2, as a measurement of the lead-resistance error.

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
Send 06;// RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;// Configure the device
Send 42// WREG starting at 02h address
05// Write to 6 registers
12// Select AINP = AIN1 and AINN = AIN2
0A// PGA enabled, Gain = 4
14// Continuous conversion mode, low-latency filter, 20-SPS data rate
12// Positive reference buffer enabled, negative reference buffer disabled
  // REFP0 and REFN0 reference selected, internal reference always on
07// IDAC magnitude set to 1mA
F0;// IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low; // For verification, read back configuration registers
Send 22// RREG starting at 02h address
05// Read from 6 registers
00 00 00 00 00 00;// Send 6 NOPs for the read
Set CS high;
Set CS low;
Send 08;// Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
{
Set CS low;// Configure the device for measurement 1
Send 42// WREG starting at 02h address
00// Write to 1 register
12;// Select AINP = AIN1 and AINN = AIN2
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
```

```
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
Set CS low;// Configure the device for measurement 2
Send 42// WREG starting at 02h address
00// Write to 1 register
23;// Select AINP = AIN2 and AINN = AIN3
Set CS high;
Wait for DRDY to transition low;
Set CS low;
Send 12// Send RDATA command
00 00 00;// Send 3 NOPs (24 SCLKs) to clock out data
Set CS high;
Subtract measurement 2 from measurement 1;// Remove lead-resistance error
}
Set CS low;
Send 0A;//STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*
- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2020) to Revision B (September 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1

Changes from Revision * (December 2018) to Revision A (March 2020)	Page
• Changed schematic to remove filtering from REFN0	1
• Changed bandwidth calculation for reference input filter	1
• Changed Register Settings Table to disable negative reference buffer	1
• Changed Pseudo Code Example to disable negative reference buffer	1

Analog Engineer's Circuit

High-Current Voltage Output Circuit Using a Precision DAC

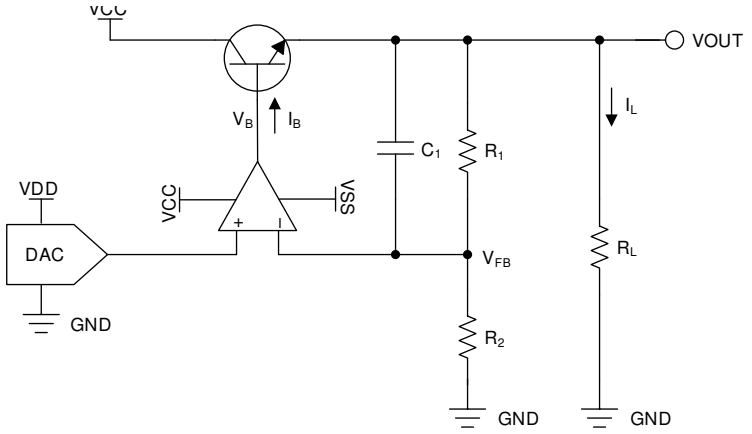
Uttama Kumar Sahu

Design Goals

Power Supply	DAC Output	Voltage Output	Current Output
VCC: 24V, VSS: –5V, VDD: 5V	0V to 2.5V	0V to 5V	0A to 10A

Design Description

High-current voltage output can be obtained from a digital-to-analog converter (DAC) using a power amplifier at the DAC output. To have additional flexibility with amplifier performance like accuracy, bandwidth, and higher current, the circuit as shown in the following figure is an excellent choice. For example, power amplifiers typically have much higher output offset error compared to a precision amplifier. The DAC programs the output voltage along with the gain of the amplifier. The amplifier maintains the output voltage using negative feedback. The high current to the load is provided by the transistor. This circuit is useful in applications where components must be tested with different AC or DC voltage excitation such as *memory and semiconductor test equipment*, *LCD test equipment*, and others.



Design Notes

1. Choose a DAC with the required resolution and output range.
2. Choose an op amp with low offset and low drift to minimize error. Choose a part with sufficient gain-bandwidth product (GBW), as required by the output signal.
3. Choose R_1 and R_2 such that the desired output voltage is met along with the DAC output voltage, along with tolerance which maintains the desired accuracy.
4. Choose the compensation capacitor C_1 such that it is larger than the input capacitance of the op-amp inputs.
5. Choose a transistor that can provide the required load current and has a high h_{FE} so that the base current is sufficiently smaller than the output current limit of the op amp. A bipolar-junction transistor (BJT) Darlington pair or a high-power metal-oxide semiconductor field-effect transistor (MOSFET) are preferable.

Design Steps

1. The DAC80501 device is a 16-bit, single-channel, high-performance precision DAC. The DAC80501 device is specified monotonic, by design, and offers excellent linearity of less than 1LSB. These devices include a 2.5V, 5ppm/°C internal reference, giving full-scale output voltage ranges of 1.25V, 2.5V, or 5V.
2. The OPA227 operational amplifier combines low noise and wide bandwidth with high precision to make it the best choice for applications requiring both AC and precision DC performance. The OPA227 device is unity-gain stable and features high slew rate (2.3V/µs) and wide bandwidth (8MHz).
3. The transfer function of the output voltage is given by:

$$V_{OUT} = V_{DAC}\left(1 + \frac{R_1}{R_2}\right)$$

   To get an output voltage of 5V with a DAC output of 2.5V, for example, chose both R_1 and R_2 as 10kΩ. This keeps the quiescent current through the feedback network as 5V / 20kΩ = 250µA. This current works for this design because this design is for a high-output current. In case the output current is lower, the resistance values can be increased so that the quiescent current is negligible, compared to the output current.
4. The base current, I_B, for the transistor for a given load current I_L is given by:

$$I_B = \frac{I_C}{h_{FE}} = \frac{1}{h_{FE}}\left(I_L + \left(\frac{V_{OUT}}{R_1 + R_2}\right)\right)$$

   To get a maximum load current of 10A, the collector current (I_C) of the transistor is approximately 10A (ignoring 250-µA quiescent current). To keep I_B less than 20mA, keep h_{FE} greater than (10A / 20mA) = 500
5. In general, compensation capacitor C_1 is not set by fixed equations, but rather by choosing values while observing the output small-signal step response. Through simulation in this example, select $C_1 \geq 22pF$.

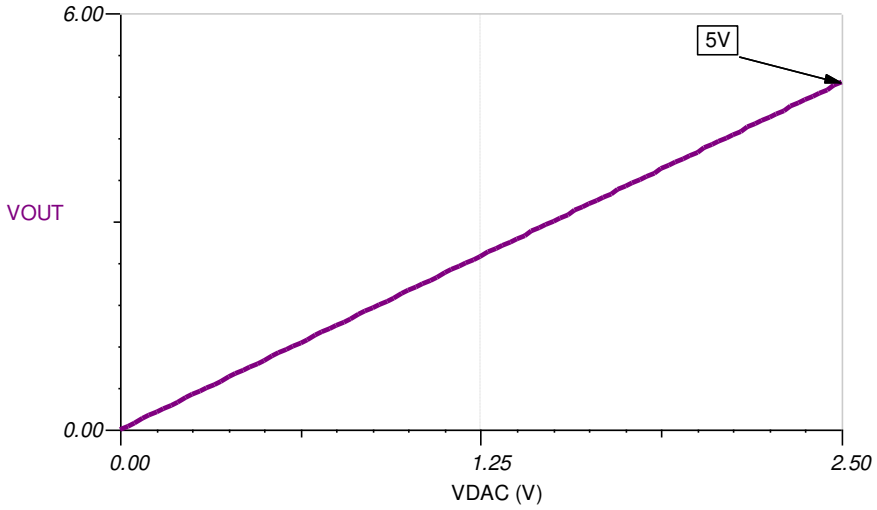


Figure 1-1. DC Transfer Characteristics

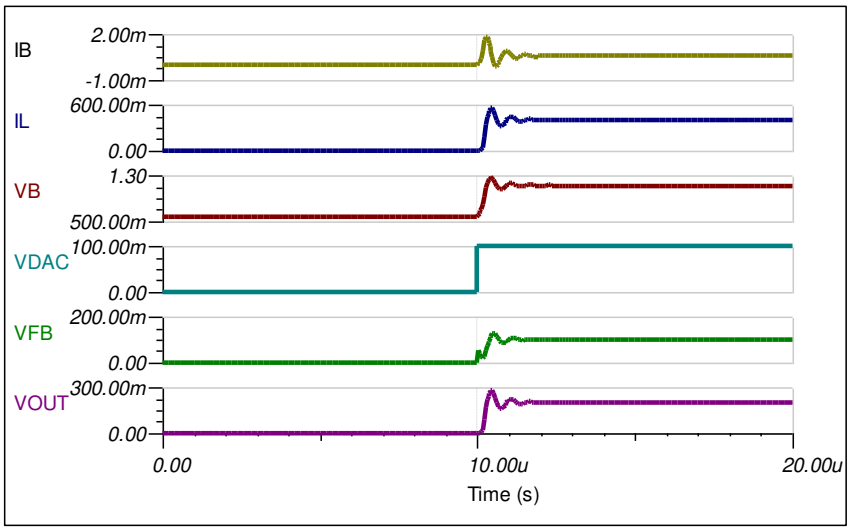


Figure 1-2. Small Signal Step Response Without Compensation

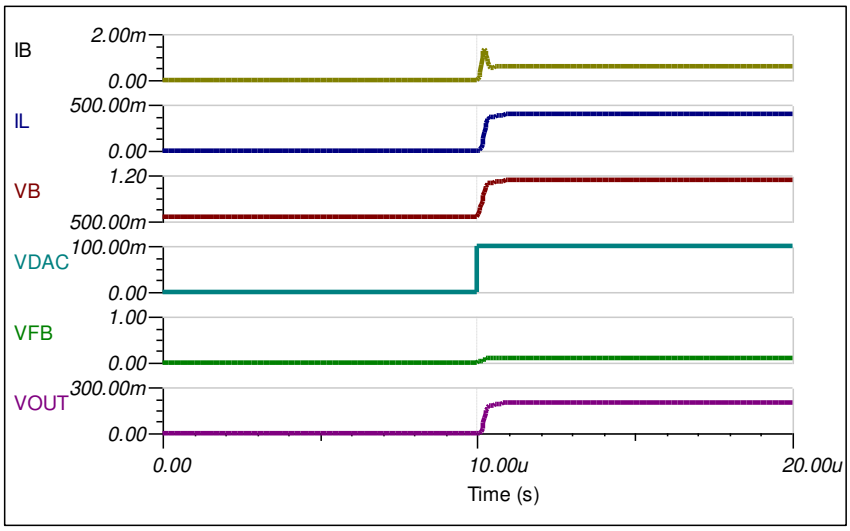
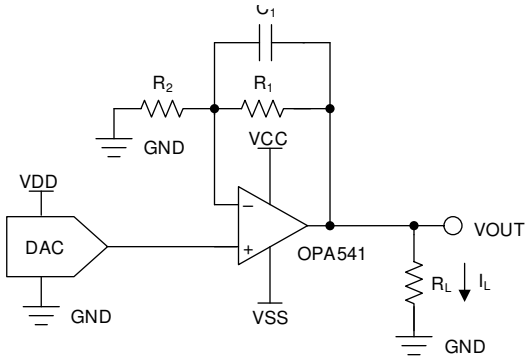


Figure 1-3. Small Signal Step Response With C_1 = 22pF

Alternative Design With Power Amplifier

The following figure depicts the simplified circuit diagram of an alternative design using a power amplifier. To achieve a high-current output from the DAC, use a power amplifier like the OPA541 device. However, as previously mentioned, this circuit can have accuracy and bandwidth limitations. Depending on the system requirements, either of the circuit topologies can be used for generating high-current output. The output transfer function of this circuit is the same as the following figure.



Design Featured Devices and Alternative Parts

Device	Key Features	Link
DAC80501	16-bit, 1-LSB INL, digital-to-analog converter (DAC) with precision internal reference	True 16-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference
DAC8551	16-Bit, ultra-low glitch, voltage output, digital-to-analog converter	16-Bit, Ultra-low Glitch, Voltage Output, Digital to Analog Converter
DAC8811	16-bit, single-channel, serial input multiplying DAC with 0.5-µs settling time	16-bit, single-channel, serial input multiplying DAC with 0.5us settling time
DAC8831	16-bit, ultra-low power, voltage output digital-to-analog converter	16-Bit, Ultra-Low Power, Voltage Output Digital to Analog Converter
OPA227	High Precision, Low Noise Operational Amplifiers	High Precision, Low Noise Operational Amplifiers
OPA541	High Power Monolithic Operational Amplifier	High Power Monolithic Operational Amplifier
THS4011	290-MHz low-distortion voltage-feedback amplifier	290-MHz Low-Distortion Voltage-Feedback Amplifier

Link to Key Files

Texas Instruments, SBAM417 sources files, software support

Trademarks

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Analog Engineer's Circuit

Space-Grade Unipolar Negative Voltage Source From Unipolar DAC Circuit

Paul Frost

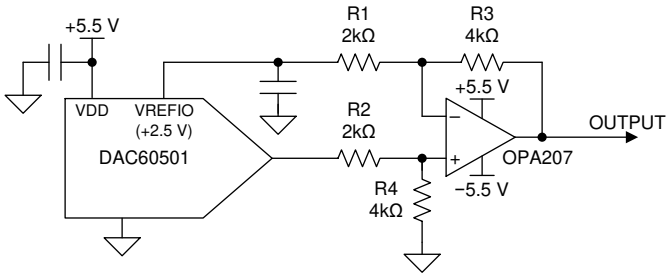
Design Goals

DAC Supply Voltage	Amplifier Supply Voltage	DAC Output Range	Output Voltage Range	Output Current Capability	Power-On Reset Output
5.5V	±5.5V	0V to 2.5V	–5V to 0V	±20mA	–5V

Design Description

This circuit shows how to convert a positive unipolar digital-to-analog (DAC) output to a negative unipolar output using only an external operational amplifier (op amp) and resistors. In many applications, such as *active antenna systems* (AAS) and *macro remote radio units* (RRU), a DAC output is used to bias the gate of gallium nitride (GaN) power amplifier (PA). For these amplifiers to be powered down, a negative potential must be applied to the gate. As such, it is beneficial to have the gate voltage be negative by default. PA biasing applications also require current output source and sink capability that usually exceeds that of most DACs.

These design goals are achieved by utilizing a voltage-output DAC that also features a reference. The DAC output and reference output are connected to differential amplifier with the reference connected to the inverting input. This enables the zero-scale output of the DAC to set the output of the amplifier to its negative full-scale value.



Design Notes

1. At power-on, the DAC output will assume a default value. This value can be configured in some devices by connecting a reset-select pin to a high or low potential, which selects a start-up value of zero-scale or mid-scale. In AAS designs, it is beneficial to start at zero-scale to ensure the PA is disabled. Other applications may require a DAC to start at mid-scale.
2. The amplifier selected must provide the output current required by the application. Rail-to-rail outputs allow the op amp power supplies to be minimized without clipping the desired output range of the circuit. In AAS applications, there is usually a capacitive load on the output as well, so capacitive load stability is important to consider.
3. The op amp must feature a bipolar supply, as the op amp inputs will always be greater than or equal to 0V in operation. The negative supply must be low enough to allow the output to reach its most negative value.

Design Steps

1. Select a DAC for the circuit based on initial on key requirements, such as the resolution, channel count, output accuracy, and power supply. These performance requirements are variable and application dependent. However, a few additional items must be considered as well.
   - The reference used to provide the offset of the differential amplifier will be required to source current. Current will flow from the reference through the resistors in the feedback network (R1 and R3) to the output of the amplifier. The maximum current would occur when the DAC output is at 0V and the output of the amplifier is at its most negative potential. The following equation shows how to calculate this current. If the current load is too great for the desired DAC reference, then a unity-gain buffer can be added to the circuit.

$$I_{REF-MAX} = \frac{V_{REF} - V_{OUT_{MIN}}}{R1 + R3}$$

   - The output of DAC will also have to drive a resistive load, comprised of R2 and R4. The maximum required current drive capability is expressed in the following equation:

$$I_{DAC-MAX} = \frac{V_{DAC-MAX}}{R2 + R4}$$

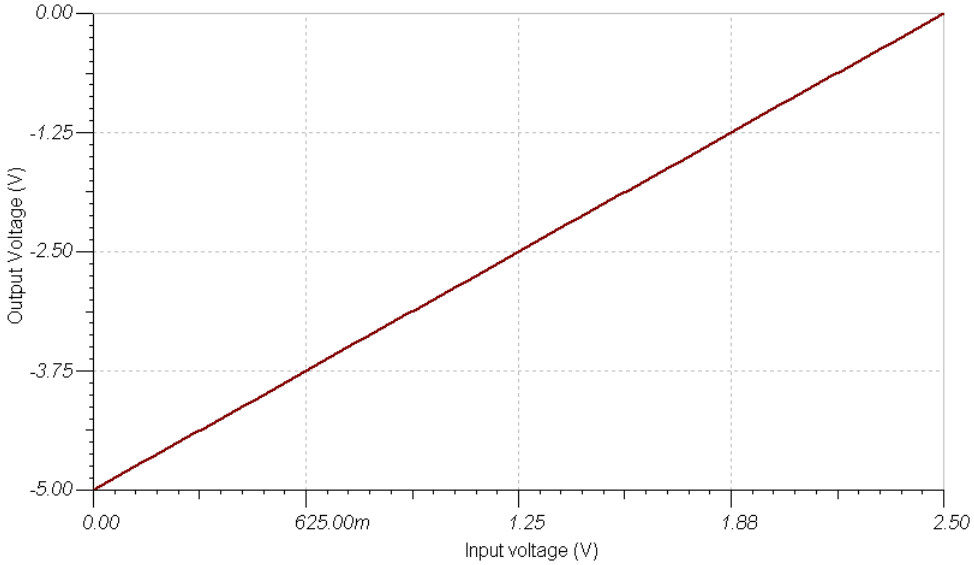
   - DACs which have an output range from 0V to V_{REF} allow the resolution to be optimized for the negative output.
2. The output range of the system can be calculated using the following equation. This is assuming that R3 and R4 are equal and R1 and R2 are equal.

$$V_{OUT} = \frac{R3}{R1}(V_{DAC} - V_{REF})$$

3. Select resistor values to achieve a balance between output noise and power consumption. Lower resistor values will minimize the thermal noise of the resistors, but increase the power dissipation. The minimum resistance values are limited by the output drive capabilities of the DAC and reference output. The accuracy of the output transfer function is heavily dependent on the accuracy of the resistor ratios. High-accuracy resistors are recommended.

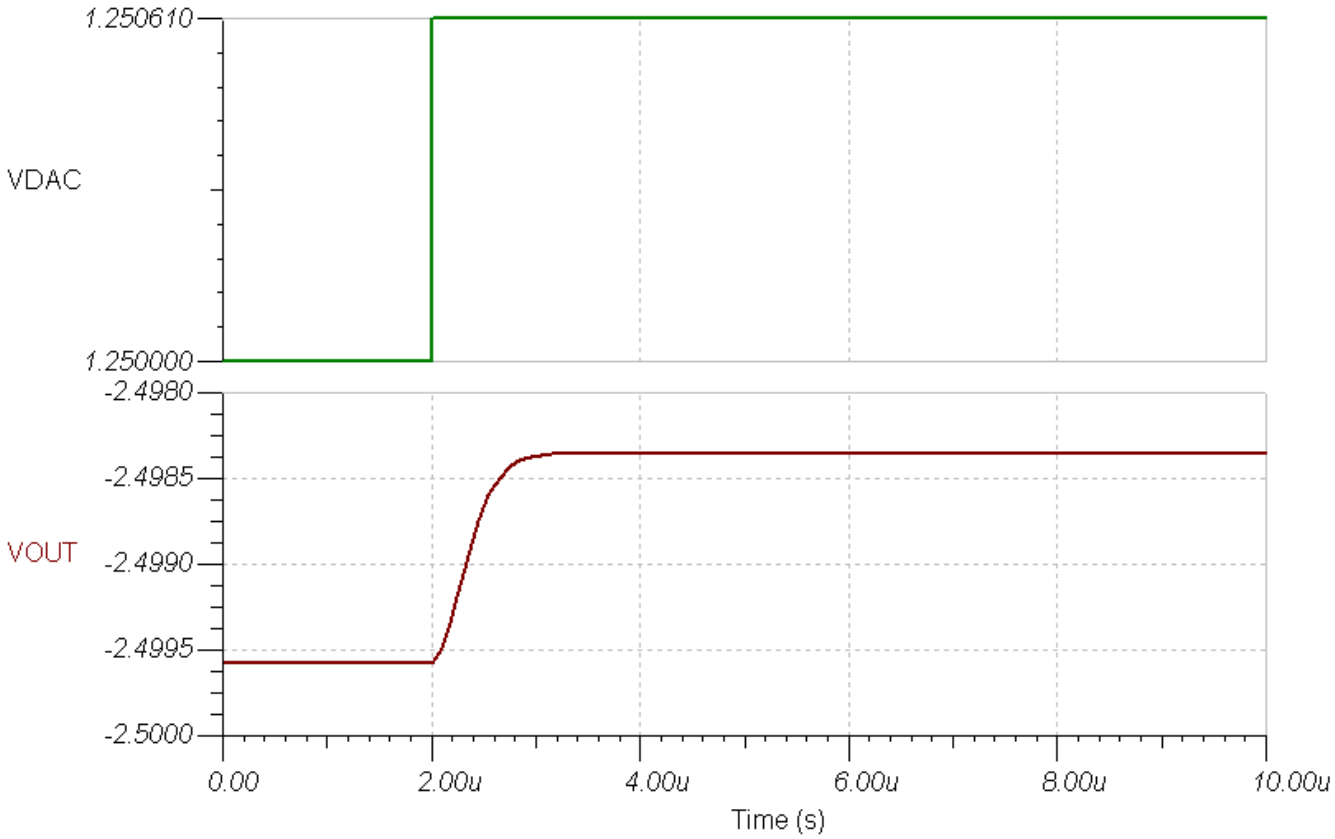
DC Transfer Characteristics

The following simulation shows the output transfer function of the circuit:



Small-Step Response

The following figure displays an LSB step response of the circuit with 15-pF load on the output.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
DAC60501	12-bit, 1-LSB, voltage-output digital-to-analog converter with precision internal reference.	True 12-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Digital-to-analog converters (DACs)
OPA207	Low-power, high-precision, low-noise, rail-to-rail output, operational amplifier	Low power (350µA), low noise (7.5nV/√Hz), high precision (100µV, 0.2µV/ºC), bipolar RRO op amp	Precision op amps (Vos<1mV)

Design References

Texas Instruments, companion simulation files for this circuit, software support

Trademarks

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Analog Engineer's Circuit

Programmable Voltage Output With Sense Connections Circuit

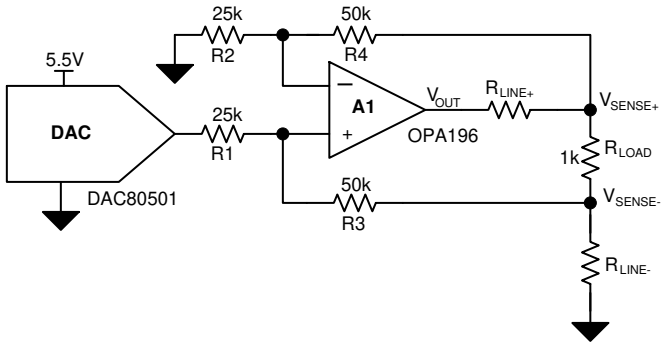
Garrett Satterfield

Design Goals

DAC Output Voltage	Output Voltage V_{LOAD}	Minimum Load Resistance R_{LOAD}	Maximum Line Resistance Compensation	Error
0V–5V	0V–10V	1kΩ	+25% of R_{LOAD}	< 0.25% FSR

Design Description

The programmable voltage output with sense connections circuit provides a precise voltage across a load, compensating for parasitic series resistance. The amplifier A1 uses feedback from the high-side and low-side of the attached load to accurately regulate the voltage between V_{SENSE+} and V_{SENSE-}. The digital-to-analog converter (DAC) output and discrete resistors set the voltage across the load. This circuit is used in applications where additional line resistance can be present and must be compensated for by increasing the output voltage to deliver the correct voltage to the load. Common end equipment that use this circuit include *analog output modules, memory and semiconductor test equipment, spectroscopy,* and *data acquisition (DAQ) cards.*



Design Notes

1. Select a DAC with low total unadjusted error (TUE) and with the required resolution for the application. A DAC with integrated reference, like the DAC80501 device, can be used to minimize components and solution size.
2. Choose a high-voltage amplifier, with rail-to-rail output to provide a sufficient output swing to drive the load and line resistance. Set the amplifer to have low offset voltage and offset voltage drift so it does not significantly contribute to output error.
3. Resistor mismatch directly contributes to gain error at the output. Use resistors with 0.05% tolerance or better and low thermal drift.
4. For correct compensation of additional line resistance the ratio of R2:R4 must match the ratio of R3:R1 as closely as possible.
5. The amplifier supply voltage is chosen based on the required output voltage, additional line resistance, and amplifier output swing at maximum load current.
6. To reduce error at zero-scale a negative voltage can be supplied to the amplifier.

Design Steps

1. The transfer function for V_{OUT} based on DAC voltage and resistor values is:

$$V_{LOAD} = \frac{R3}{R1} \cdot V_{DAC}; \quad \frac{R3}{R1} = \frac{R4}{R2}$$

2. A 50-kΩ resistance is chosen for R3. A relatively large value should be selected to reduce the current in the feedback paths. R1 is then calculated:

$$R1 = \frac{V_{DAC,FS}}{V_{LOAD,FS}} \cdot R3 = \frac{5V}{10V} \cdot 50k\Omega = 25k\Omega$$

3. R4 and R2 are chosen equal to R3 and R1, respectively.
4. Calculate the maximum load current based on the minimum load resistance and full scale V_{LOAD}. The maximum load current impacts the amplifier output voltage swing and the additional line resistance the circuit can compensate.

$$I_{LOAD,max} = \frac{V_{LOAD,FS}}{R_{LOAD,min}} = \frac{10V}{1k\Omega} = 10mA$$

5. The required V_{CC} voltage is calculated to drive 25% additional load resistance and still maintain voltage regulation across R_{LOAD}. $V_{O,rail}$ is the approximate amplifier output swing from V+ at a 10-mA load current.

$$V_{CC,min} = V_{O,rail} + 0.25 \cdot R_{LOAD,min} \cdot I_{LOAD,max} + V_{LOAD,FS} = 500mV + 250\Omega \cdot 10mA + 10V = 13V$$

6. The output error can be approximated based on the DAC TUE, amplifier offset voltage, resistor tolerance, and reference initial accuracy using root sum square (RSS) analysis.

$$\text{Output TUE(\%FSR)} = \sqrt{TUE_{DAC}^2 + \left(\frac{V_{OS}}{FSR} \cdot 100\right)^2 + 4 \cdot R^2_{Tol} + Accuracy^2_{Ref}} = \sqrt{0.1^2 + \left(\frac{100\mu V}{5V} \cdot 100\right)^2 + 4 \cdot 0.05^2 + 0.1^2} = 0.173\%$$

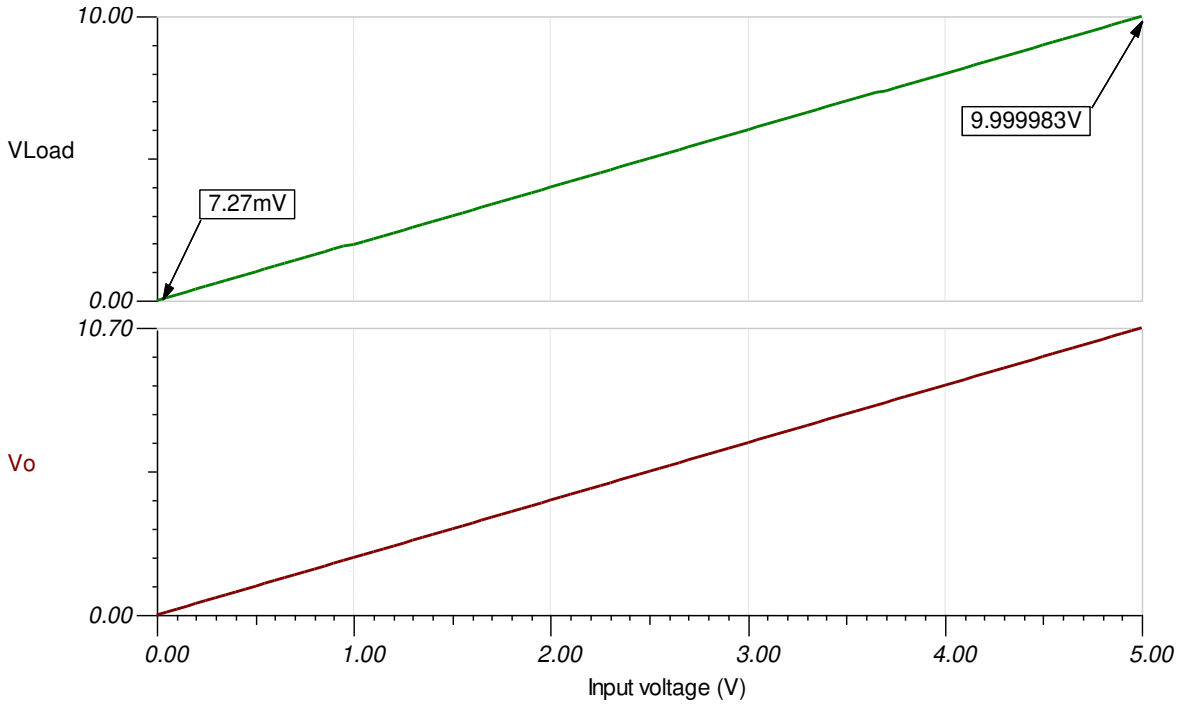


Figure 1-1. DC Transfer Characteristic

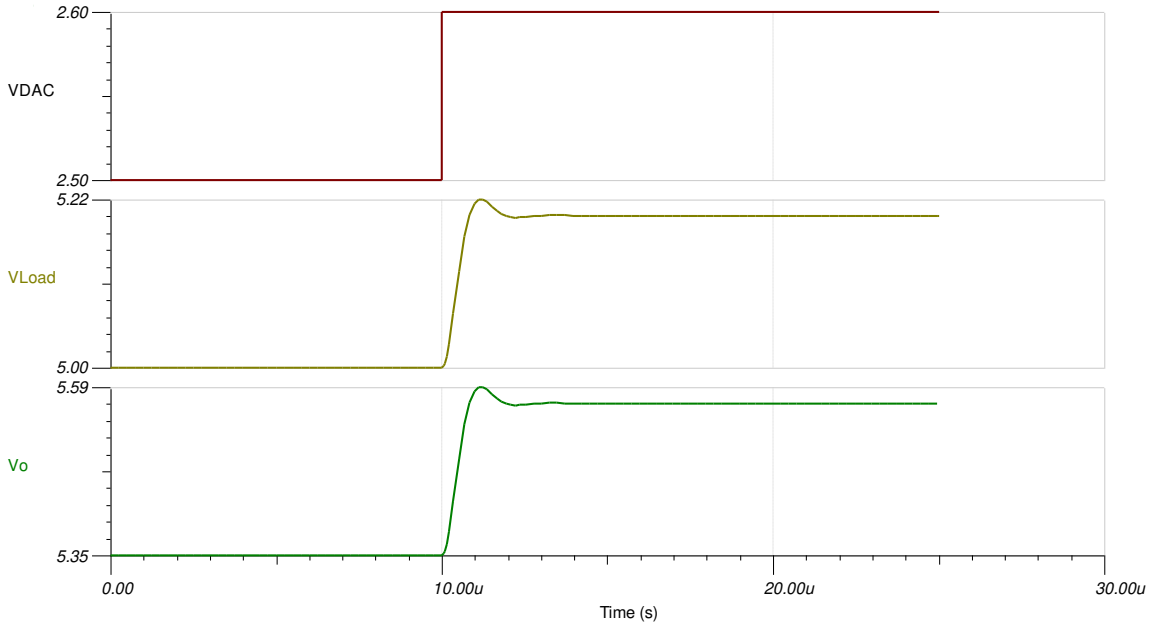


Figure 1-2. Small-Signal Step Response

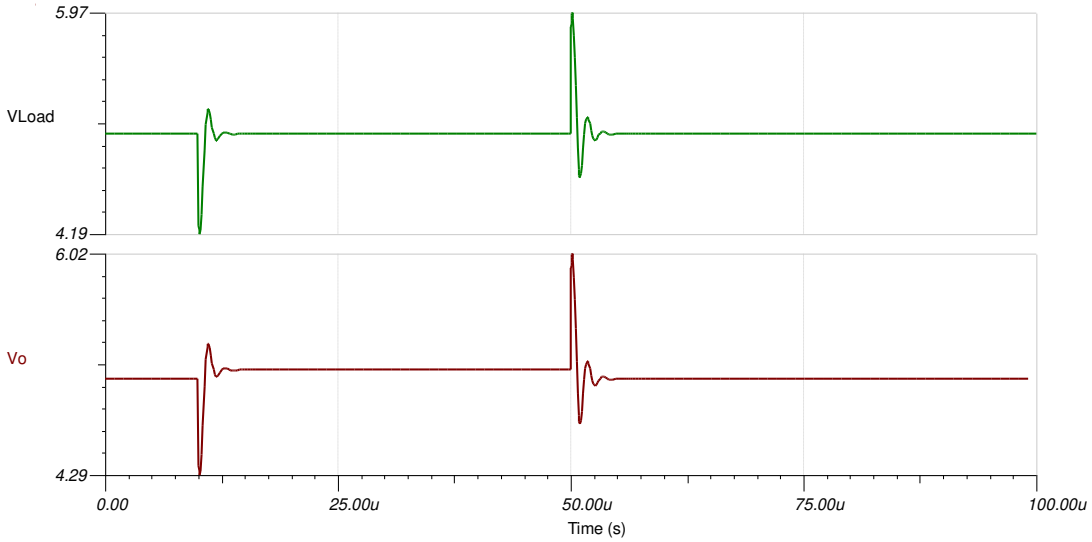


Figure 1-3. Load Transient 10kΩ to 5kΩ R_{LOAD}

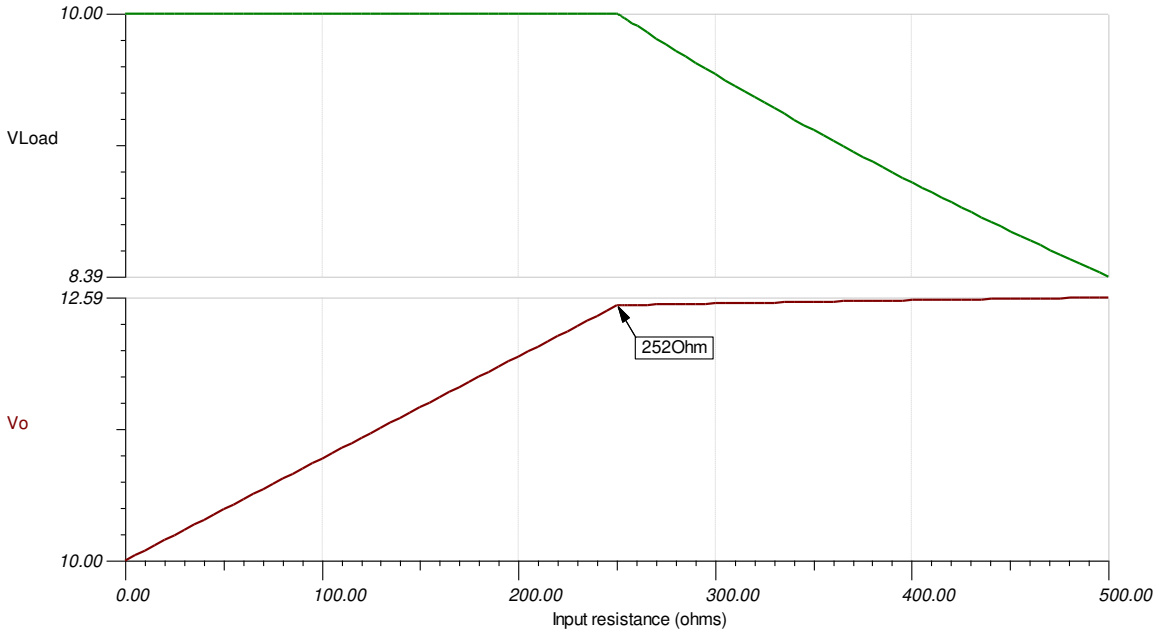


Figure 1-4. Maximum Additional Line Resistance at Amplifier V_{CC} = 13V

Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC80501	16-bit resolution, 1-LSB INL, single-channel, voltage output DAC with 5ppm/°C internal reference	True 16-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Precision DACs (≤10 MSPS)
DAC81416	16-bit resolution, 1-LSB INL, 16-channel ±20-V high-voltage output DAC with 5ppm/°C internal reference	16-channel 16-bit high-voltage output DAC with integrated internal reference	
DAC80508	16-bit resolution, 1-LSB INL, octal-channel, voltage output DAC with 5ppm/°C internal reference	True 16-bit, 8-channel, SPI, voltage-output DAC with precision internal reference	
Op Amps			
OPA196	Low-offset (100µV), Low-drift, rail-to-rail I/O, 2.25V to 36V supply	Single, 36V, low power, all-purpose amplifier with mux-friendly input	Operational amplifiers (op amps)
TLV170	Cost-sensitive, rail-to-rail output, 2.7V to 36V supply	Single, 36V, 1.2MHz, low-power operational amplifier for cost-sensitive applications	
OPA192	Precision, ultra-low offset (5µV) and drift, rail-to-rail I/O, 4.5V to 36V supply	High-Voltage, Rail-to-Rail Input/Output, 5µV, 0.2µV/˚C, Precision Operational Amplifier	

Links to Key Files

Texas Instruments, Programmable Voltage Output with Sense Connections, source files

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Analog Engineer's Circuit

Unipolar Voltage Output DAC to Bipolar Voltage Output Circuit

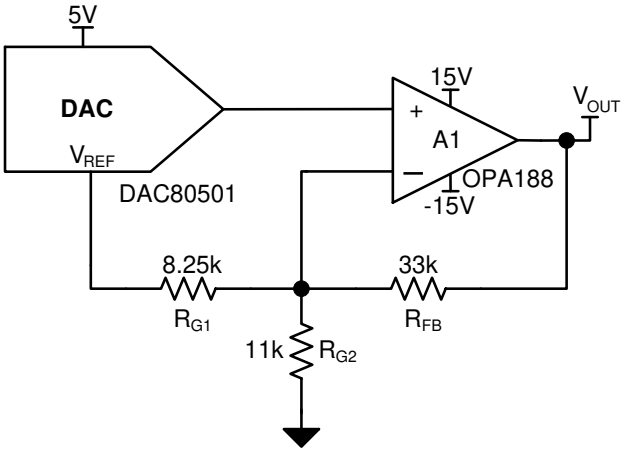
Garrett Satterfield

Design Goals

DAC Supply Voltage	Amplifier Supply Voltage	DAC Voltage	Output Voltage	Error
5V	±15V	0V–2.5V	±10V	<0.25% FSR

Design Description

The unipolar to bipolar output voltage circuit converts the voltage from a unipolar DAC into a bipolar voltage span. The circuit consists of a DAC, op amp, voltage reference, and three resistors to set the scale and span of the bipolar output voltage. This circuit is commonly used in Analog output module, Field Transmitters, and other applications requiring a programmable bipolar voltage.



Design Notes

1. Choose a DAC with low gain error, offset error, drift, and INL. Use a high-voltage op amp with low offset voltage and low offset voltage drift.
2. Use precision 0.1% or better tolerance resistors with low temperature drift.
3. Use a DAC with integrated reference to minimize solution size.

Design Steps

1. The voltage output based on DAC voltage, reference voltage, and resistors is given by:

$$V_{OUT} = \left(1 + \frac{R_{FB}}{R_{G1}} + \frac{R_{FB}}{R_{G2}}\right) V_{DAC} - \frac{R_{FB}}{R_{G1}} V_{REF}$$

2. Set the DAC voltage to zero to calculate ratio of R_{FB} and R_{G1} to create the desired negative full-scale output. Select standard resistor values to produce this gain.

$$\frac{V_{NegativeFS}}{V_{REF}} = \frac{R_{FB}}{R_{G1}} = \frac{10\,V}{2.5\,V} = \frac{33\,k\Omega}{8.25\,k\Omega}$$

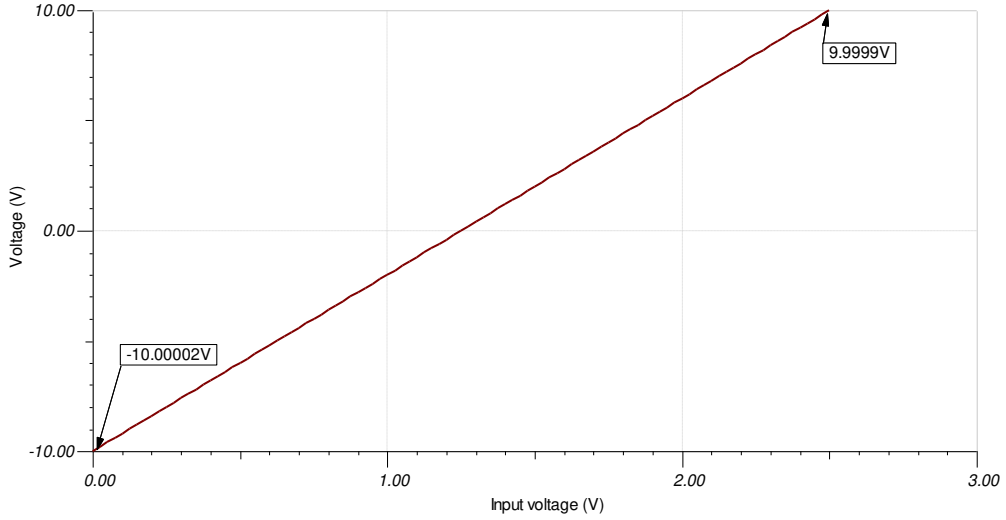
3. Calculate R_{G2} based on the full-scale range required, in this case 20V to produce ±10V range.

$$R_{G2} = \frac{R_{FB}}{\frac{V_{FSR}}{V_{DAC}} - \frac{R_{FB}}{R_{G1}} - 1} = \frac{33\,k\Omega}{\frac{20V}{2.5V} - \frac{33\,k\Omega}{8.25\,k\Omega} - 1} = 11k\Omega$$

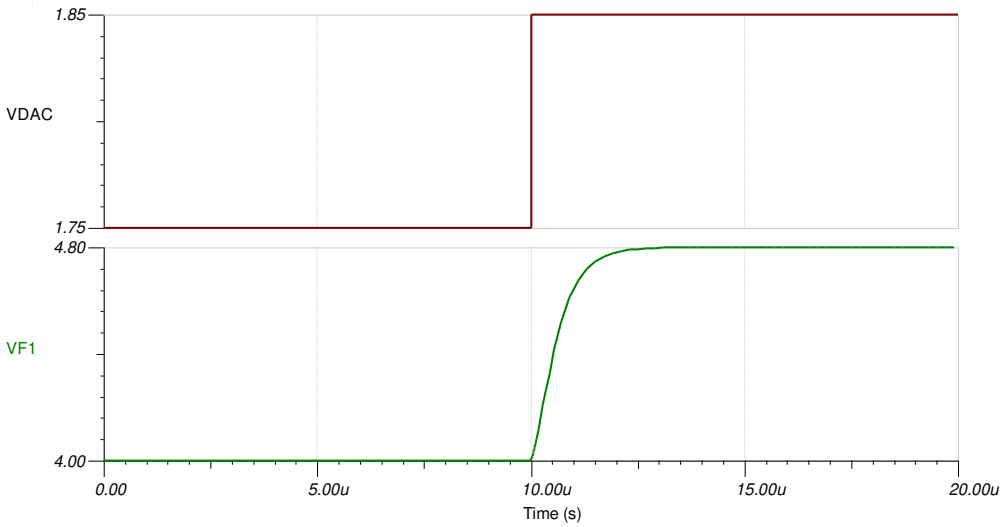
4. The output error can be approximated based on DAC TUE, amplifier offset voltage, resistor tolerance, and reference initial accuracy using root sum square (RSS) analysis.

$$\text{Output TUE (\%FSR)} = \sqrt{TUE_{DAC}^2 + \left(\frac{V_{OS,Amplifier}}{FSR} \times 100\right)^2 + Tol_{R_{G1}}^2 + Tol_{R_{G2}}^2 + Tol_{R_{FB}}^2 + Accuracy_{Ref}^2} = \sqrt{0.1^2 + \left(\frac{6\,\mu V}{2.5\,V} \times 100\right)^2 + 3 \times 0.1^2 + 0.1^2} = 0.224\%\ FSR$$

DC Transfer Characteristic



Small Signal Step Response



Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC8560	16-bit resolution, single channel, internal reference, low power, 4 LSB INL, SPI, 2V to 5.5V supply	16-bit, single-channel, low-power, ultra-low glitch, voltage output DAC with 2.5V, 2ppm/°C reference	Precision DACs (≤10 MSPS)
DAC80501	16-bit resolution, 1LSB INL, Single-Channel, Voltage Output DAC with 5ppm Internal Reference	True 16-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Precision DACs (≤10 MSPS)
DAC8830	16-bit resolution, single channel, ultra-low power, unbuffered output, 1 LSB INL, SPI, 2.7V to 5.5V supply	16-bit, single-channel, ultra-low power, voltage output DAC	Precision DACs (≤10 MSPS)
Amplifiers			
OPA188	Low-Noise, Low Offset Voltage, RRO, Zero-Drift, ±2V to ±18V supply	Precision, Low-Noise, Rail-to-Rail Output, 36V Zero-Drift Operational Amplifier	Operational amplifiers (op amps)
OPA196	Low-Power, Low Offset Voltage, RRIO, ±2V to ±18V supply	One-channel, 1MHz, rail-to-rail input and output 1.8V to 5.5V operational amplifier	Operational amplifiers (op amps)
TLV170	Cost Sensitive, Rail-to-Rail Output, ±1.35V to ±18V supply	Low Offset, Rail-to-Rail I/O Operational Amplifier	Operational amplifiers (op amps)

Links to Key Files:

Texas Instruments, *Bipolar ±10V Output from a Unipolar DAC for Industrial Voltage Drivers*, TIPD125 tool

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